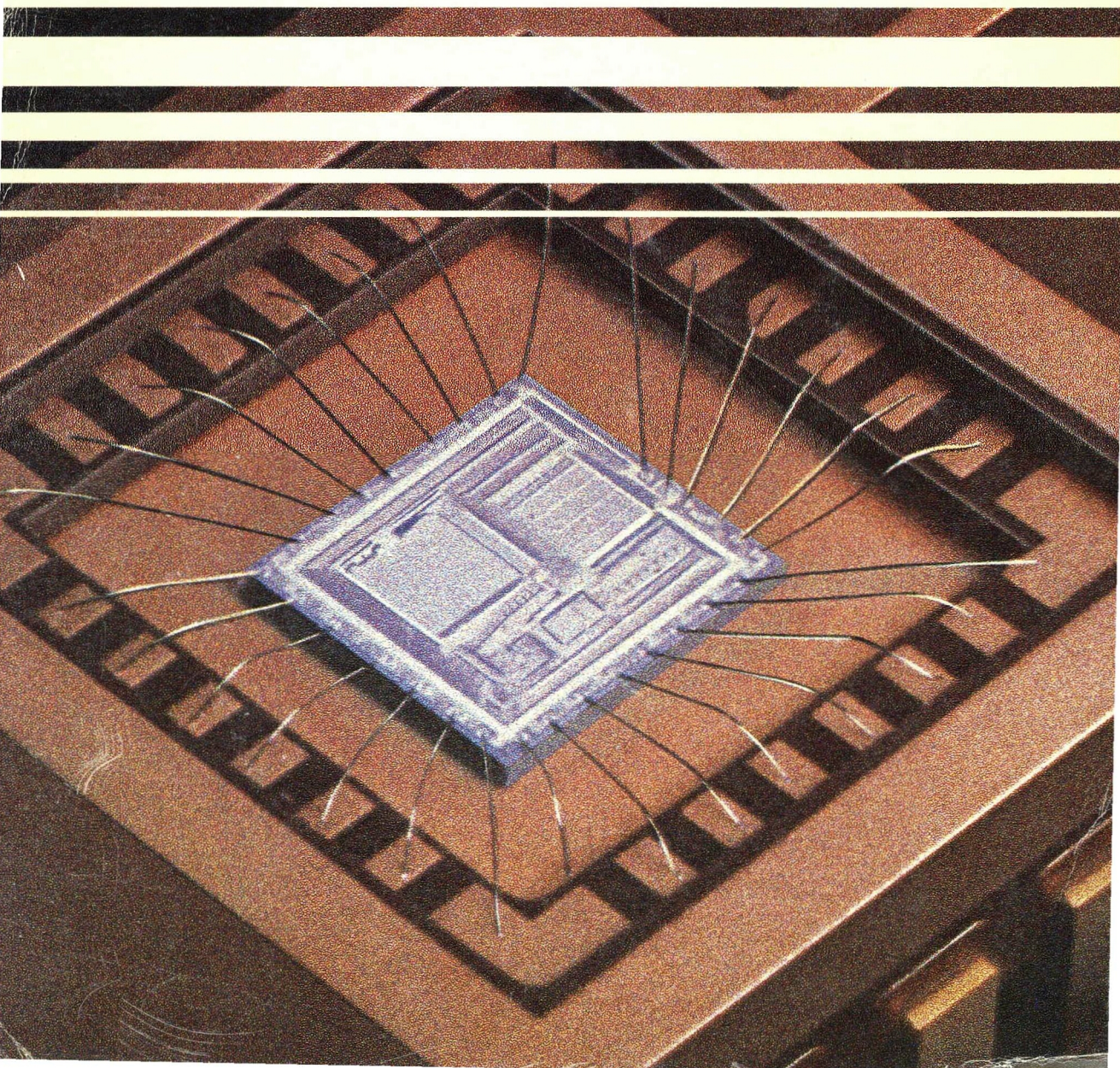
GENERAL INSTRUMENT

Microelectronics Data Catalog

1980



GENERAL INSTRUMENT

Microelectronics Data Catalog 1980

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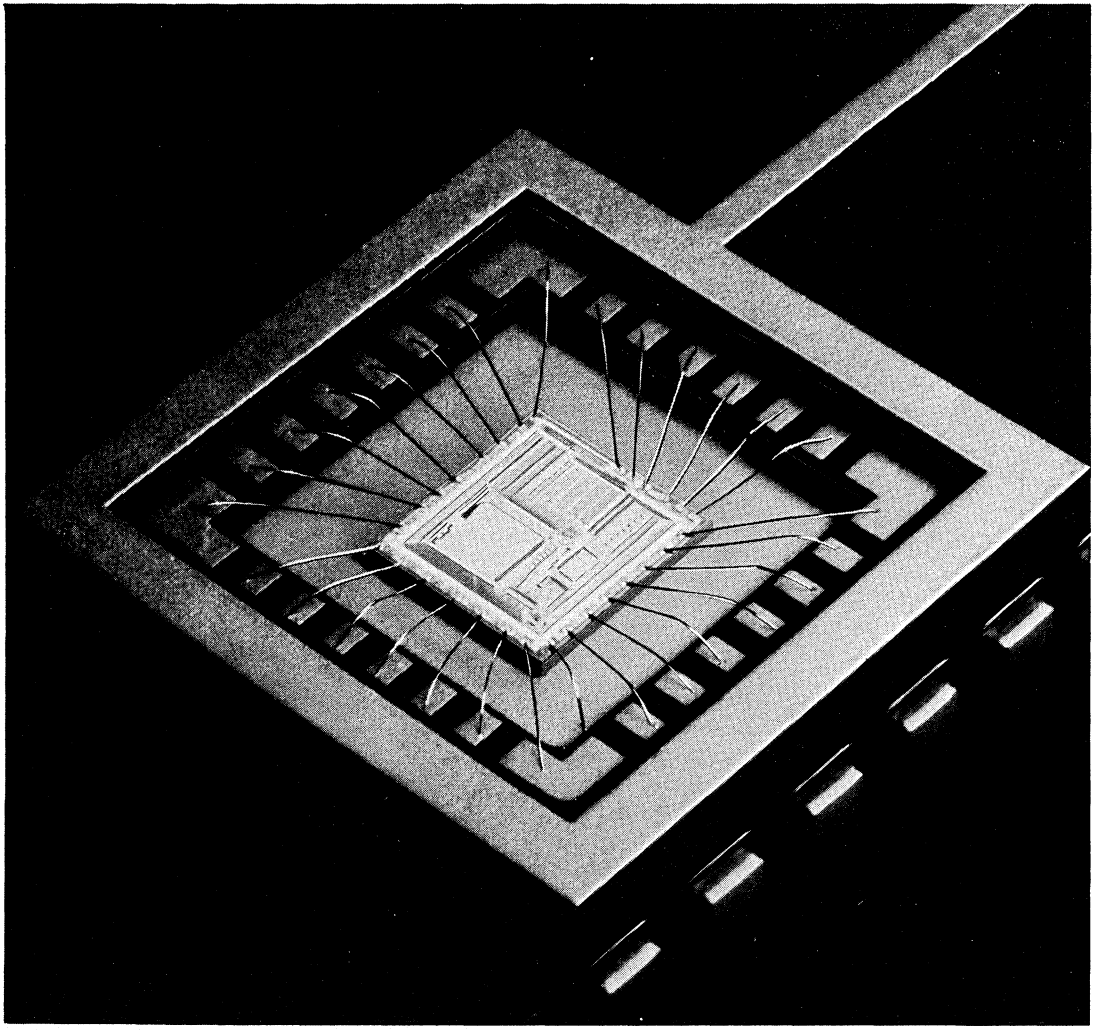

PART NUMBER INDEX

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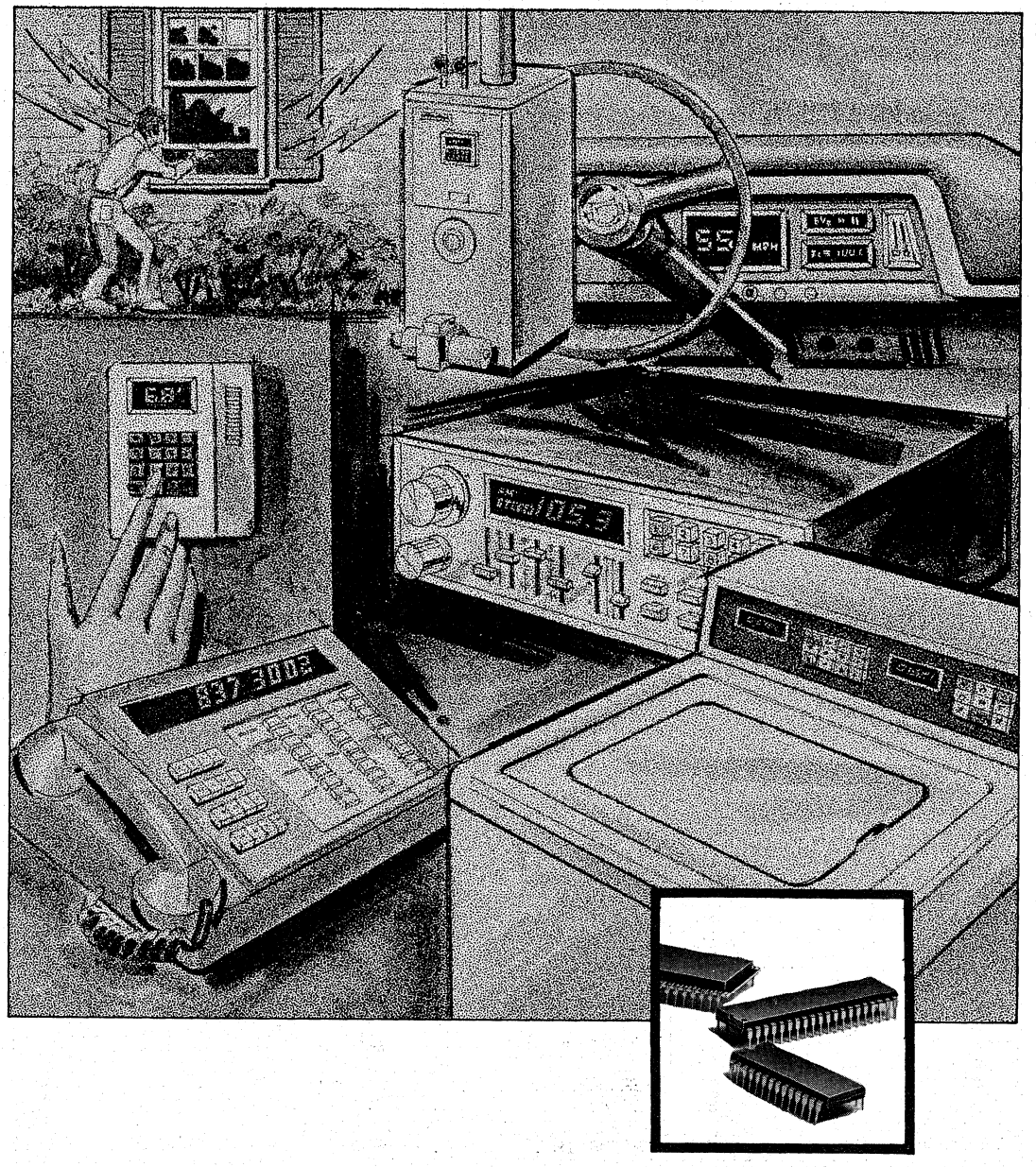
Microprocessor 2



FUNCTIONAL INDEX

GENERAL INSTRUMENT

PIC SERIES

FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES	PAGE NUMBER
8 BIT MICRO-COMPUTER	The PIC 1650 series of microcomputers contain RAM, I/O, and a central processing unit as well as a customer defined ROM to specify the overall functional characteristics of the device.	**PIC 1650A**	40 DIP	Mask programmable 512 x 12 bit program ROM. 32 8-bit registers, arithmetic logic unit and 4 sets of user-defined TTL compatible input/output lines. Self-contained oscillator. Single +5V power supply.	2-4
		PIC 1655A	28 DIP	All the features of the PIC 1650A but with fewer I/O lines (4 in, 8 out, 8 I/O).	2-16
		PIC 1656	28 DIP	All the features of the PIC 1655A but with internal and external interrupts and a 3 level stack.	2-28
PROGRAM DEVELOPMENT MICRO-COMPUTER	PIC microcomputer without ROM and with the addition of a HALT pin.	**PIC 1664B**	64 DIP	ROM address and data lines are brought out to pins to allow the use of any external RAM or PROM to aid in program development. Program can be halted or single-stepped.	2-41

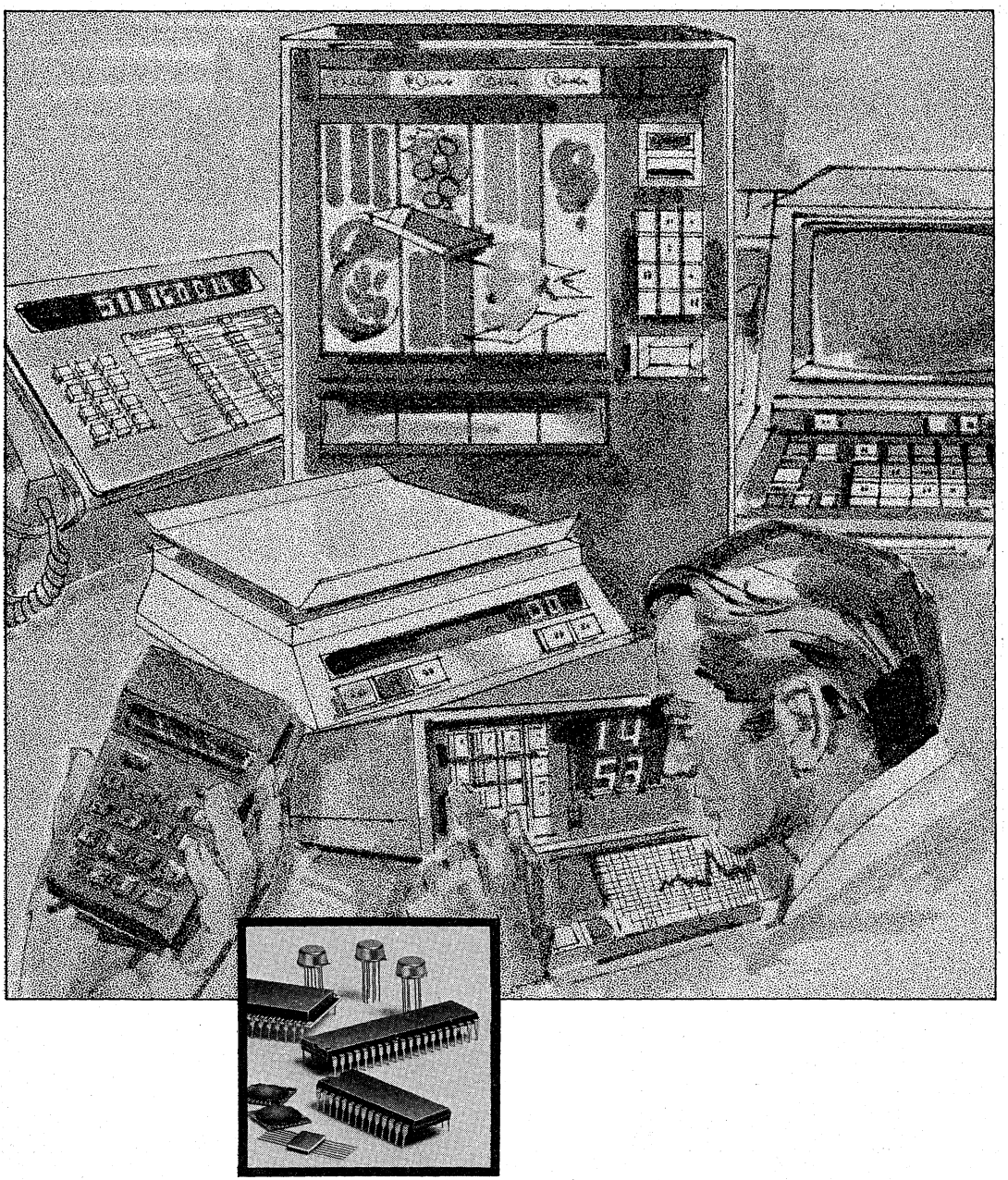
PIC DEVELOPMENT SYSTEMS

FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES	PAGE NUMBER
PIC DEVELOPMENT SYSTEM	In-circuit emulation and debug system. Can operate as stand alone system or as peripheral to host computer.	**PICES**	Console with remote module	Self contained console, with built-in power supply. Can emulate PIC 1650A, PIC 1655A, and PIC 1656 with module changes only.	2-58
PIC FIELD DEMO SYSTEMS	Contains PIC 1664B, PROMs, and provision for on-board RC oscillator or external clock.	**PFD 1000**	4" x 4-3/8" P.C. Board	Emulates PIC 1650A and PIC 1655A. Supplied with ribbon cable terminated with a 40 DIP or 28 DIP plug to demonstrate a PIC system before committing to a masked PIC program.	2-60
		PFD 1010	4" x 4-3/8" P.C. Board	Emulates PIC 1656. Supplied with ribbon cable terminated with a 28 DIP plug to demonstrate a PIC system before committing to a masked PIC program.	2-60
PIC ASSEMBLER	Converts symbolic source programs for the PIC series into object code.	**PICAL**	—	Produces an output file which may be loaded and executed by the PICES or used to directly mask program a PIC chip. Written in Fortran IV to achieve compatibility with most computer systems. Supplied as magnetic tape or floppy disks.	2-61

SERIES 1600

FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES	PAGE NUMBER
16 BIT MICRO-PROCESSOR	Third generation minicomputer architecture with 8 general purpose registers.	**CP1600**	40 DIP	8 program accessible 16-bit general purpose registers. 87 basic instructions. 4 addressing modes. Unlimited interrupt nesting and priority resolution. 16-bit 2's complement arithmetic and logic. Cycle times: 600ns (CP1600), 1μs (CP1610).	2-64
		CP1610	40 DIP		2-64
D/A CONVERTER	Contains 4 x 10 bit D/A registers.	**DAC 1600**	40 DIP	10-bit bidirectional data bus. Synchronous/asynchronous loading. Manual input mode. Designed to interface to a process control loop.	2-71
I/O BUFFER	A programmable buffer with 16 bidirectional lines.	**IOB 1680**	40 DIP	Single 16-bit or dual 8-bit I/O ports. Parity check on both ports. Three levels of priority. Automatic handshake logic and signals.	2-75
ANALOG MULTIPLEXER	Binary addressed mux, includes on-chip address latch.	**MUX 1600**	28 DIP	Connects 1 of 18 analog inputs. On-chip address latch. 0 to 6 Volt input range. Analog output controlled by chip select signal.	2-81
READ ONLY MEMORY	2048 x 10 bits	**RO-3-9504**	28 DIP	Includes on-chip address latches, bus control logic, and 5-bit chip select decode.	2-83

FUNCTIONAL INDEX
ROM 3



READ ONLY MEMORIES

FUNCTION	DESCRIPTION	PART NUMBER	REPLACES	ACCESS TIME	CLOCKS / VOLTAGE	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NUMBER
5K ROM	5,120 bits organized 512 x 10	**RO-3-5120**	EA4000	500ns	Static	+5	24 DIP		**3-4**
16K ROM	16,384 bits organized 2,048 x 8	**RO-3-8316A**	INTEL 8316A	850ns	Static	+5	24 DIP		**3-6**
		RO-3-8316B	AMI S6831A	450ns					**3-6**
		RO-3-9316A	INTEL 8316E	850ns	Static	+5	24 DIP	Replaces 2716 UV EPROM.	**3-6**
		RO-3-9316B	AMI S6831B	450ns					**3-6**
		RO-3-9316C	SY2316B	350ns					**3-6**
32K ROM	32,768 bits organized 4,096 x 8	**RO-3-9332A**	TMS4732	850ns	Static	+5	24 DIP		**3-11**
		RO-3-9332B	SY2332	450ns					**3-11**
64K ROM	65,536 bits organized 8,192 x 8	***RO-3-9364B**	MK36000	450ns	Static	+5	24 DIP	Edge-activated.	**3-14**

*For future release.

Note: All Read Only Memories are mask-programmable.

KEYBOARD ENCODERS

FUNCTION	DESCRIPTION	PART NUMBER	REPLACES	ACCESS TIME	CLOCKS / VOLTAGE	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NUMBER
KEYBOARD ENCODERS	2,376 bits organized as 88 keys x 3 modes x 9 bits.	**AY-5-2376**	SMC KR2376	10-100kHz Scan rate	1/TTL or Int. Osc.	+5, −12	40 DIP	2 key rollover.	**3-18**
	3,600 bits organized as 90 keys x 4 modes x 10 bits.	**AY-5-3600**	SMC KR3600	10-100kHz Scan rate	1/TTL or Int. Osc.	+5, −12	40 DIP	2/N key rollover.	**3-29**
		AY-5-3600-PRO	—					Preprogrammed binary codes.	**3-29**
CAPACITIVE KEYBOARD ENCODER	4,592 bits organized as 112 keys x 4 modes x 10 bits, plus 112 bits for internal programming of "function" keys.	**AY-3-4592**	—	11-66kHz Scan rate	1/TTL or Int. Osc.	+5	40 DIP	Also usable: inductive, Hall effect, mechanical switches.	**3-32**

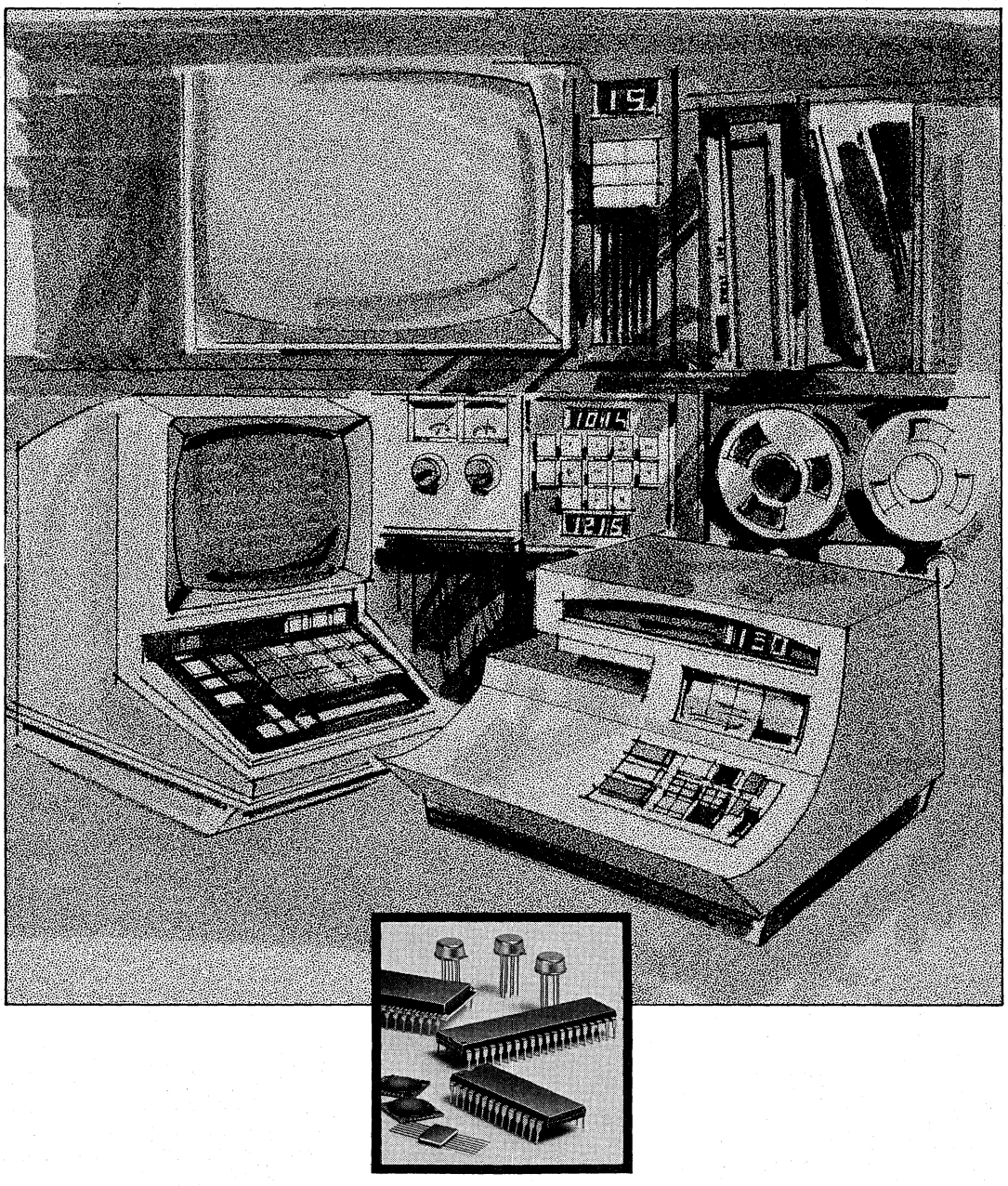
Note: Standard patterms are available.

CHARACTER GENERATOR

FUNCTION	DESCRIPTION	PART NUMBER	REPLACES	ACCESS TIME	CLOCKS/ VOLTAGE	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NUMBER
CHARACTER GENERATOR	2,560 bits organized as 64 - 5 x 8 characters.	**RO-3-2513**	SIG 2513	450ns	Static	+5	24 DIP	Row output.	**3-44**

Note: Standard patterns are available.

FUNCTIONAL INDEX
EAROM 4



ELECTRICALLY ALTERABLE READ ONLY MEMORIES

FUNCTION	DESCRIPTION	PART NUMBER	READ ACCESS	ERASE TIME	WRITE TIME	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NUMBER
82 BIT EAROM	82 bits organized 82 x 1	**ER0082**	100μs	Included in write time.	200ms	+5, −30	18 DIP	Bit erase	**4-3**
1400 BIT SERIAL EAROM	1400 bits organized 100 x 4	**ER1400**	2.8μs	16ms	16ms	−35	14 DIP	Word erase	**4-6**
512 BIT EAROM	512 bits organized 32 x 16	**ER2051**	1μs	50ms	50ms	+5, −28	28 DIP	Word erase	**4-9**
	512 bits organized 64 x 8	**ER2055**	2μs	50ms	50ms	+5, −28	22 DIP	Word erase	**4-12**
4K EAROM	4096 bits organized 1024 x 4	**ER3400**	900ns	10ms	1ms	+5, −12, −30	22 DIP	Word/bulk erase	**4-19**

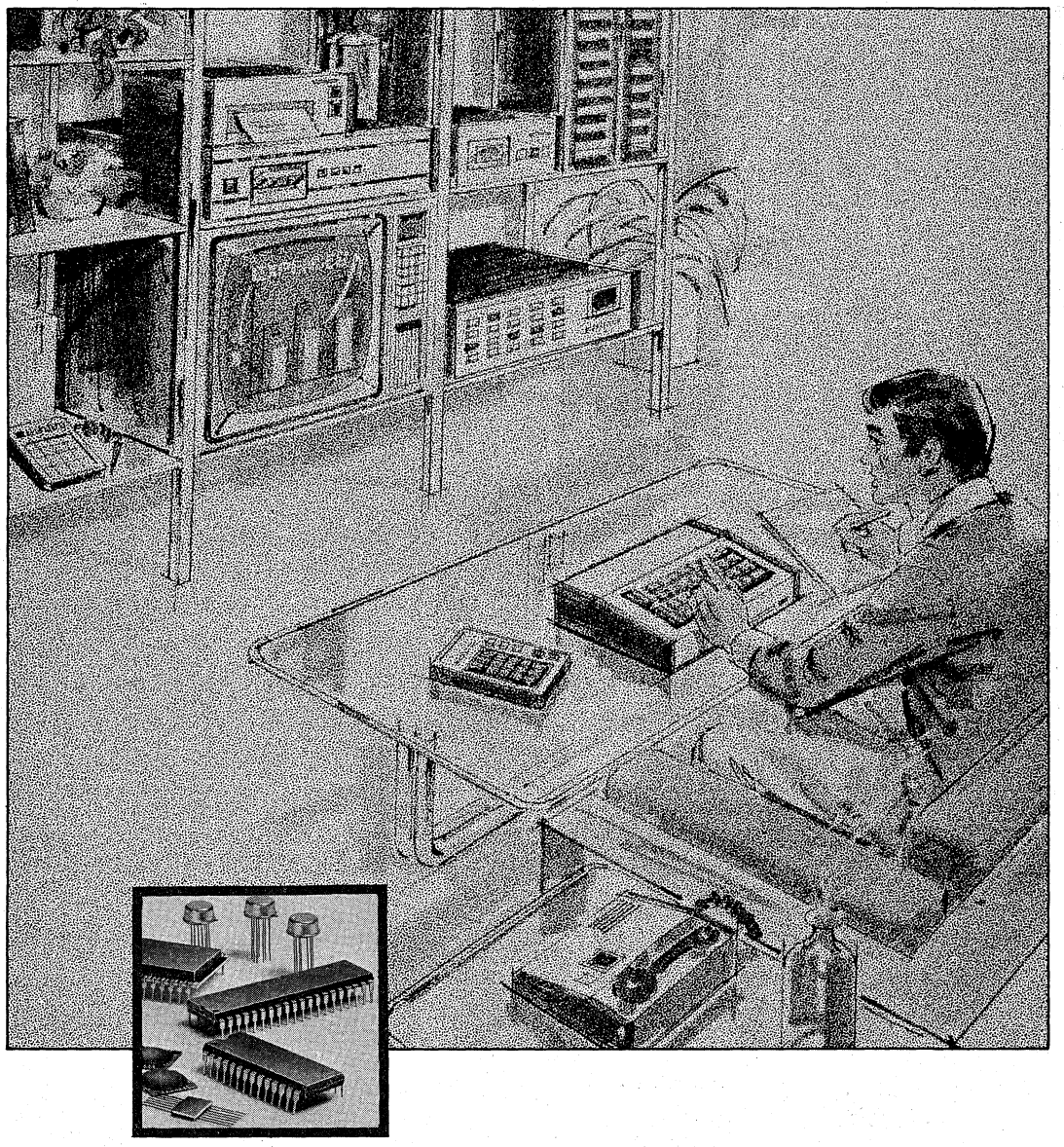
Also available are EAROMs which operate across extended temperature ranges. These devices are designed for use in military and industrial applications where high reliability product is essential.

INDUSTRIAL/MILITARY EAROMs

FUNCTION	DESCRIPTION	PART NUMBER	OPERATING TEMPERATURE	883B/ 5004 SCREENING	SUPPLY VOLTAGES	PACKAGE	READ ACCESS	ERASE TIME	WRITE TIME	PAGE NUMBER
512 BIT EAROM	512 bits organized 32 x 16	**ER2051 HR**	−55°C to +125°C	X	+5, −28	28 DIP	4.5μs	100ms	100ms	**4-9**
		ER2051 IR	−40°C to +85°C	X						
	512 bits organized 64 x 8	**ER2055 HR**	−55°C to +125°C	X	−5, +28	22 DIP	6.0μs	100ms	100ms	**4-12**
		ER2055 IR	−40°C to +85°C	X						
4K EAROM	4096 bits organized 1024 x 4	**ER3400 HR**	−55°C to +125°C	X	−5, +12, −30	22 DIP	1000ns	20ms	2ms	**4-19**
		ER3400 IR	−40°C to +85°C	X						
8K EAROM	8192 bits organized 2048 x 4	**ER2810 HR**	−55°C to +125°C	X	+5, +14, −24	24 DIP	2.0μs	100ms	500ms	**4-15**
		ER2810 IR	−40°C to +85°C	X						

NOTE: HR devices are available over full temperature without Burn-in. Check Factory for further information on this option.

FUNCTIONAL INDEX
Personal Terminal 5



PERSONAL TERMINALS

FUNCTION	DESCRIPTION	PART NUMBER	SYSTEM FUNCTION	PACKAGE	FEATURES	PAGE NUMBER
"8900" HOME INFORMATION SYSTEM	The "8900" Home Information System is a powerful system for video display of game, educational, financial, research and related "home computer" service information with detailed graphics definition and manipulation.	CP1610	MICROPROCESSOR	40 DIP	A variant of the GI CP1600 microprocessor, the CP1610 is a 16-bit unit for fast and efficient processing of all home information center data.	5-3
		AY-3-8900 AY-3-8900-1	TV INTERFACE	40 DIP	The "STIC", Standard Television Interface Chip, provides the video signals for interaction of all graphics data generated by the system.	5-10
		RO-3-9502	PROGRAM ROM	40 DIP	The 20K program ROM, organized as 2048 x 10, contains the executive program plus resident home information center routines.	5-13
		RO-3-9503	GRAPHICS ROM	40 DIP	The 16K graphics ROM, organized 2048 x 8, contains 256 8 x 8 matrices for a large variety of symbols, background/field data, and alpha-numerics.	5-16
		RA-3-9600	SYSTEM RAM	40 DIP	The "working" memory during home information center operation—contains a 352 x 16 read/write memory plus a 20 word "current line" buffer.	5-18
	The basic Home Information System can easily be expanded to include additional functions through the use of cartridge ROMs and increased memory, and further enhanced with full color operation, complex sound effects generation, and interface to audio cassette decks and other peripherals.	RO-3-9504	CARTRIDGE ROM	28 DIP	The 20K cartridge ROM, organized as 2048 x 10, contains additional program instructions and symbol characteristics—custom programmable.	5-21
		AY-3-8910	SOUND GENERATOR	40 DIP	Provides full software programmability for complex sound effects generation without external timing components. Dual 8-bit I/O ports.	5-23
		AY-3-8915	COLOR PROCESSOR	16 DIP	Accepts digital R,G,B,Y, and sync signals from AY-3-8900-1 and generates a single composite color signal.	5-30
		IOB 1680	INPUT/OUTPUT BUFFER	40 DIP	A programmable interface with dual 8-bit I/O ports, parity checking on both ports, three priority levels, automatic handshake logic and signals.	2-75
TELEVIEW SYSTEM	The Teleview System is a powerful system to display information on a TV receiver. It can store data from either telephone line or TV RF signals information.	PIC 1650	MICROCOMPUTER	40 DIP	A PIC series microcomputer programmed to control the Teleview receiver system. It receives keyboard commands to store data and operate system functions.	5-37
		AY-3-9710	DATA ACQUISITION CHIP	40 DIP	The Data Acquisition chip receives data from Teletext or Viewdata formats and loads it into correct location in a preselected page of memory.	5-38
		AY-3-9725	VIDEO GENERATOR	40 DIP	The Video Generator chip reads the contents of pages in memory and generates outputs suitable for driving a standard 625 line TV receiver.	5-45
		AY-3-1014A	UART	40 DIP	The UART is used to capture serial data from telephone lines, and convert it into 8-bit parallel data for acquisition.	6-80

FUNCTIONAL INDEX
Telecommunications 6

TELEPHONY

	FUNCTION	DESCRIPTION	PART NUMBER	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NUMBER
	5 CHANNEL RELAY DRIVER	Isolates +5V logic and exchange-powered relays.	**AY-5-9050**	+5, −48	14 DIP	Separate logic and exchange grounds, each driver is capable of supplying 50mA.	**6-4**
	PUSH BUTTON TELEPHONE DIALLERS	Converts push button input to rotary dial pulses.	**AY-5-9100**	See data sheet.	18 DIP	20 digit storage, selectable dialling rate, selectable mark/space ratio, selectable inter-digital pause. Redial of last number and access pause facility (except on AY-5-9118).	**6-6**
			AY-5-9151A/52	+2.5 to +5	18 DIP		**6-10**
			AY-5-9153A/54A		28 DIP		**6-10**
			***AY-5-9158**		18 DIP		**6-16**
	REPERTORY DIALLER	Stores ten 22 digit telephone numbers.	**AY-5-9200**	See data sheet.	16 DIP	Complements the AY-5-9100 series to provide storage of up to ten 22 digit telephone numbers. Stackable.	**6-19**
	DUAL-TONE MULTI-FREQUENCY GENERATORS	Generates DTMF/tone telephone frequencies.	**AY-3-9400**	+5	14 DIP	12 tone pairs, 3.52 dB high group pre-emphasis.	**6-25**
			AY-3-9401		16 DIP	16 tone pairs, 2 dB high group pre-emphasis.	**6-25**
			AY-3-9410		16 DIP	16 tone pairs, 3 or 6 dB high group pre-emphasis.	**6-25**
	CLOCK GENERATOR	Generates 2-phase clocks from a single power supply.	**AY-5-9500**	−4 to −15	14 DIP	Generates the 2-phase clocks for the AY-5-9100/9200.	**6-28**
	DUAL-TONE MULTI-FREQUENCY RECEIVERS	Detects and converts DTMF/ tone telephone frequencies.	**AY-5-9801**	+8.5, −8.5	28 DIP	4 bit output code, on-chip Op Amps.	**6-32**
			AY-5-9802		40 DIP	1 of 16 output code, on-chip Op Amps.	**6-32**
			AY-5-9803		40 DIP	2 of 8 output code, on-chip Op Amps.	**6-32**
			AY-5-9804		28 DIP	Binary output code, on-chip Op Amps.	**6-32**
			AY-5-9805		24 DIP	4 bit output code.	**6-32**
			AY-5-9807		24 DIP	2 of 8 output code.	**6-32**
			AY-5-9808		24 DIP	Binary output code.	**6-32**
NEW	CODEC	Duplex Delta-Sigma/PCM converter.	**AY-3-9900**	+9, +5	24 DIP	With external D-S modulator, provides full duplex PCM. Pin-selectable A-Law/μ-Law.	**6-37**
	MICRO-COMPUTER DIALLERS	A single-chip microcomputer pre-programmed for in-telephone applications.	**TZ2001**	+5	40 DIP	Push button dialling (pulse output), display of up to 12 dialled digits, 32 telephone number storage with one button selection, 6 digit clock and elapsed time display.	**6-44**
NEW			**TZ2002***	+5	40 DIP	Dual tone code dialling, display of up to 12 dialled digits, 16 telephone number storage with one button selection and a 6 digit clock.	**6-44**
NEW			**TZ2003***	+5	40 DIP	Pulse or Dual tone code dialling up to 16 dialled digits, 32 telephone number storage with two button selection.	**6-44**

*For future release

TELECOM HYBRIDS

FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES	PAGE NUMBER
UNIVERSAL ACTIVE FILTERS	Generate any filter response by means of external connections.	ACF 7092C	16 DIP	The design provides for independent control of Frequency, Q, and Amplifier Gain, and is usable throughout the frequency range of 10Hz to 10kHz.	6-52
LOW PASS FILTERS	PCM transmit filter.	ACF 7270C	8 SIP	Minimum 32dB attenuation at 4.2kHz and an in-band ripple of ±0.125dB from 300Hz to 3kHz.	6-56
	PCM receive filter.	ACF 7271C	8 SIP	Minimum 32dB attenuation at 4.2kHz. Compensated for sinx/x response.	6-58
BAND PASS FILTERS	Full wave detector and a factory tunable four pole fixed bandwidth band pass filter.	ACF 7300C ACF 7301C ACF 7302C	14 DIP	Center frequency range (F_o): 540Hz to 1980Hz. Center frequency range (F_o): 700Hz to 1700Hz. Center frequency range (F_o): 2280Hz to 3825Hz.	6-60
	Detects and passes the 2600Hz signalling frequency.	ACF 7310C	28 DIP	Minimum attenuation from center frequency of 2600Hz: 30dB ± 200Hz, 50dB ± 500Hz, 70dB ± 1000Hz. Center frequency gain: 0 ± 0.5dB.	6-62
	DTMF/tone detection band pass filters.	ACF 7323C ACF 7363C ACF 7383C	12 TO 10 SIP 16 DIP	These two pole constant Q filters are available in the standard AT&T tone frequencies and in the standard MF steps.	6-64 6-66 6-68
	Detects and passes the 2800Hz signalling frequency.	ACF 7328C	28 DIP	Minimum attenuation from center frequency of 2800Hz: 30dB ± 200Hz, 50dB ± 500Hz, 70dB ± 1000Hz. Center frequency gain: 0 ± 1.5dB.	6-70
BAND REJECTION FILTERS	Rejects the 2600Hz signalling frequency.	ACF 7410C	34 DIP	1000Hz gain: −9 ± .5dB. Pass band gain: 0 ± .5dB referred to 1000Hz gain. Minimum attenuation of 60dB ± 15Hz and maximum attenuation of 5dB ± 400Hz from the center frequency of 2600Hz.	6-72
		ACF 7412C	34 DIP	1000Hz gain: 0 ± .75dB. Pass band gain: 0 ± .25dB referred to 1000Hz gain. Minimum attenuation of 30dB ± 15Hz and maximum attenuation of 3dB ± 120Hz from the center frequency of 2600Hz.	6-73
		NCS 2061**	17 SIP	Unsymmetrical frequency response. 1000Hz gain: 0 ± .25dB. 2400Hz gain: −5dB min. 2600Hz ± 15Hz gain: −45dB max. 3000Hz gain: 0 ± 1dB. 3200Hz gain: 0 ± 1dB.	6-74
	Rejects the 2800Hz signalling frequency.	NCS 2062**	17 SIP	Unsymmetrical frequency response. 1000Hz gain: 0 ± .25dB. 2000Hz gain: −.4dB min. 2400Hz gain: 0 ± 1dB. 2800Hz gain: −45dB max. 3000Hz gain: −5dB min. 3200Hz gain: 0 ± 1dB.	6-74
BAND SEPARATION FILTERS	Isolates low and high groups of DTMF frequencies.	ACF 7711C	16 DIP	Minimum attenuation of 30dB for the adjacent frequencies of 941Hz and 1209Hz. 0dB in the pass bands, 25dB out of band.	6-75
	DTMF Low Group Band Splitting Filter	ACF 7720C*	14 SIP	Minimum 30dB attenuation from 1190Hz to 1658Hz. 1.5dB ± 1.5dB gain from 686Hz to 955Hz.	6-77
	DTMF High Group	ACF 7721C*	14 SIP	Minimum 30dB attenuation from 686Hz to 955Hz. 1.5dB ± 1.5dB gain from 1190Hz to 1658Hz.	6-78

*For future release. **Sold as matched pair only.

DATA COMMUNICATIONS

FUNCTION	DESCRIPTION	PART NUMBER	MAXIMUM BAUD	MAXIMUM FREQUENCY	TEMP. RANGE	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NUMBER
UAR/T	Complete 5-8 bit receiver/ transmitter interface.	AY-5-1013A	40kB	640kHz	0 to 70	+5, −12	40 DIP	1 or 2 stop bits.	6-80
		AY-6-1013	22.5kB	360kHz	−55 to +125	+5, −12			
		AY-3-1014A	30kB	480kHz	0 to 70	+5 to +14		1, 1½, or 2 stop bits	6-80
		AY-3-1015D	30kB	480kHz	0 to 70	+5			
16 CHANNEL MULTIPLEXER	Multiplexes 16 analog channels with on-chip logic control.	AY-5-1016	—	2MHz	0 to 70	+5, −12	40 DIP	Current mode or voltage mode.	6-93
		AY-6-4016			−55 to +125				

FUNCTIONAL INDEX
Entertainment 7

RADIO

FUNCTION	DESCRIPTION	PART NUMBER	SYSTEM FUNCTION	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NUMBER
PROGRAMMABLE PLL TUNING CONTROLLERS	Provides full electronic control of a varactor tuned AM/FM radio mask programmable for custom tuning functions. (ref. ER1400 for optional unpowered memory.)	AY-3-8118	CONTROLLER	+12	40 DIP	Programmable microcomputer based chip. Provides up to 10 AM or FM station storage, on board PLL, Fluorescent display drivers, and RAM storage. Optional EAROM can be added for power off memory.	7-4
	Microcomputer radio tuning controller. (ref. ER2055 for optional unpowered memory.)	*AY-3-8120		+5		AM/FM stero controller circuit with 5 AM and 5 FM favorite station Memory-EAROM and R/C compatible.	7-10

*For future release.

TELEVISION

FUNCTION	DESCRIPTION	PART NUMBER	SYSTEM FUNCTION	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NUMBER
OMEGA 82 CHANNEL TUNING SYSTEM	Provides full electronic control of a varactor-tuned 82-channel television from a two-digit calculator-like keyboard entry.	T-1002	CONTROLLER	+12	40 DIP	Accepts keyboard/remote inputs to control system.	7-14
		T-1102	DISPLAY DRIVER	+12	40 DIP	Stores, decodes, displays selected channel number.	7-14
		ER1400	EAROM MEMORY	+12, −24	14 DIP	Non-volatile storage of station tuning information.	7-18
		MEM 4956	D/A CONVERTER	+12, V_{REF}	14 DIP	Converts output to coarse and fine tune outputs.	7-21
		T-1201	FAVORITE CHANNEL MEMORY	+12	40 DIP	A 20-line EAROM for single-digit channel selection.	7-14
ECONOMEGA 16 CHANNEL TUNING SYSTEM	Provides full electronic control of a varactor-tuned 8, 12 or 16 channel television, featuring automatic or manual tuning.	AY-3-8203	CONTROLLER	+12	40 DIP	Accepts direct/remote inputs to control system.	7-24
		ER1400	EAROM MEMORY	+12, −24	14 DIP	Non-volatile storage of station tuning information.	7-18
		MEM 4956	D/A CONVERTER	+12, V_{REF}	14 DIP	Converts output to coarse and fine tune outputs.	7-21
*ECONOMEGA IIA TUNING SYSTEM	Provides electronic control of a varactor tuned TV from keyboard entry.	AY-3-8211	CONTROLLER	+12	40 DIP	Accepts keyboard/remote inputs to control system	7-30
		ER1400	EAROM MEMORY	+12, −24	14 DIP	Non-volatile storage of station tuning information.	7-18
*ECONOMEGA IV PLL TUNING SYSTEM	A five chip TV frequency synthesizer system.	AY-9-2010	PRESCALER/PREAMP	+30, +12, +5 −23	8 DIP	100 channel PLL TV tuner-32 favorite channel Memory-EAROM and R/C Compatible.	7-38
		AY-3-2022	FREQ. SYNTHESIZER		24 DIP		7-38
		PIC 1650A	CONTROLLER		40 DIP		7-38
		ER1400	NON-VOLATILE MEM		14 DIP		7-38
		AY-9-2017	PERIPHERAL CIRCUIT.		18 DIP		7-38

FUNCTION	DESCRIPTION	PART NUMBER	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NUMBER
ON-SCREEN CHANNEL/TIME DISPLAY	Various circuits in series to display channel numbers on TV screen with some additionally featuring either separate or simultaneous time display (ref. AY-5-1203A clock circuit)	AY-5-8301	+18	14 DIP	Channels 1-16, upper right screen display.	7-39
		AY-5-8320		24 DIP	Channels 1-16 and/or time, upper right screen display, automatic on channel change.	7-39
		AY-5-8321	+12			7-39
ON-SCREEN TUNING SCALE	Provides an electronic on-screen tuning scale for varactor-tuned TV sets.	AY-3-8331	+12	16 DIP	Four bands, mask-programmable band or channel number display and display position.	7-48

*For future release.

REMOTE CONTROL

FUNCTION	DESCRIPTION	PART NUMBER	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NUMBER
R/C SYSTEM I	30 channel discrete frequency ultrasonic transmitter.	**AY-5-8450**	+9	16 DIP	30 control frequencies, interfaces with a 5 x 6 matrix keyboard.	**7-52**
	16 channel discrete frequency ultrasonic receivers.	**AY-5-8460**	+12, −6	18 DIP	Interfaces directly with OMEGA keyboard, plus on/off, recall, 4 analog functions.	**7-54**
R/C SYSTEM II	264 command PCM transmitter.	**AY-3-8470**	+9	28 DIP	8-bit PCM system plus 8 PWM analog commands. 4 x 8 keyboard (32 x 8 with shifts).	**7-58**
	264 command PCM receiver.	**AY-3-8475**	+12	40 DIP	5-bit program output. CPU data bus interface for full 264 functions.	**7-64**

SOUND GENERATION

FUNCTION	DESCRIPTION	PART NUMBER	MAXIMUM FREQUENCY	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NUMBER
TOP OCTAVE GENERATORS	Generates a complete octave of musical frequencies.	**AY-1-0212**	1.5MHz	−14, −27	16 DIP	12 outputs, 50% duty cycle.	**7-72**
		AY-3-0214	4.5MHz	+10 to +16	16 DIP	12 outputs, 50% duty cycle.	**7-74**
		AY-3-0215				13 outputs, 50% duty cycle.	**7-74**
LATCHING NETWORK	Establishes priority of 13 pedal latch inputs/outputs.	**AY-1-1313**	20kHz	−12, −27	40 DIP	Stackable for expanded latching/ priority function.	**7-76**
CHORD GENERATOR	Produces major, minor, 7th chords, walking bass.	**AY-5-1317A**	50kHz	−15	40 DIP	Mixed outputs, sustain, top key priority.	**7-78**
PIANO KEYBOARD	Electronically simulates piano keyboard operation.	**AY-1-1320**	—	−10, −27	40 DIP	12 keys per unit, "loudness" proportional to key press velocity.	**7-82**
FREQUENCY DIVIDERS	7 stage dividers.	**AY-1-5050**	1MHz	−13, −27	14 DIP	Arranged 3+2+1+1.	**7-86**
PROGRAMMABLE SOUND GENERATORS	Generates programmable sound effects via a microcomputer compatible bus without the aid of external components.	**AY-3-8910**	2MHz	+5	40 DIP	Register oriented bus input has 3 analog outputs with 2 8 bit bus I/O ports.	**7-88**
		AY-3-8912			28 DIP	Same as AY-3-8910 except has only 1 8 bit I/O port.	**7-88**
NEW MICRO-COMPUTER TUNES SYNTHESIZER	Produces musical tunes from pre-programmed micro-computer.	**AY-3-1350**	1MHz	+5	28 DIP	Contains 28 tunes each 8 notes in duration. Adjustable pitch and time duration. Can be custom programmed with up to 252 notes of music.	**7-95**

FUNCTIONAL INDEX
Consumer 8

TV GAMES

FUNCTION	DESCRIPTION	PART NUMBER	GAMES	LINE STANDARD	PACKAGE	FEATURES	PAGE NUMBER
BALL & PADDLE	Six selectable games for one or two players, with vertical paddle motion.	AY-3-8500	Tennis Practice Soccer Rifle I Squash Rifle II	625	28 DIP	On-screen scoring. Sound generation. Selectable paddle size, ball speed, rebound angles.	8-4
		AY-3-8500-1		525			
ROADRACE	One or two player games where racing skill in "traffic" generates the highest score.	AY-3-8603	Roadrace Qualify	625	28 DIP	Each player maneuvers around other cars on the race track. Color display with the AY-3-8615.	8-19
		AY-3-8603-1		525			
NEW WARFARE	One or two player games featuring subs, destroyers, cargo ships, and spaceships.	AY-3-8605	Sea Battle Counterattack I&II Night Battle Space Battle I&II	625	28 DIP	Fire depth charges, missiles, and torpedoes. Varied skill selection. Color display with the AY-3-8615.	8-22
		AY-3-8605-1		525			
WIPEOUT	One or two player games where players "wipe out" objects by controlling a ball in the play area.	AY-3-8606	Wipeout I-IV Color Squares I-IV Breakthrough I&II	625	28 DIP	Skill selection including paddle size, ball size, and ball speed. Color display with the AY-3-8615.	8-27
		AY-3-8606-1		525			
SHOOTING GALLERY	Twelve games for one or two players using external photocell rifles for shooting.	AY-3-8607	Skeet I-IV Attack I-IV Destruct I-IV	625	28 DIP	Three dimensional target effect by diminishing target size. Color display with the AY-3-8615.	8-36
		AY-3-8607-1		525			
SUPERSPORT	Ten selectable games for one or two players, with vertical and horizontal paddle motion.	AY-3-8610	Tennis Practice Hockey Gridball Soccer Basketball I&II Squash Target I&II	625	28 DIP	Realistic ball service & scoring. Individually selectable paddle sizes. Color-coded score. Color display with the AY-3-8615.	8-42
		AY-3-8610-1		525			
COLOR PROCESSOR	Adds color to the "8600" series dedicated TV Game circuits.	AY-3-8615	—	525	28 DIP	Colors changed by the "game select" inputs.	8-53

CLOCKS

FUNCTION	DESCRIPTION	PART NUMBER	FLASHING SECONDS	ZERO BLANKING	50/60Hz OPERATION	PACKAGE	FEATURES	PAGE NUMBER
4 DIGIT	12/24 hour clocks with features for most clock/timing applications.	AY-5-1202A	✓	✓	✓	24 DIP	For 7-segment fluor. display.	8-60
		AY-5-1203A	✓		✓	24 DIP	BCD outputs.	8-60
		AY-5-1224A		✓	✓	16 DIP	BCD or 7-seg. LED outputs.	8-63
4 DIGIT CLOCK RADIO	12/24 hour clock, 24 hour alarm, sleep timer, battery standby.	CK3300	✓	✓	✓	28 DIP	Includes snooze alarm and pre-settable timeswitch.	8-65

APPLIANCES

FUNCTION	DESCRIPTION	PART NUMBER	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NUMBER
CLOCK / TIMERS	24 hour programmable, repeatable on/off time switch with 4 digit clock.	AY-5-1230	−12 to −18	28 DIP	50Hz input (50 or 60Hz on AY-5-1231), BCD or 7-segment direct fluorescent display drive outputs, zero blanking, 24 hour display (12 or 24 hour on AY-5-1231).	8-78
		AY-5-1231		40 DIP		8-78
		AY-5-1232		28 DIP		8-78
NEW DIGITAL THERMOMETER	Digital Thermometer and temperature controllor	AY-3-1270	+9	40 DIP	For LCD/LED display, ±1°C accuracy, power fail/over-range indication (flashing display), adjustable hysteresis.	8-82

COUNTERS / DVMs

FUNCTION	DESCRIPTION	PART NUMBER	MAX. COUNT FREQUENCY	SUPPLY VOLTAGES	PACKAGE	FEATURES	PAGE NUMBER
3½ DIGIT DVM	DVM logic utilizing dual ramp integration.	AY-5-3507	40kHz	−15	18 DIP	Range to 1999, 7-segment outputs.	8-94
3¾ DIGIT DVM	DVM logic utilizing single ramp integration.	AY-5-3500	200kHz	−7.5, −15	28 DIP	Ranges: 999, 1999, 2999. Dual polarity, BCD & 7-segment outputs.	8-99
4 DIGIT COUNTER/ DISPLAY	Counts, stores, and decodes 4 decades to 7-segment outputs.	AY-5-4007	600kHz	+5, −12	24 DIP	BCD outputs, true/complement control.	8-103
		AY-5-4007A			40 DIP	Includes all features of AY-5-4007 and AY-5-4007D.	8-103
		AY-5-4007D			24 DIP	Serial output with shift clock input, 3 carry outputs.	8-103
FLUORESCENT DISPLAY DRIVER	Direct drive to fluorescent display stores and siplay with internal max clock.	AY-5-4121	25KHz	−12V,	40 DIP	BCD to Fluorescent display 7 segments 21 digits.	8-109
		AY-5-4221				7 segment to Fluorescent display 7 segments 21 digits.	8-110

Microprocessor 2

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
			PIC Series
8 BIT MICROCOMPUTER	The PIC 1650 series of microcomputers contain RAM I/O and a central processing unit as well as a customer defined ROM to specify the overall functional characteristics of the device.	PIC 1650A	2-4
		PIC 1655A	2-16
		PIC 1656	2-28
PROGRAM DEVELOPMENT MICROCOMPUTER	PIC microcomputer without ROM and with the addition of a HALT pin.	PIC 1664B	2-41
			PIC Development Systems
PIC DEVELOPMENT SYSTEM	In-circuit emulation and debug system. Can operate as stand alone system or as peripheral to host computer.	PICES	2-58
PIC FIELD DEMO SYSTEMS	Contains PIC 1664B, PROMs, and provision for on-board RC oscillator or external clock.	PFD 1000	2-60
		PFD 1010	2-60
PIC ASSEMBLER	Converts symbolic source programs for the PIC series into object code.	PICAL	2-61
			Series 1600
16 BIT MICROPROCESSOR	Third generation minicomputer architecture with 8 general purpose registers.	CP1600 CP1610	2-64
D/A CONVERTER	Contains 4 x 10 bit D/A registers.	DAC 1600	2-71
I/O BUFFER	A programmable buffer with 16 bidirectional lines.	IOB 1680	2-75
ANALOG MULTIPLEXER	Binary addressed mux, includes on-chip address latch.	MUX 1600	2-81
READ ONLY MEMORY	2048 x 10 bits.	RO-3-9504	2-83

PIC Series

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
8 BIT MICROCOMPUTER	The PIC 1650 series of microcomputers contain RAM, I/O and a central processing unit as well as a customer defined ROM to specify the overall functional characteristics of the device.	PIC 1650A	2-4
		PIC 1655A	2-16
		PIC 1656	2-28
PROGRAM DEVELOPMENT MICROCOMPUTER	PIC microcomputer without ROM and with the addition of a HALT pin.	PIC 1664B	2-41

8 Bit Microcomputer

FEATURES

- User Programmable
- Intelligent Controller for Stand-Alone Applications
- 32 8-bit RAM Registers
- 512 x 12-bit Program ROM
- Arithmetic Logic Unit
- Real Time Clock Counter
- Self-contained Oscillator
- Access to RAM Registers inherent in instruction
- Wide Power Supply Operating Range (4.5V to 7.0V)
- Available in two temperature ranges: 0° to 70° C and −40° to 85° C
- 4 Sets of 8 User Defined TTL-compatible Input/Output Lines
- 2 Level Stack

DESCRIPTION

The PIC 1650A microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit ALU.

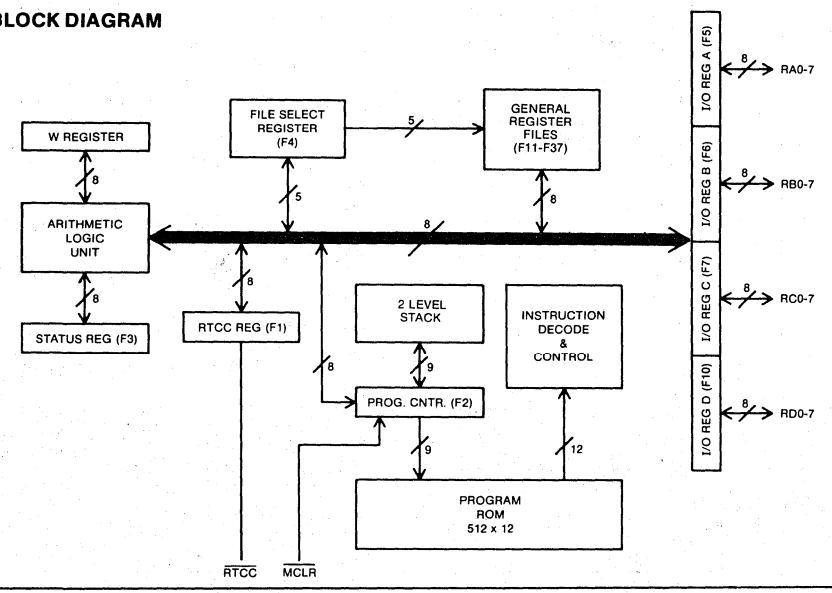
The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC 1650A is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or buffered crystal oscillator signal, for greater accuracy) to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC 1664B. The PIC 1664B is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD 1000 Field Demo System is available containing a PIC 1664B with sockets for erasable CMOS PROMs. Finally, the PICES (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

PIC 1650A BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The primary purpose of the PIC is to perform logical processing, basic code conversions, formatting, and to generate fundamental timing and control signals for I/O devices. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

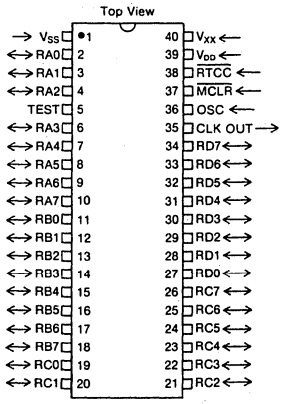
The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the $\overline{\text{MCLR}}$ input on power up initializes the ROM program to address 777_8.

PIN FUNCTIONS

Signal	Function
OSC (input)	Oscillator input. This signal can be driven by an external oscillator if a precise frequency of operation is required or an external RC network can be used to set the frequency of operation of the internal clock generator. This is a Schmitt trigger input.
$\overline{\text{RTCC}}$ (input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The RTCC register increments on falling edges applied to this pin. This register can be loaded and read by the program. This is a Schmitt trigger input.
RA0-7, RB0-7, RC0-7, RD0-7 (input/output)	User programmable input/output lines. These lines can be inputs and/or outputs and are under direct control of the program.
$\overline{\text{MCLR}}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch all I/O register high. Should be held low at least 1ms past the time when the power supply is valid. This is a Schmitt trigger input.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
TEST	Used for testing purposes only. Must be grounded for normal operation.
V_{DD}	Primary power supply.
V_{XX}	Output Buffer power. Used to enhance output current sinking capability.
V_{SS}	Ground

PIN CONFIGURATION

40 LEAD DUAL IN LINE



REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$.
F2	Program Counter (PC).The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2).The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	1	1	1	Z	DC	C

C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.

DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

Z (Zero): Set if the result of an arithmetic operation is zero.

Bits: 3-7 These bits are defined as logic ones.

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	I/O Register A (A0-A7)
F6	I/O Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10	I/O Register D (D0-D7)
F11-F37	General Purpose Registers

Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

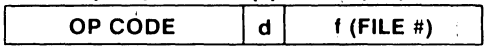
For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1MHz the instruction execution time is 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

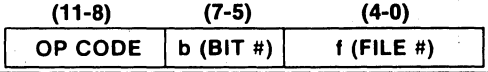
BYTE-ORIENTED FILE REGISTER OPERATIONS



For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

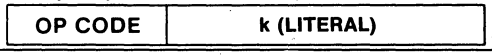
Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\bar{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1),f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇋f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	kVW→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore. subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

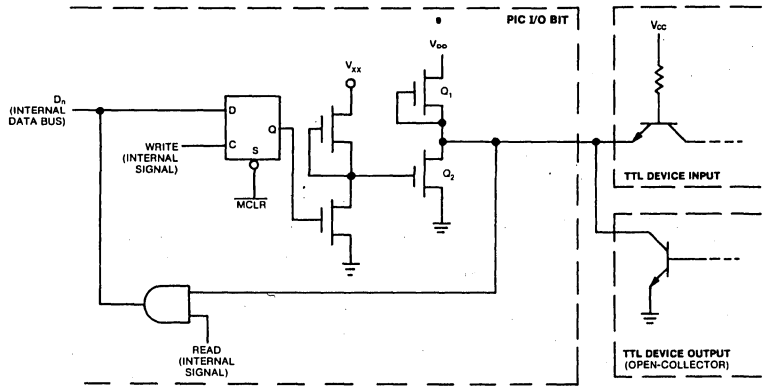
The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Programming Cautions

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation.

Bidirectional I/O Ports

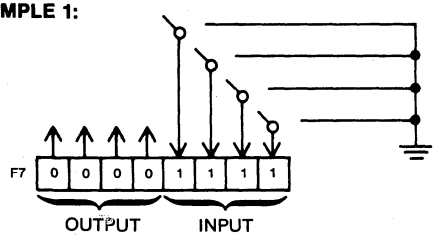
The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the intput/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:



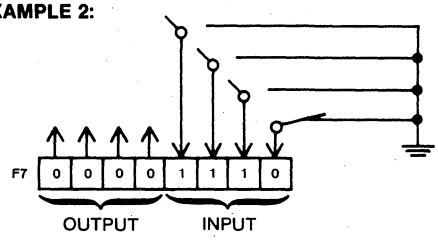
What is thought to be happening:

BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low:

BSF 7,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any pin with Respect to V_{SS} ..... −0.3V to +12.0V
Power Dissipation 1000mW
Power Dissipated by any one I/O pin (Note 1) 60mW
Power Dissipated by all I/O pins (Note 1) 600mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	55	mA	No Load
Output Buffer Supply Current	I_{XX}	—	1	5	mA	No Load (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC when driven externally)	V_{IH1}	2.4	—	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH2}	V_{DD}−1	—	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	—	V_{DD}	V	I_{OH} = −100μA provided by internal pullups (Note 4)
Output Low Voltage (I/O only)	V_{OL1}	—	—	0.45	V	I_{OL} = 1.6mA, V_{XX} = 4.5V
		—	—	0.90	V	I_{OL} = 5.0mA, V_{XX} = 4.5V
		—	—	0.90	V	I_{OL} = 5.0mA, V_{XX} = 8.0V
		—	—	1.20	V	I_{OL} = 10.0mA, V_{XX} = 8.0V
		—	—	2.0	V	I_{OL} = 20.0mA, V_{XX} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	I_{OL} = 1.6mA (Notes 5 & 6)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	−10	—	+10	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.6	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	—	mA	V_{IH} = 2.4V

NOTES:
1. Power dissipation for I/O pins is calculated by
   $\Sigma (V_{CC} - V_{IL})(|I_{IL}|) + \Sigma (V_{CC} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(I_{OL})$.
   The term I/O refers to all interface pins; input, ouput or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

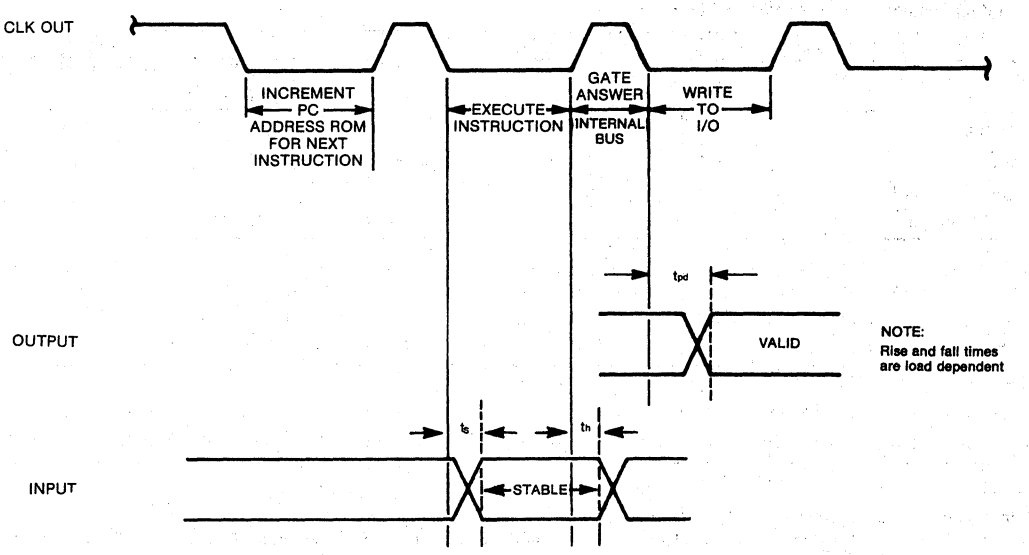
Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	—	20	μs	0.2MHz −1.0MHz external time base (Note 1)
$\overline{RTCC}$ Input						
Period	t_{RT}	t_{CY}	—	—	—	
High Pulse Width	t_{RTH}	½t_{CY}	—	—	—	
Low Pulse Width	t_{RTL}	½t_{CY}	—	—	—	(Note 2)
I/O Ports						
Data Input Setup Time	t_S	—	—	¼t_{CY}−125	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	500	800	ns	Capacitive load = 50pF
OSC Input						
External Input Impedance High	R_{OSCH}	—	120	—	Ω	V_{OSC} = 5V } Applies to external
External Input Impedance Low	R_{OSCL}	—	10^6	—	Ω	V_{OSC} = 0.4V } OSC drive only.

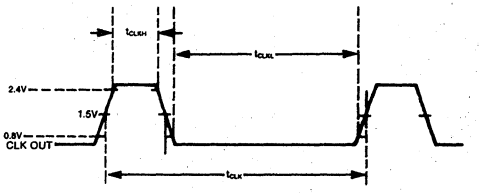
NOTES:

1. Instruction cycle period (t_{CY}) equals four times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RTCC}$ input, CLK OUT may be directly tied to the $\overline{RTCC}$ input.

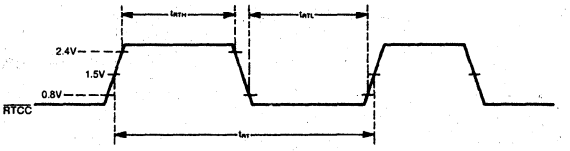
I/O TIMING



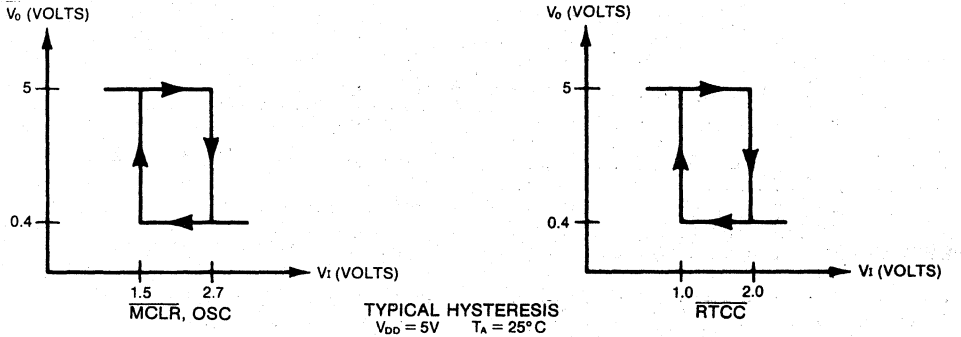
CLK OUT TIMING



RTCC TIMING



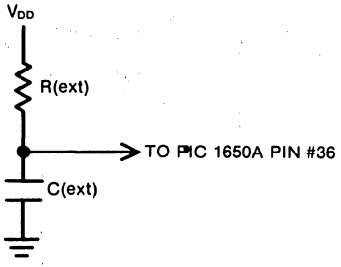
SCHMITT TRIGGER CHARACTERISTICS

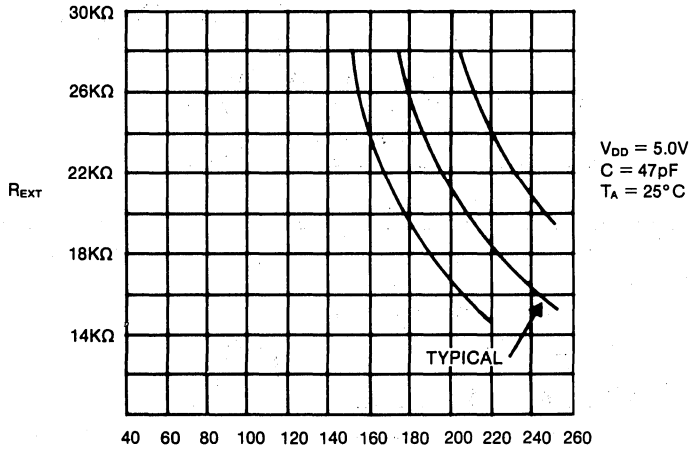


TYPICAL HYSTERESIS
V_{DD} = 5V T_A = 25°C

PIC 1650A OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

RC OPTION OPERATION

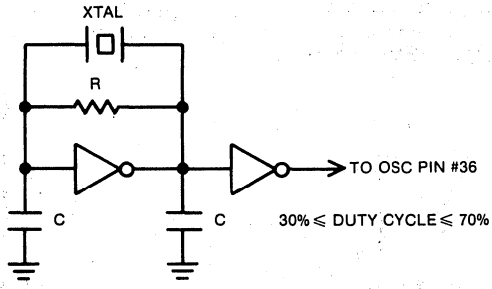




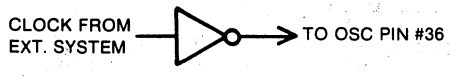
Oscillator Frequency With Typical Unit To Unit Variance

Unit to Unit Variation at V_{DD} = 5.0V, T_A = 25°C is ±25%
Variation from V_{DD} = 4.5V −7.0V referenced to 5V is −3%, +9%
Variation from T_A = 0°C −70°C referenced to 25°C is +3%, −5%

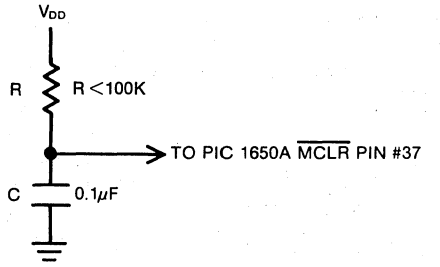
BUFFERED CRYSTAL INPUT OPERATION



EXTERNAL CLOCK INPUT OPERATION

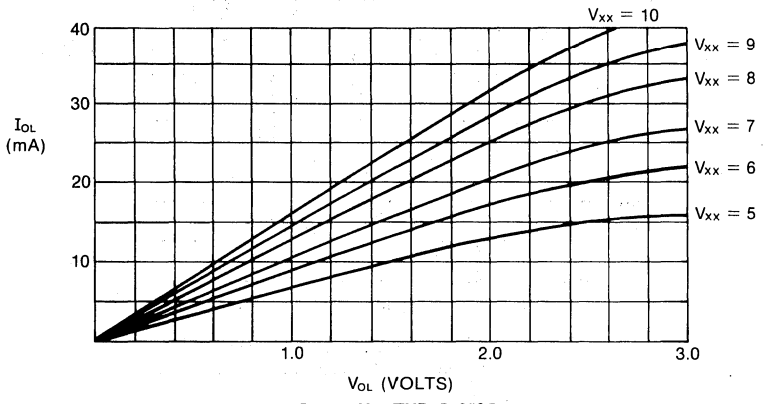


MASTER CLEAR



Master Clear requires >1.0ms delay before activation after power is applied to the V_{DD} pin. To acheive this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

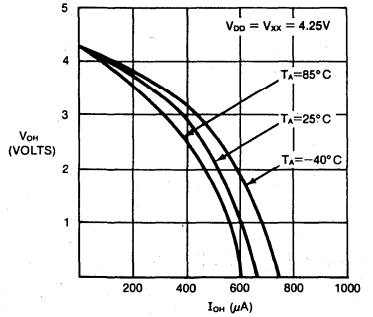
OUTPUT SINK CURRENT GRAPH



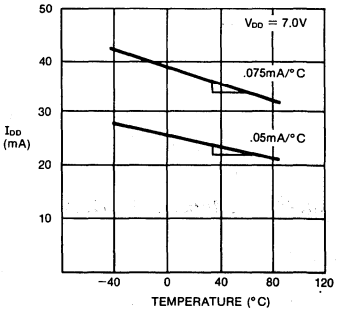
IOL vs. VOL TYP @ 25°C

The Output Sink Current is dependent on the V_{XX} supply and the output load. This chart shows the typical curves used to express the output drive capability.

VOH VS IOH (I/O PORTS)



POWER SUPPLY CURRENT VS TEMPERATURE



PIC 1650A EMULATION CAUTIONS

When emulating a PIC 1650A using a PICES development system certain precautions should be taken.

A. Be sure that the PICES Module being used is programmed for the PIC 1650A mode. (Refer to PICES Manual). The PIC 1664B contained within the module should have the MODE pin #22 set to a high state.

1. This causes the $\overline{MCLR}$ to force all I/O registers high.
2. The OSC 1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 40 pin socket for the module plug.

E. Make sure that during an actual application that the $\overline{MCLR}$ input swings from a low to high level a minimum of 1msec after the supply voltage is applied.

F. If an external oscillator drive is used, be sure that it can drive the 120Ω input impedance of the OSC pin on the PIC 1650A.

G. The cable length and internal variations may cause some parameter values to differ between the PICES module and a production PIC 1650A.

8 Bit Microcomputer

FEATURES

- User Programmable
- Intelligent Controller for Stand-Alone Applications
- 32 8-bit RAM Registers
- 512 x 12-bit Program ROM
- Arithmetic Logic Unit
- Real Time Clock Counter
- Self-contained Oscillator
- Access to RAM Registers inherent in instruction
- Wide Power Supply Operating Range (4.5V to 7.0V)
- Available in two temperature ranges: 0° to 70° C and −40° C to 85° C
- 4 inputs, 8 outputs, 8 bi-directional I/O lines
- 2 Level Stack

DESCRIPTION

The PIC 1655A microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit ALU.

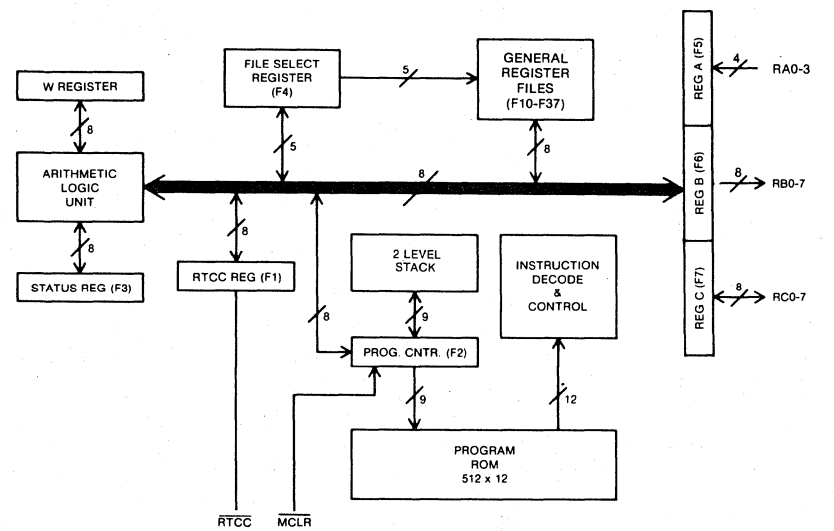
The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC 1655A is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or buffered crystal oscillator signal, for greater accuracy) to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC 1664B. The PIC 1664B is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD 1000 Field Demo System is available containing a PIC 1664B with sockets for erasable CMOS PROMs. Finally, the PICES (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

PIC 1655A BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The primary purpose of the PIC is to perform logical processing, basic code conversions, formatting, and to generate fundamental timing and control signals for I/O devices. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

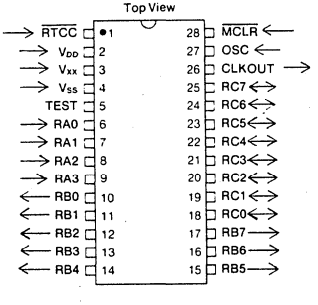
The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the $\overline{MCLR}$ input on power up initializes the ROM program to address 777_8.

PIN FUNCTIONS

Signal	Function
OSC (input)	Oscillator input: This signal can be driven by an external oscillator if a precise frequency of operation is required or an external RC network can be used to set the frequency of operation of the internal clock generator. This is a Schmitt trigger input.
$\overline{RTCC}$ (input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The Real Time Clock Counter Register increments on falling edges applied to this pin. This register can be loaded and read by the program. This is a Schmitt trigger input.
RA0-3 (input)	4 input lines
RB0-7 (output)	8 output lines
RC0-7 (input/output)	8 user programmable input/ouput lines All inputs and outputs are under direct control of the program.
$\overline{MCLR}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch all I/O register high. Should be held low at least 1ms past the time when the power supply is valid. This is a Schmitt trigger input.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
TEST	Used for testing purposes only. Must be grounded for normal operation.
V_{DD}	Primary power supply.
V_{XX}	Output Buffer power supply. Used to enhance output current sinking capability.
V_{SS}	Ground

PIN CONFIGURATION
28 LEAD DUAL IN LINE



REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{\text{RTCC}}$.
F2	Program Counter (PC).The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2).The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	1	1	1	Z	DC	C

C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.

DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

Z (Zero): Set if the result of an arithmetic operation is zero.

Bits: 3-7 These bits are defined as logic ones.

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	Input Register A (A0-A3) (A4-A7 defined as zeroes)
F6	Output Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10-F37	General Purpose Registers

Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1MHz the instruction execution time is 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec.

BYTE-ORIENTED FILE REGISTER OPERATIONS

(11-6)	(5)	(4-0)
OP CODE	d	f (FILE #)

For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	$\bar{f}$→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\bar{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1),f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇋f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS

(11-8)	(7-5)	(4-0)
OP CODE	b (BIT #)	f (FILE #)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS

(11-8)	(7-0)
OP CODE	k (LITERAL)

Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	k∨W→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

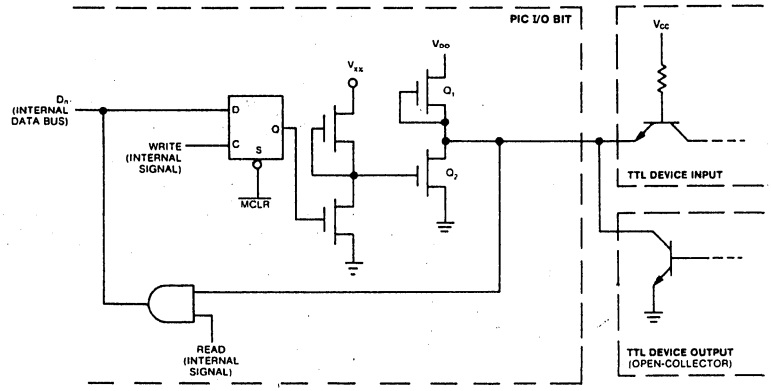
The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Programming Cautions

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation.

Bidirectional I/O Ports

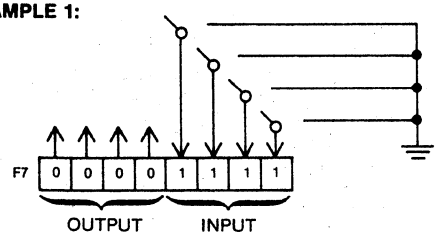
The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the intput/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:



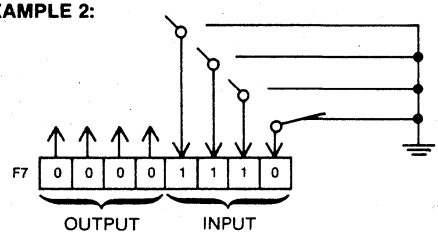
What is thought to be happening:

BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low:

BSF 7,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias
Storage Temperature ..... −55°C to +150°C
Voltage on any pin with Respect to V_{SS} ..... −0.3V to +12.0V
Power Dissipation 1000mW
Power Dissipated by any one I/O pin (Note 1) 60mW
Power Dissipated by all I/O pins (Note 1) 600mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	55	mA	No Load
Output Buffer Supply Current	I_{XX}	—	1	5	mA	No Load (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$ & OSC when driven externally)	V_{IH1}	2.4	—	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$ & OSC)	V_{IH2}	V_{DD}−1	—	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	—	V_{DD}	V	I_{OH} = −100μA provided by internal pullups (Note 4)
Output Low Voltage (I/O only)	V_{OL1}	—	—	0.45	V	I_{OL} = 1.6mA, V_{XX} = 4.5V
		—	—	0.90	V	I_{OL} = 5.0mA, V_{XX} = 4.5V
		—	—	0.90	V	I_{OL} = 5.0mA, V_{XX} = 8.0V
		—	—	1.20	V	I_{OL} = 10.0mA, V_{XX} = 8.0V
		—	—	2.0	V	I_{OL} = 20.0mA, V_{XX} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	I_{OL} = 1.6mA (Notes 5 & 6)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$)	I_{LC}	−10	—	+10	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.6	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	—	mA	V_{IH} = 2.4V

NOTES:
1. Power dissipation for I/O pins is calculated by
   $\Sigma (V_{CC} - V_{IL}) (|I_{IL}|) + \Sigma (V_{CC} - V_{OH}) (|I_{OH}|) + \Sigma (V_{OL}) (I_{OL})$.
   The term I/O refers to all interface pins; input, ouput or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

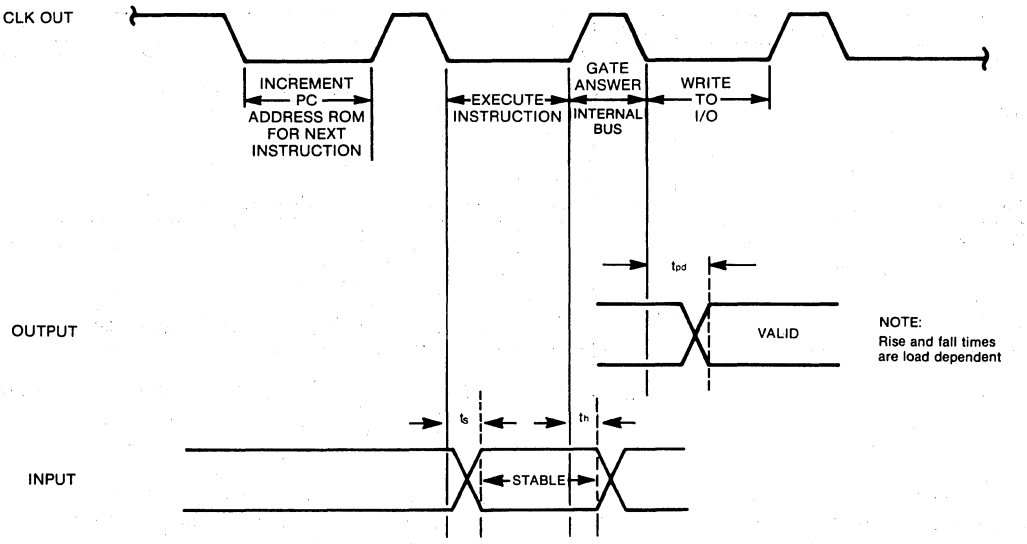
Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{cy}	4	—	20	μs	0.2MHz −1.0MHz external time base (Note 1)
$\overline{RTCC}$ Input						
Period	t_{RT}	t_{cy}	—	—	—	
High Pulse Width	t_{RTH}	½t_{cy}	—	—	—	
Low Pulse Width	t_{RTL}	½t_{cy}	—	—	—	(Note 2)
I/O Ports						
Data Input Setup Time	t_S	—	—	¼t_{cy}−125	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	500	800	ns	Capacitive load = 50pF
OSC Input						
External Input Impedance High	R_{OSCH}	—	120	—	Ω	V_{osc} = 5V } Applies to external
External Input Impedance Low	R_{OSCL}	—	10^6	—	Ω	V_{osc} = 0.4V } OSC drive only.

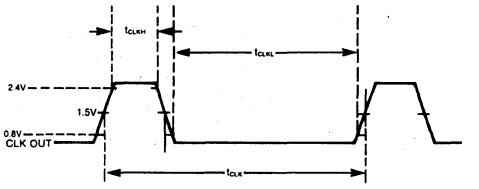
NOTES:

1. Instruction cycle period (t_{cy}) equals four times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RTCC}$ input, CLK OUT may be directly tied to the $\overline{RTCC}$ input.

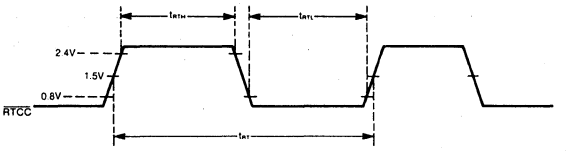
I/O TIMING



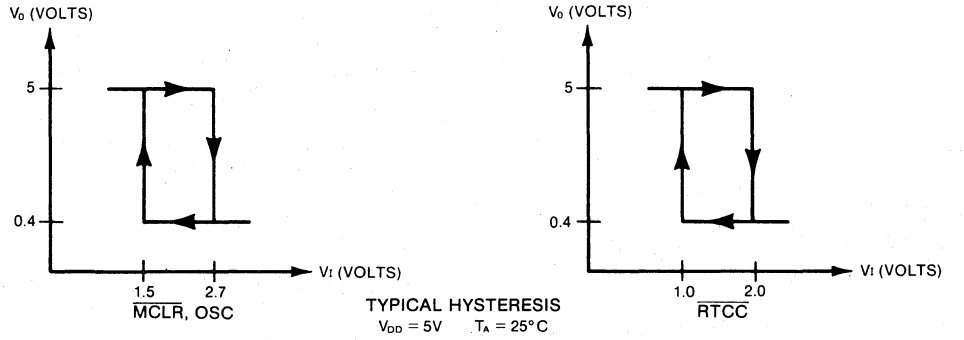
CLK OUT TIMING



$\overline{\text{RTCC}}$ TIMING

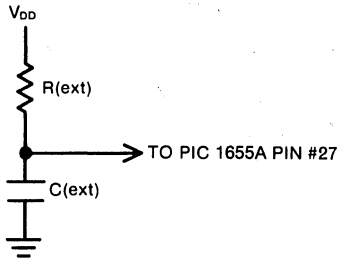


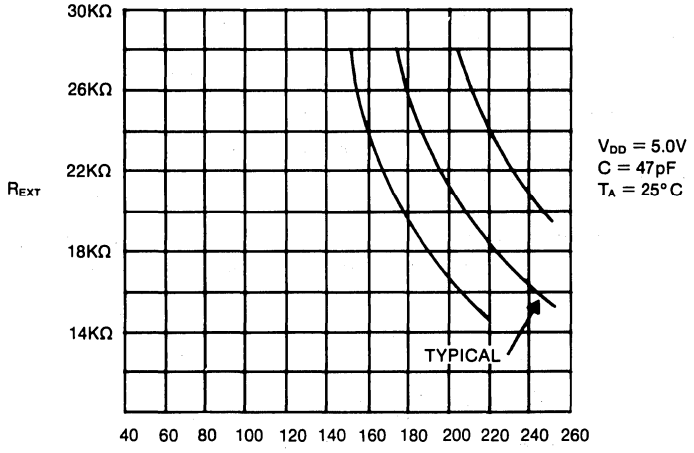
SCHMITT TRIGGER CHARACTERISTICS



PIC 1655A OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

RC OPTION OPERATION

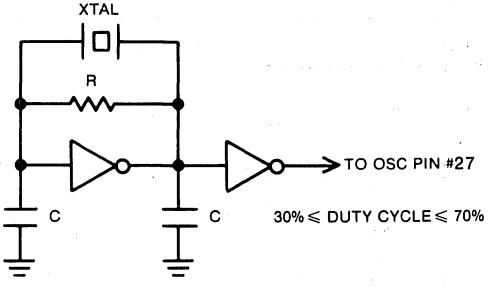




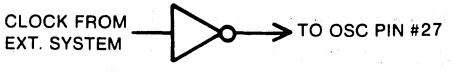
Oscillator Frequency With Typical Unit To Unit Variance

Unit to Unit Variation at V_{DD} = 5.0V, T_A = 25°C is ±25%
Variation from V_{DD} = 4.5V −7.0V referenced to 5V is −3%, +9%
Variation from T_A = 0°C −70°C referenced to 25°C is +3%, −5%

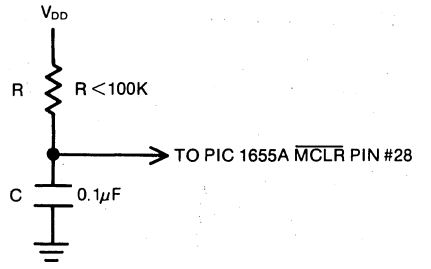
BUFFERED CRYSTAL INPUT OPERATION



EXTERNAL CLOCK INPUT OPERATION

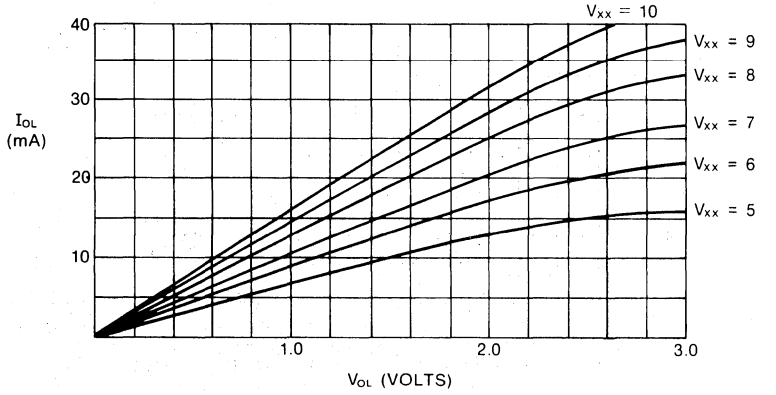


MASTER CLEAR



Master Clear requires >1.0ms delay before activation after power is applied to the V_{DD} pin. To acheive this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

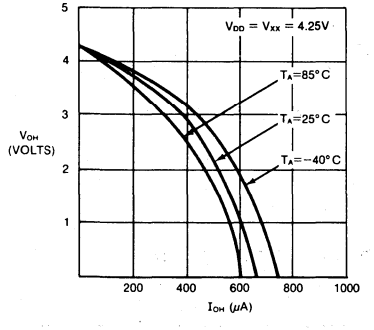
OUTPUT SINK CURRENT GRAPH



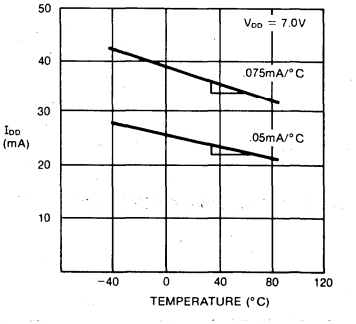
I_{OL} vs. V_{OL} TYP @ 25°C

The Output Sink Current is dependent on the V_{xx} supply and the output load. This chart shows the typical curves used to express the output drive capability.

V_{OH} VS I_{OH} (I/O PORTS)



POWER SUPPLY CURRENT VS TEMPERATURE



PIC 1655A EMULATION CAUTIONS

When emulating a PIC 1655A using a PICES development system certain precautions should be taken.

A. Be sure that the PICES Module being used is programmed for the PIC 1650A mode. (Refer to PICES Manual). The PIC 1664B contained within the module should have the MODE pin #22 set to a high state.

1. This causes the $\overline{MCLR}$ to force all I/O registers high.
2. The OSC 1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 28 pin socket for the module plug.

E. Make sure that during an actual application that the $\overline{MCLR}$ input swings from a low to high level a minimum of 1msec after the supply voltage is applied.

F. If an oscillator drive is used, be sure that it can drive the 120Ω input impedance of the OSC pin on the PIC 1655A.

G. The cable length and internal variations may cause some parameter values to differ between the PICES module and a production PIC 1655A.

8 Bit Microcomputer

FEATURES

- Vectored interrupt servicing capability
- User Programmable
- Intelligent Controller for Stand-Alone Applications
- 32 8-bit RAM Registers
- 512 x 12-bit Program ROM
- Arithmetic Logic Unit
- Real Time Clock Counter
- Event counter capability
- Self-contained Oscillator for RC network or Crystal
- Access to RAM Registers inherent in instruction
- Wide Power Supply Operating Range (4.5V to 7.0V)
- Available in two temperature ranges: 0° to 70°C and −40°C to 85°C
- 4 inputs, 8 outputs, 8 bidirectional I/O lines
- 3 Level Stack
- Same PIC instruction set as PIC 1650A or PIC 1655A with the addition of Return (0002_8) instruction

DESCRIPTION

The PIC 1656 microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit as well as customer-defined ROM on a single chip. This combination produces a low cost solution for applications which require sensing individual inputs and controlling individual outputs. Keyboard scanning, display driving, and other system control functions can be done at the same time due to the power of the 8-bit ALU.

The PIC 1656 is designed for real-time control applications requiring external and internal clock-driven interrupts. The PIC 1656 has 20 I/O lines organized as two 8-bit registers and the 4 LSB's of a third register.

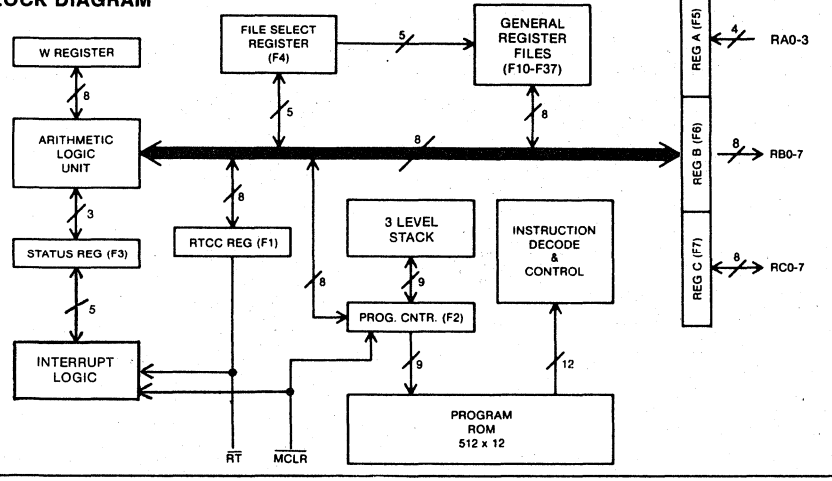
The internal ROM contains a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications. The PIC can be used to scan keyboards, drive displays, control electronic games and provide enhanced capabilities to vending machines, traffic lights, radios, television, consumer appliances, industrial timing and control applications. The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic operations using bytes.

The PIC 1656 is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or buffered crystal oscillator signal, for greater accuracy) to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing an application program and to verify performance before committing to mask tooling. Programs can be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PIC's operation can be verified in any hardware application by using the PIC 1664B. The PIC 1664B is a ROM-less PIC microcomputer with additional pins to connect external PROM or RAM and to accept HALT commands. The PFD 1010 Field Demo System is available containing a PIC 1664B with sockets for erasable CMOS PROMs. Finally, the PICES (PIC In-Circuit Emulation System) provides the user with emulation and debugging capability in either a stand-alone mode or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM. With these development tools, the user can quickly and confidently order the masking of the PIC's ROM and bring his application into the market.

A PIC Series Microcomputer Data Manual is available which gives additional detailed data on PIC based system design.

PIC 1656 BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC series microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The primary purpose of the PIC is to perform logical processing, basic code conversions, formatting, and to generate fundamental timing and control signals for I/O devices. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined Program ROM composed of 512 words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general registers. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

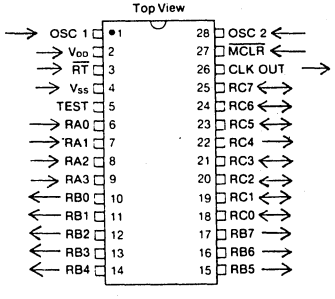
The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Program ROM contains the operational program for the rest of the logic within the controller. Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip two-level stack is employed to provide easy to use subroutine nesting. Activating the $\overline{\text{MCLR}}$ input on power up initializes the ROM program to address 777_8.

PIN FUNCTIONS

Signal	Function
OSC 1, OSC 2 (input)	Oscillator inputs. The oscillator freuqnecy can be set by a crystal (if a precise frequency is required) or by an external RC network.
$\overline{\text{RT}}$ (input)	Real-Time Input. Function is controlled by bits 4 and 7 of the Status Word Register (F3). A high-to-low transition of this pin will increment the RT register (event counter mode) or will inititate a vectored interrupt (external interrupt mode).
RA0-3 (input)	Dedicated input lines, read under direct control of the program. The 4 MSB's are always read as logic zeroes.
RB0-7 (output)	Dedicated output lines, user programmable under direct control of the program.
RC0-7 (input/output)	User programmable input/output lines. These lines can be inputs and/or outputs and are under direct control of the program.
$\overline{\text{MCLR}}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and latch I/O registers F6 and F7 low. Also clears bits 3-7 of status register (F3). Should be held low at least 1ms past the time when the power supply is valid.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.
TEST	Used for testing purposes only. Must be grounded for normal operation.
V_{DD}	Primary Power Supply.
V_{SS}	GND.

PIN CONFIGURATION
28 LEAD DUAL IN LINE



REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The $\overline{RTCC}$ register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$.
F2	Program Counter (PC).The PC is automatically incremented during each instruction cycle, and can be written into under program control (MOVWF F2).The PC is nine bits wide, but only its low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.
F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	Input Register A (A0-A3) (A4-A7) defined as zeroes
F6	Output Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10-F37	General Purpose Registers

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
CNT	RTCR	IR	RTCE	IE	Z	DC	C

C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.

DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

Z (Zero): Set if the result of an arithmetic operation is zero.

Bits: 3-7 Interrupt Service Flags (Cleared on $\overline{MCLR}$.)
Bit 3: IE (external Interrupt Enable) bit
Bit 4: RTCE (Real Time CLock Enable) bit
Bit 5: IR (external Interrupt Request) bit
Bit 6: RTCR (Real Time CLock interrupt Request) bit
Bit 7: CNT (Count) bit (selects input to $\overline{RTCC}$)

PIC 1656 INTERRUPT SYSTEM

The interrupt system of the PIC 1656 is comprised of an external interrupt and an internal real-time clock/counter interrupt. These have different interrupt vectors, enable bits, and status bits. Both interrupts are controlled by the Status Word Register F3, shown below:

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
CNT	RTCR	IR	RTCE	IE	Z	DC	C

(NOTE: F3 bits 3-7 are cleared on $\overline{MCLR}$.)

The first high to low transition of the $\overline{RT}$ pin will set F3, bit 5 (IR, Interrupt Request) to a one. [The external interrupt is enabled by F3, bit 3 (IE, Interrupt Enable).] If the interrupt is enabled (IE is a one), or as soon as it is, during the next two instruction cycles the processor will push the current Program Counter contents onto the stack and execute the instruction at location 760_8. The IR bit is immediately cleared. Note that although the processor cannot be interrupted again until a return from interrupt (RETURN) instruction is executed, an additional interrupt request can be generated by another high to low transition of the $\overline{RT}$ pin, setting IR high again. If this is done, the processor will reinterrupt right after the return from the preceeding interrupt (assuming IE is a one).

The Real Time Clock/Counter (RTCC, File Register 1) has a similar mechanism of interrupt service. The clocking source for the RTCC is selected by bit 7 (CNT, Count Select) of the Status register. If CNT is set to a one, the RTCC will increment on each high to low transition of the $\overline{RT}$ pin. If CNT is cleared to a "zero", the RTCC will count at the internal instruction clock rate, 1/16 the frequency present on the OSC pins. When the RTCC transitions from 377_8 to 0, an interrupt request will be generated (RTCR is set to a one). If RTCE is a one, or as soon as it is set to a one, an interrupt will be generated. That is, the present contents of the Program Counter is stored on the stack and the instruction at location 740_8 is executed.

The RETURN instruction (0002_8) must be used to return from any interrupt service routine as it re-enables interrupts to allow pending or future interrupts to be generated. External interrupts have priority over RTCC driven interrupts in the event that both occur simultaneously (and both are enabled). Interrupts cannot be nested but will be serviced sequentially. The existence of any pending interrupts can be tested via the state of the IR and RTCR bits in the Status Word Register, and enabled or disabled as if desired.

A summary of the PIC 1656 Interrupt Logic is as follows:

Status Register Bits					
7 CNT	6 RTCR	5 IR	4 RTCE	3 IE	Interrupt Logic
0	0	0	0	X	The first high-to-low transition at the $\overline{RT}$ pin causes IR bit 5 to set to a one.
0	0	1	0	1	IE and IR both set to ones enables the PIC to interrupt to 760_8. IR (bit 5) then immediately resets to a zero.
0	X	X	X	X	The RTCC register is enabled to increment at the internal clock rate. When the contents of the RTCC register transition from 377_8 to 000_8, RTCR (bit 6) is set to a one.
1	X	X	X	X	The RTCC register is enabled to increment at the rate of the input at the $\overline{RT}$ pin (event timer mode). When the contents of the RTCC register transition from 377_8 to 000_8, RTCC (bit 6) is set to a one.
X	1	0	1	0	Both RTCE and RTCR set to ones enables the PIC to interrupt to 740_8. RTCR (bit 6) then immediately resets to a zero.
0	0	0	X	X	Regardless of the states of IE and RTCE, an interrupt on the $\overline{RT}$ pin and/or an RTCC transition from a full count to a zero count will set the IR bit and/or the RTCR bit to one(s).
X	1	0	1	1	If the IR bit is set to a zero at the time that the RTCR bit is set to a one, the PIC will interrupt to 740_8 (RTCC interrupt mode). The RTCR bit then immediately resets to a zero.
X	0	1	1	1	If the RTCR bit is set to a zero at the time that the IR bit is set to a one, the PIC will interrupt to 760_8 (external interrupt mode). The IR bit then immediately resets to a zero.
X	1	1	1	1	If the IR bit and the RTCR bit are each set to ones at the same time, the PIC will first interrupt to 760_8 (external interrupt mode). The IR bit then immediately resets to a zero. If the IR bits remains at a zero (indicating that no other external interrupts have occurred in the meantime), the PIC will then interrupt to 740_8 (RTCC interrupt mode) immediately after a RETFI instruction is executed. The RTCR bit then immediately resets to a zero.

X = DON'T CARE

Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

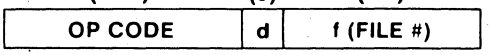
For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 4MHz the instruction execution time as 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction, In these two cases, the insruction execution time is 8 μsec.

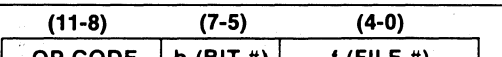
BYTE-ORIENTED FILE REGISTER OPERATIONS



For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

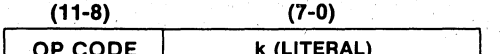
Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	WVf→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\bar{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1),f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇆f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 010 (0002)	Return from Interrupt	RETURN	—	Stack→PC	None
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	kVW→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

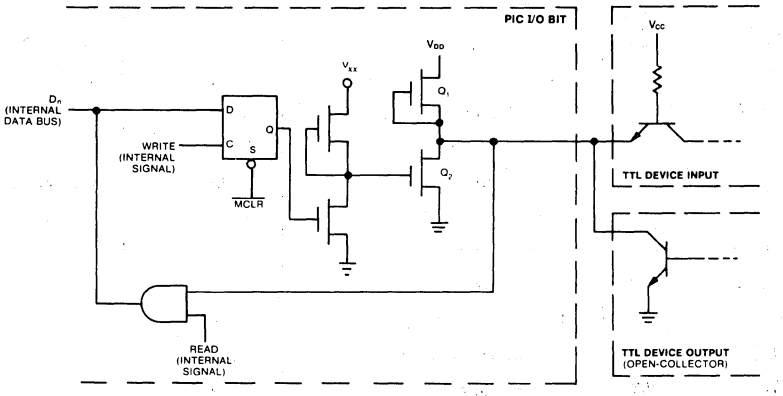
The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Programming Cautions

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation.

Bidirectional I/O Ports

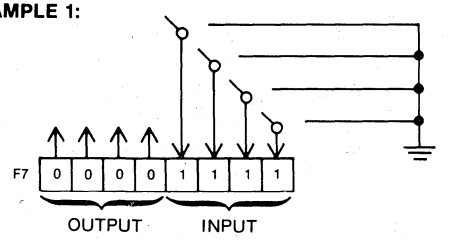
The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the intput/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:



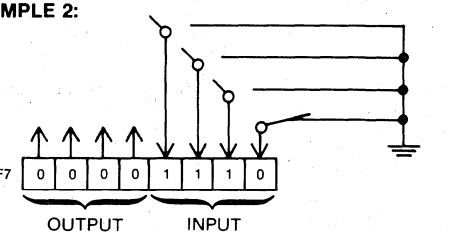
What is thought to be happening:

BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low:

BSF 7,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any pin with Respect to V_{SS} ..... −0.3V to +12.0V
Power Dissipation 1000mW
Power Dissipated by any one I/O pin (Note 1) 60mW
Power Dissipated by all I/O pins (Note 1) 600mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	55	mA	No Load
Output Buffer Supply Current	I_{XX}	—	1	5	mA	No Load (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RT}$ & OSC when driven externally)	V_{IH1}	2.4	—	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RT}$ & OSC)	V_{IH2}	V_{DD}−1	—	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	—	V_{DD}	V	I_{OH} = −100μA provided by internal pullups (Note 4)
Output Low Voltage (I/O only)	V_{OL1}	—	—	0.45	V	I_{OL} = 1.6mA, V_{XX} = 4.5V
		—	—	0.90	V	I_{OL} = 5.0mA, V_{XX} = 4.5V
		—	—	0.90	V	I_{OL} = 5.0mA, V_{XX} = 8.0V
		—	—	1.20	V	I_{OL} = 10.0mA, V_{XX} = 8.0V
		—	—	2.0	V	I_{OL} = 20.0mA, V_{XX} = 8.0V (Note 5)
Output Low Voltage (CLK OUT)	V_{OL2}	—	—	0.45	V	I_{OL} = 1.6mA (Notes 5 & 6)
Input Leakage Current ($\overline{MCLR}$, $\overline{RT}$, OSC 1)	I_{LC}	−10	—	+10	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.6	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH}	−0.1	−0.4	—	mA	V_{IH} = 2.4V

NOTES:
1. Power dissipation for I/O pins is calculated by
   $\Sigma (V_{CC} - V_{IL}) (|I_{IL}|) + \Sigma (V_{CC} - V_{OH}) (|I_{OH}|) + \Sigma (V_{OL}) (I_{OL})$.
   The term I/O refers to all interface pins; Input, Output or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

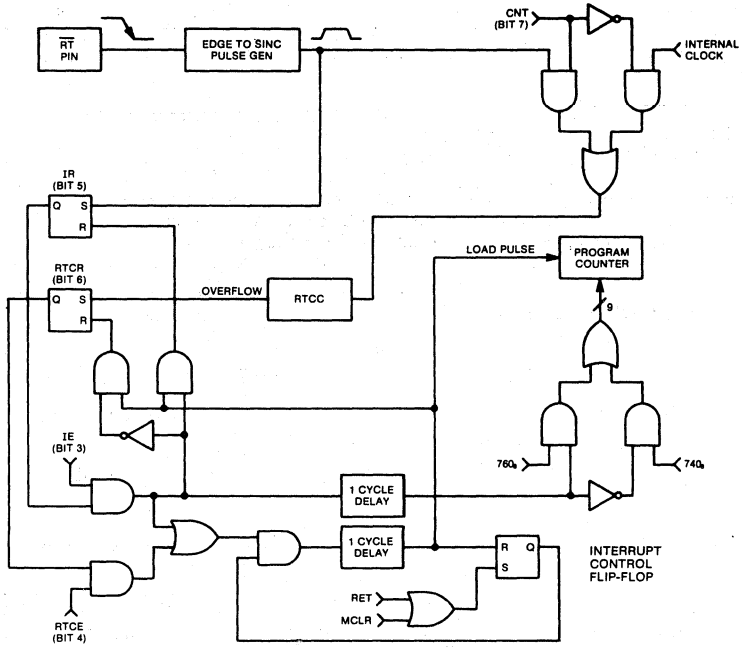
Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{cy}	4	—	20	μs	0.8MHz—4.0MHz external time base (Note 1)
$\overline{RT}$ Input						
Period	t_{RT}	t_{cy}	—	—	—	
High Pulse Width	t_{RTH}	½t_{cy}	—	—	—	
Low Pulse Width	t_{RTL}	½t_{cy}	—	—	—	(Note 2)
I/O Ports						
Data Input Setup Time	t_s	—	—	¼t_{cy}−125	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	500	800	ns	Capacitive load = 50pF
OSC Input						
External Input Impedance High	R_{OSCH}	—	10^6	—	Ω	V_{OSC} = 5V } Applies to external
External Input Impedance Low	R_{OSCL}	—	10^6	—	Ω	V_{OSC} = 0.4V } OSC drive only.

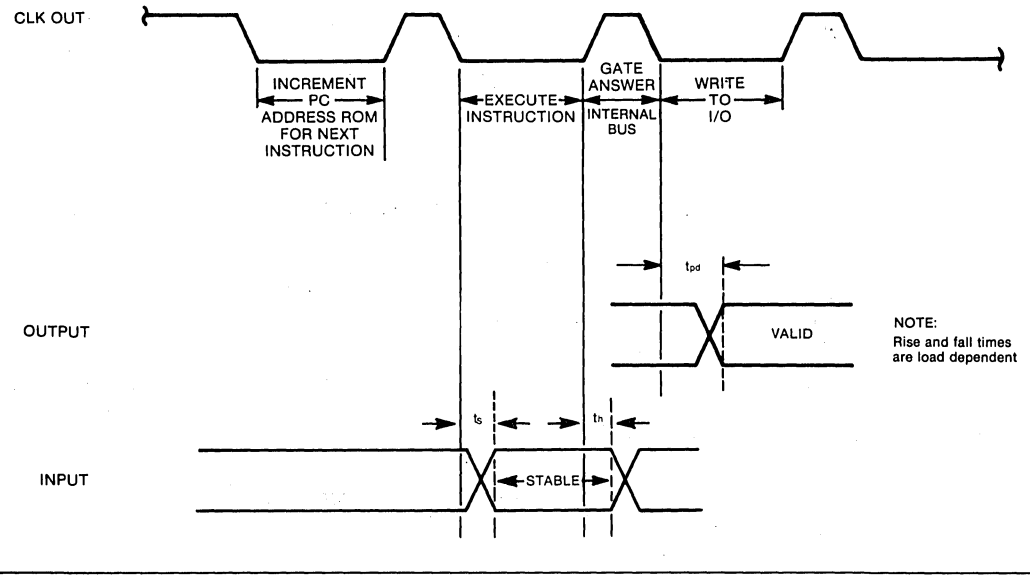
NOTES:

1. Instruction cycle period (t_{CY}) equals four times the input oscillator time base period.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the $\overline{RT}$ input, CLK OUT may be directly tied to the $\overline{RT}$ input.

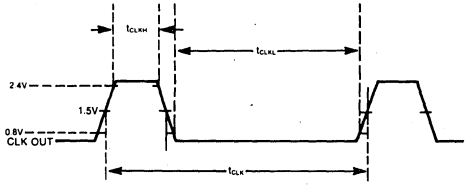
INTERRUPT SYSTEM BLOCK DIAGRAM



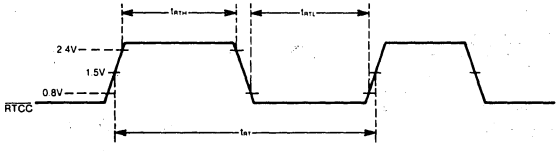
I/O TIMING



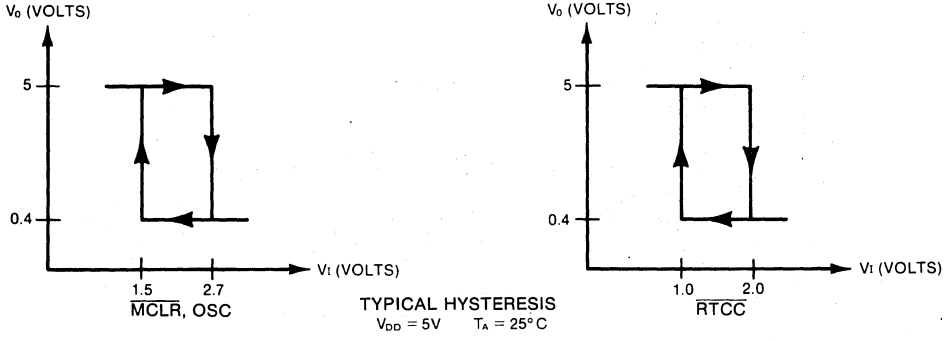
CLK OUT TIMING



RTCC TIMING

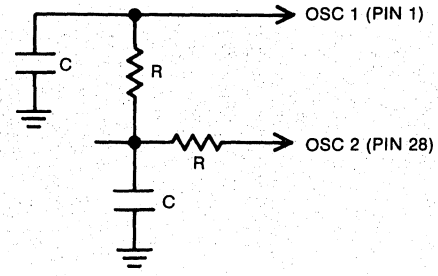


SCHMITT TRIGGER CHARACTERISTICS

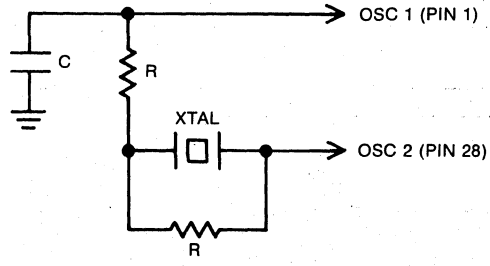


PIC 1656 OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

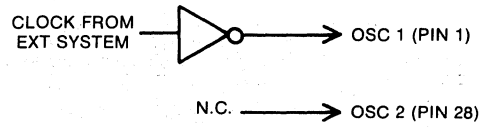
RC OPTION OPERATION



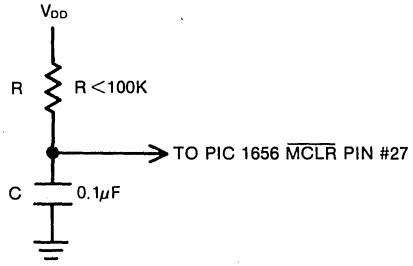
CRYSTAL INPUT OPERATION



EXTERNAL CLOCK INPUT OPERATION

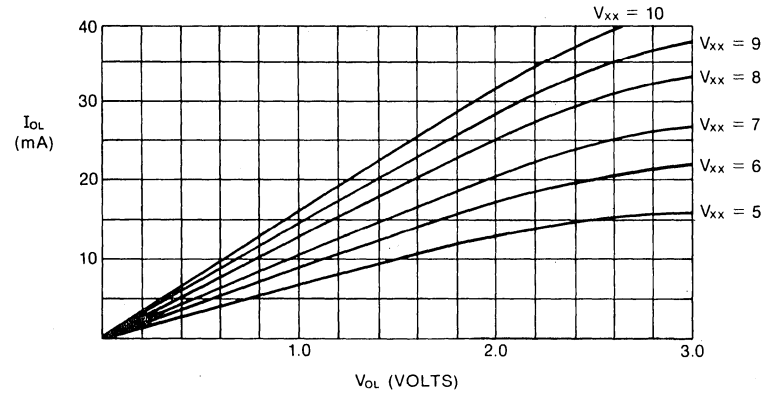


MASTER CLEAR



Master Clear requires >1.0ms delay before activation after power is applied to the V_{DD} pin. To acheive this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

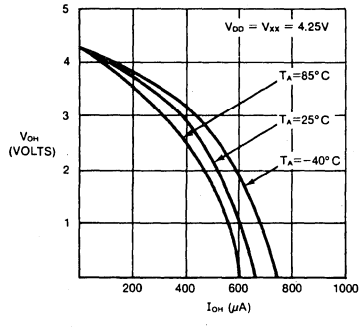
OUTPUT SINK CURRENT GRAPH



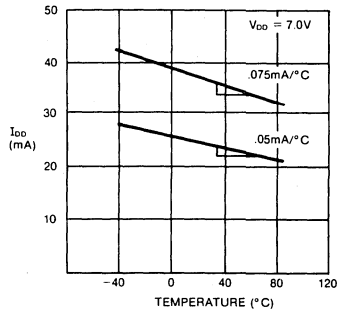
IOL vs. VOL TYP @ 25°C

The Output Sink Current is dependent on the V_{XX} supply and the output load. This chart shows the typical curves used to express the output drive capability.

VOH VS IOH (I/O PORTS)



POWER SUPPLY CURRENT VS TEMPERATURE



PIC 1656 EMULATION CAUTIONS

When emulating a PIC 1656 using a PICES development system certain precautions should be taken.

A. Be sure that the PICES Module being used is programmed for the PIC 1656 mode. (Refer to PICES Manual). The PIC 1664B contained within the module should have the MODE pin #22 set to a low state.

1. This causes the $\overline{\text{MCLR}}$ to register F5 high and register F6, and F7 low.
2. The OSC becomes a two input clock (pins 1 & 28).
3. The interrupt system becomes enabled and the RT always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are used for interrupt service.

B. Three levels of stack can be used within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 28 pin socket for the module plug.

E. Make sure that during an actual application that the MCLR input swings from a low to high level a minimum of 1msec after the supply voltage is applied.

F. If an external oscillator drive is used, be sure that it can drive the 120Ω input impedance of the OSC pins on the PIC 1656.

G. The cable length and internal variations may cause some parameter values to differ between the PICES module and a production PIC 1656.

8 Bit Development Microcomputer

FEATURES

- PIC microcomputer with ROM removed
- Useful for engineering prototyping of PIC applications
- PIC ROM address & data lines brought out to pins
- HALT pin for single stepping or stopping program execution
- MODE pin for selection of PIC 1650A/1655A or PIC 1656 emulation
- User Programmable via external Memory
- 32 8-bit RAM Registers
- Arithmetic Logic Unit
- User Defined TTL-compatible Input and Output Lines
- Real Time Clock Counter
- Self-Contained Oscillator
- Access to RAM Registers inherent in instruction
- Wide Power Supply Operating Range (4.5V to 7.0V)

DESCRIPTION

The PIC 1664B development microcomputer is an MOS/LSI device containing RAM, I/O, and a central processing unit on a single chip.

The PIC 1664B MOS/LSI device is functionally identical to the PIC microcomputers except that the ROM is removed and the ROM address and data lines are brought out, requiring a 64-pin package. The addition of a HALT pin gives the user the ability to stop as well as single-step the chip. The logic level applied to a MODE pin determines whether the PIC 1664B emulates a PIC 1650A/1655A or a PIC 1656.

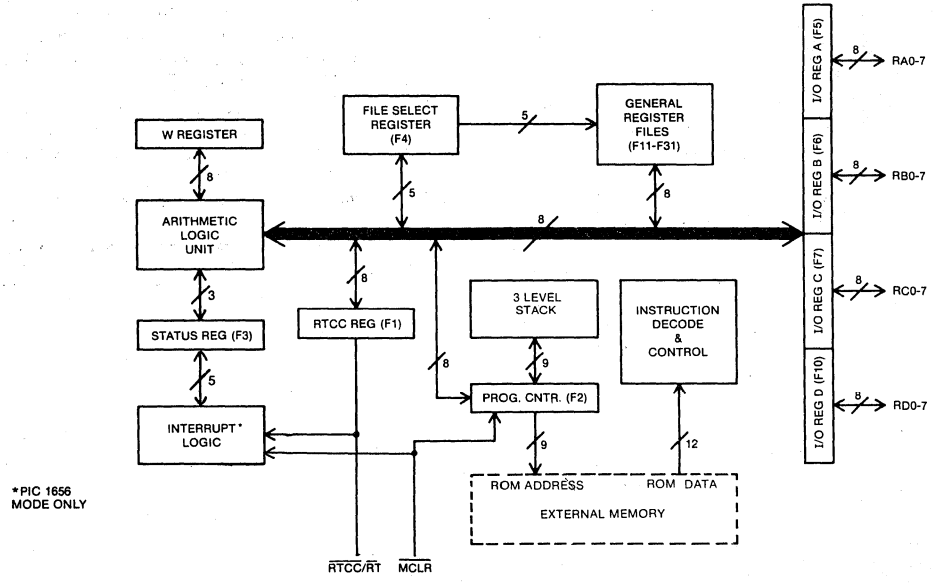
The external ROM can contain a customer-defined program using the PIC's powerful instruction set to specify the overall functional characteristics of the device. The 8-bit input/output registers provide latched lines for interfacing to a limitless variety of applications.

The 12-bit instruction word format provides a powerful yet easy to use instruction repertoire emphasizing single bit manipulation as well as logical and arithmetic oeprations using bytes.

The PIC Series is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and production history. Only a single wide range power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external RC network (or buffered crystal oscillator signal, for greater accuracy) to establish the frequency. Inputs and outputs are TTL-compatible.

Extensive hardware and software support is available to aid the user in developing this application program and to verify performance before committing to mask tooling. Application notes and sample programs are used to develop programs which can then be assembled into machine language using PICAL, eliminating the burden of coding with ones and zeros. PICAL is available in a Fortran IV version that can be run on many popular computer systems. Once the application program is developed several options are available to insure proper performance. The PFD Field Demo Systems are available containing a PIC 1664B with sockets for erasable CMOS PROMs. Finally, the PICES (PIC In-Circuit Emulation System) provides the user with stand-alone emulation and debugging operation or operation as a peripheral to a larger computer system. Easy program debugging and changing is facilitated because the user's program is stored in RAM.

PIC 1664B GENERAL BLOCK DIAGRAM



ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC 1664B microcomputer is based on a register file concept with simple yet powerful commands designed to emphasize bit, byte, and register transfer operations. The primary purpose of the PIC is to perform logical processing, basic code conversions, formatting, and to generate fundamental timing and control signals for I/O devices. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC 1664B is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a user-defined external ROM composed of 512 program words each 12 bits in width. The Register File is divided into two functional groups: operational registers and general register. The operational registers include, among others, the Real Time Clock Counter Register, the Program Counter (PC), the Status Register, and the I/O Registers. The general purpose registers are used for data and control information under command of the instructions.

The Arithmetic Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

Sequencing of microinstructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions, Jump instructions, Call instructions, or by loading computed addresses into the PC. In addition, an on-chip three-level stack is employed to provide easy to use subroutine nesting. Activating the MCLR input on power up initializes the external ROM program to address 777_8.

PIN FUNCTIONS

Signal	Function
MODE (input)	Mode input. Used to set the PIC 1664B to emulate the PIC 1650A/PIC 1655A (logic "one") or the PIC 1656 (logic "zero"). The mode must be selected before $\overline{MCLR}$ is brought high.
OSC 1, OSC 2 (input)	Oscillator inputs. When the MODE switch selects PIC 1650A/1655A operation OSC 1 becomes a single input clock using either RC control or a buffered crystal. When the PIC 1664B is in the PIC 1656 mode both OSC 1 and OSC 2 are used as a two input clock using either crystal, ceramic resonator or RC network.
$\overline{RT}$ (input)	Real Time input. This pin increments the Real Time Clock Counter Register 1 on high to low transitions appied to this input. This pin has different modes of operation depending on the MODE input as well as the contents of F3, the Status Register. In PIC 1650A/1655A mode this pin emulates the $\overline{RTCC}$ pin. In the PIC 1656 mode this pin emulates the $\overline{RT}$ pin.
RA0-7, RB0-7, RC0-7, RD0-7 (input/output)	User programmable input/output lines. These lines can be inputs and/or outputs and are under direct control of the program. During emulation of the PIC 1655A or PIC 1656, Register D will become internal general purpose File Register 10; I/O lines RD0-7 will be undefined and must be left unconnected.
$\overline{MCLR}$ (input)	Master Clear. Used to initialize the internal ROM program to address 777_8 and to latch all I/O registers high (for PIC 1650A/1655A) or I/O registers F6 and F7 low and F5 high (for PIC 1656). Also clears bits 3-7 of status register (F3) (for PIC 1656). This pin should be held low at least 1ms after the power supply is valid. $\overline{MCLR}$ has no internal pullup resistor.
V_{DD}	Primary Power supply input.
V_{XX}	Output buffer power supply input. Used to increase current sinking capability when emulating the PIC 1650A and PIC 1655A. When emulating the PIC 1656 this pin must be connected to V_{DD}.
CLK OUT (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing. The OSC frequency is divided by 4 for PIC 1650A/1655A mode or by 16 for the PIC 1656 mode.
HALT (input)	Halt. When high this input suspends execution of the next instruction. No data is lost and after HALT is brought low execution proceeds exactly as if no HALT signal had been applied.
HALT ACK (output)	Halt Acknowledge. This output is high when the PIC 1664B is halted either due to an active HALT input or execution of the HALT instruction (0001_8). In the first case HALT ACK is brought back low when the PIC 1664B begins execution when the HALT input is brought low; and in the second case it is brought low using $\overline{MCLR}$ or by first raising and then lowering the HALT input.
D0-D11 (input)	Data Input. These twelve lines accept twelve bit PIC instruction codes generated by an external source D0 is the LSB of the instruction.
A0-A8 (output)	Address Output. These nine lines represent the address of the next instruction to be executed by the PIC 1664B. A0 is the LSB of the address.

MODE PIN OPERATION

The mode pin is used to select either PIC 1650A/1655A emulation or PIC 1656 emulation.

With the MODE pin set high, the PIC 1664B is set to emulate the PIC 1650A/1655A. Specifically:

1. $\overline{MCLR}$ will force all I/O registers high.
2. OSC 1 becomes a single clock input. The PIC 1664B will execute instructions at one fourth the OSC frequency.
3. The interrupt system is disabled and the RTCC always counts on trailing edges.
4. Bits 3-7 of F3 are ones.

When the MODE input is low, the PIC 1664B will emulate the PIC 1656 circuit. Specifically:

1. $\overline{MCLR}$ will force I/O registers F6 and F7 low and F5 high.
2. OSC 1 and OSC 2 become a two input clock supporting crystals, ceramic resonators, or RC networks. The PIC 1664B will execute instructions at one sixteenth the OSC frequency.
3. The interrupt system is connected and the interrupt/RTCC operation is as described in the PIC 1656 data sheet.
4. Bits 3-7 of F3 are used for interrupt service.

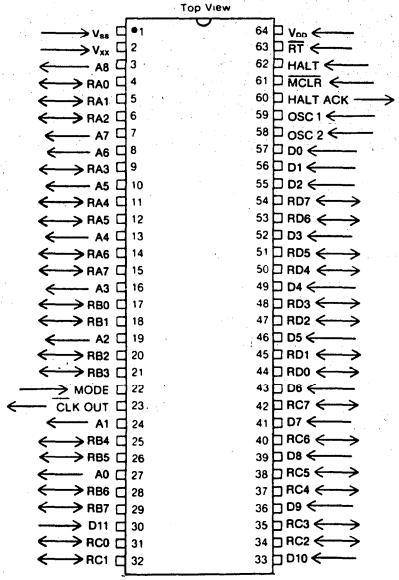
To insure proper chip operation, the Mode pin should be preset before $\overline{MCLR}$ is brought high at initialization. "Dynamic-type" switching of this pin during processor operation will result in undefined conditions and must be avoided.

PROGRAMMING CAUTIONS

The PIC 1664B is designed as a development circuit for emulating the operation of the PIC 1650A, PIC 1655A and PIC 1656. While all circuits in the PIC series have the same basic architecture and instruction set, there are differences which require attention on the part of the user to insure that all conditions are met for proper operation of the PIC 1664B with respect to the target PIC circuit (either PIC 1650A, PIC 1655A, or PIC 1656). The following checklist should be used to achieve proper emulation.

1. The MODE pin must be properly set (high for PIC 1650A/PIC 1655A or low for PIC 1656).
2. With the MODE pin high OSC 1 is a single clock input. A low on the MODE pin enables the two input clock.
3. For PIC 1650A and PIC 1655A emulation, bits 3-7 of F3 (the status register) should be considered undefined.
4. For PIC 1655A and PIC 1656 emulation bits 4-7 of F5 (the input only file) should be tied to V_{SS} (ground) as these bits are always read as low inputs.
5. For PIC 1655A and PIC 1656 emulation the pins corresponding to $F10_8$ (I/O port RD on the PIC 1650A) should be left unconnected. In this way $F10_8$ will operate as an internal register as is appropriate for the PIC 1655A and PIC 1656.
6. The I/O Programming Caution on page 3-11 describing the I/O variations between the PIC 1650A and the PIC 1655A/PIC 1656 must be carefully followed. The PIC 1664B contains all bidirectional input/ouput ports as required for PIC 1650A emulation. The I/O structure variation used in the PIC 1655A and PIC 1656 require careful adherence to the cautions listed in the following pages.
7. The RETURN (0002_8) instruction is not supported by the PIC 1650A and PIC 1655A and should not be used when emulating these parts. The HALT instruction (0001_8) is not recognized by any PIC circuit other than the PIC 1664B.
8. For PIC 1656 emulation the V_{XX} pin must be tied directly to V_{DD} as there is no V_{XX} pin on the PIC 1656.
9. The PIC 1664B contains 3 levels of Stack. Becuase the PIC 1650A and PIC 1655A only use 2 levels of Stack, caution should be used in programming. Make sure the PIC 1650A or PIC 1655A emulation is not utilizing 3 levels of Stack in software.

PIN CONFIGURATION
64 LEAD DUAL IN LINE



REGISTER FILE ARRANGEMENT

File (Octal)	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0→W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W.
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. The RTCC register keeps counting up after zero is reached. The counter increments on the falling edge of the input $\overline{RTCC}$. In the PIC 1656, Register F1 can also be incremented by the internal clock and is used to produce vectored interrupts.
F2	Program Counter (PC). The PC is automatically incremented and each instruction cycle can be written into under program control e.g., MOVWF F2. The PC is nine bits wide, but only the low order 8 bits can be read under program control.
F3	Status Word Register. F3 can be altered under program control only via bit set, bit clear, or MOVWF F3 instruction.

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
CNT	RTCR	IR	RTCE	IE	Z	DC	C

C (Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the most significant bit of the resultant.
For ROTATE instructions, this bit is loaded with either the high or low order bit of the source.

DC (Digit Carry): For ADD and SUB instructions, this bit is set if there is a carry out from the 4th low order bit of the resultant.

Z (Zero): Set if the result of an arithmetic operation is zero.

Bits: 3-7 Interrupt Service Flags. (Read as "ones" in PIC 1650A and PIC 1655A mode. In PIC 1656 mode, these bits are cleared on $\overline{MCLR}$.)

Bit 3: IE (external Interrupt Enable) bit

Bit 4: RTCE (Real Time Clock Enable) bit

Bit 5: IR (external Interrupt Request) bit

Bit 6: RTCR (Real Time Clock interrupt Request) bit

Bit 7: CNT (Count) bit (selects input to $\overline{RTCC}$)

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits are read as ones.
F5	I/O Register A (A0-A7)
F6	I/O Register B (B0-B7)
F7	I/O Register C (C0-C7)
F10	I/O Register D (D0-D7)
F11-F37	General Purpose Registers

PIC 1664B INTERRUPT SYSTEM

The interrupt system of the PIC 1656 is comprised of an external interrupt and an internal real-time clock/counter interrupt. These have different interrupt vectors, enable bits, and status bits. Both interrupts are controlled by the Status Word Register F3, shown below:

(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
CNT	RTCR	IR	RTCE	IE	Z	DC	C

(NOTE: F3 bits 3-7 are cleared on MCLR.)

The first high to low transition of the $\overline{RT}$ pin will set F3, bit 5 (IR, Interrupt Request) to a one. [The external interrupt is enabled by F3, bit 3 (IE, Interrupt Enable).] If the interrupt is enabled (IE is a one), or as soon as it is, during the next two instruction cycles the processor will push the current Program Counter contents onto the stack and execute the instruction at location 760_8. The IR bit is immediately cleared. Note that although the processor cannot be interrupted again until a return from interrupt (RETURN) instruction is executed, an additional interrupt request can be generated by another high to low transition of the $\overline{RT}$ pin, setting IR high again. If this is done, the processor will reinterrupt right after the return from the preceeding interrupt (assuming IE is a one).

The Real Time Clock/Counter (RTCC, File Register 1) has a similar mechanism of interrupt service. The clocking source for the RTCC is selected by bit 7 (CNT, Count Select) of the Status register. If CNT is set to a one, the RTCC will increment on each high to low transition of the $\overline{RT}$ pin. If CNT is cleared to a "zero", the RTCC will count at the internal instruction clock rate, 1/16 the frequency present on the OSC pins. When the RTCC transitions from 377_8 to 0, an interrupt request will be generated (RTCR is set to a one). If RTCE is a one, or as soon as it is set to a one, an interrupt will be generated. That is, the present contents of the Program Counter is stored on the stack and the instruction at location 740_8 is executed.

The RETURN instruction (0002_8) must be used to return from any interrupt service routine as it re-enables interrupts to allow pending or future interrupts to be generated. External interrupts have priority over RTCC driven interrupts in the event that both occur simultaneously (and both are enabled). Interrupts cannot be nested but will be serviced sequentially. The existence of any pending interrupts can be tested via the state of the IR and RTCR bits in the Status Word Register, and enabled or disabled as if desired.

The following is a summary of the relationship of F3 bits 3-7 to the PIC 1656 interrupt function:

Status Register Bits					Interrupt Logic
7 CNT	6 RTCR	5 IR	4 RTCE	3 IE	
0	0	0	0	X	The first high-to-low transition at the $\overline{RT}$ pin causes IR bit 5 to set to a one.
0	0	1	0	1	IE and IR both set to ones enables the PIC to interrupt to 760_8. IR (bit 5) then immediately resets to a zero.
0	X	X	X	X	The RTCC register is enabled to increment at the internal clock rate. When the contents of the RTCC register transition from 377_8 to 000_8, RTCR (bit 6) is set to a one.
1	X	X	X	X	The RTCC register is enabled to increment at the rate of the input at the $\overline{RT}$ pin (event timer mode). When the contents of the RTCC register transition from 377_8 to 000_8, RTCC (bit 6) is set to a one.
X	1	0	1	0	Both RTCE and RTCR set to ones enables the PIC to interrupt to 740_8. RTCR (bit 6) then immediately resets to a zero.
0	0	0	X	X	Regardless of the states of IE and RTCE, an interrupt on the $\overline{RT}$ pin and/or an RTCC transition from a full count to a zero count will set the IR bit and/or the RTCR bit to one(s).
X	1	0	1	1	If the IR bit is set to a zero at the time that the RTCR bit is set to a one, the PIC will interrupt to 740_8 (RTCC interrupt mode). The RTCR bit then immediately resets to a zero.
X	0	1	1	1	If the RTCR bit is set to a zero at the time that the IR bit is set to a one, the PIC will interrupt to 760_8 (external interrupt mode). The IR bit then immediately resets to a zero.
X	1	1	1	1	If the IR bit and the RTCR bit are each set to ones at the same time, the PIC will first interrupt to 760_8 (external interrupt mode). The IR bit then immediately resets to a zero. If the IR bits remains at a zero (indicating that no other external interrupts have occurred in the meantime), the PIC will then interrupt to 740_8 (RTCC interrupt mode) immediately after a RETFI instruction is executed. The RTCR bit then immediately resets to a zero.

X = DON'T CARE

Basic Instruction Set Summary

Each PIC instruction is a 12-bit word divided into an OP code which specifies the instruction type and one or more operands which further specify the operation of the instruction. The following PIC instruction summary lists byte-oriented, bit-oriented, and literal and control operations.

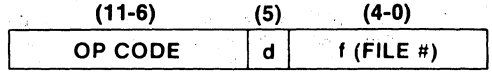
For byte-oriented instructions, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction.

For bit-oriented instructions, "b" represents a bit field designator which selects the number of the bit affected by the operation, while "f" represents the number of the file in which the bit is located.

For literal and control operations, "k" represents an eight or nine bit constant or literal value.

For an oscillator frequency of 1MHz for PIC 1650A and PIC 1655A (4MHz for PIC 1656) the instruction execution time as 4 μsec, unless a conditional test is true or the program counter is changed as a result of an instruction. In these two cases, the insruction execution time is 8 μsec.

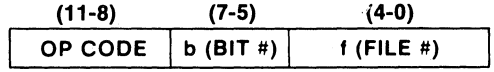
BYTE-ORIENTED FILE REGISTER OPERATIONS



For d = 0, f→W (PICAL accepts d = 0 or d = W in the mnemonic)
d = 1, f→f (If d is omitted, assembler assigns d = 1.)

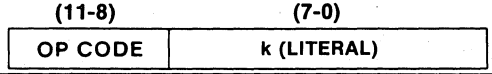
Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 000 (0000)	No Operation	NOP	—	—	None
000 000 1ff fff (0040)	Move W to f (Note 1)	MOVWF	f	W→f	None
000 001 000 000 (0100)	Clear W	CLRW	—	0→W	Z
000 001 1ff fff (0140)	Clear f	CLRF	f	0→f	Z
000 010 dff fff (0200)	Subtract W from f	SUBWF	f, d	f - W→d	C,DC,Z
000 011 dff fff (0300)	Decrement f	DECF	f, d	f - 1→d	Z
000 100 dff fff (0400)	Inclusive OR W and f	IORWF	f, d	W∨f→d	Z
000 101 dff fff (0500)	AND W and f	ANDWF	f, d	W•f→d	Z
000 110 dff fff (0600)	Exclusive OR W and f	XORWF	f, d	W⊕f→d	Z
000 111 dff fff (0700)	Add W and f	ADDWF	f, d	W+f→d	C,DC,Z
001 000 dff fff (1000)	Move f	MOVF	f, d	f→d	Z
001 001 dff fff (1100)	Complement f	COMF	f, d	$\bar{f}$→d	Z
001 010 dff fff (1200)	Increment f	INCF	f, d	f+1→d	Z
001 011 dff fff (1300)	Decrement f, Skip if Zero	DECFSZ	f, d	f - 1→d, skip if Zero	None
001 100 dff fff (1400)	Rotate Right f	RRF	f, d	f(n)→d(n-1),f(0)→C, C→d(7)	C
001 101 dff fff (1500)	Rotate Left f	RLF	f, d	f(n)→d(n+1), f(7)→C, C→d(0)	C
001 110 dff fff (1600)	Swap halves f	SWAPF	f, d	f(0-3)⇋f(4-7)→d	None
001 111 dff fff (1700)	Increment f, Skip if Zero	INCFSZ	f, d	f+1→d, skip if zero	None

BIT-ORIENTED FILE REGISTER OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
010 0bb bff fff (2000)	Bit Clear f	BCF	f, b	0→f(b)	None
010 1bb bff fff (2400)	Bit Set f	BSF	f, b	1→f(b)	None
011 0bb bff fff (3000)	Bit Test f, Skip if Clear	BTFSC	f, b	Bit Test f(b): skip if clear	None
011 1bb bff fff (3400)	Bit Test f, Skip if Set	BTFSS	f, b	Bit Test f(b): skip is set	None

LITERAL AND CONTROL OPERATIONS



Instruction-Binary (Octal)	Name	Mnemonic, Operands		Operation	Status Affected
000 000 000 010 (0002)	Return from Interrupt	RETURN	—	Stack→PC	None
100 0kk kkk kkk (4000)	Return and place Literal in W	RETLW	k	k→W, Stack→PC	None
100 1kk kkk kkk (4400)	Call subroutine (Note 1)	CALL	k	PC+1 → Stack, k → PC	None
101 kkk kkk kkk (5000)	Go To address (k is 9 bits)	GOTO	k	k→PC	None
110 0kk kkk kkk (6000)	Move Literal to W	MOVLW	k	k→W	None
110 1kk kkk kkk (6400)	Inclusive OR Literal and W	IORLW	k	kVW→W	Z
111 0kk kkk kkk (7000)	AND Literal and W	ANDLW	k	k•W→W	Z
111 1kk kkk kkk (7400)	Exclusive OR Literal and W	XORLW	k	k⊕W→W	Z

NOTES:

1. The 9th bit of the program counter in the PIC is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in program memory locations $0\text{-}377_8$. However, subroutines can be called from anywhere in the program memory since the Stack is 9 bits wide.
2. When an I/O register is modified as a function of itself, the value used will be that value present on the output pins. For example, an output pin which has been latched high but is driven low by an external device, will be relatched in the low state.

SUPPLEMENTAL INSTRUCTION SET SUMMARY

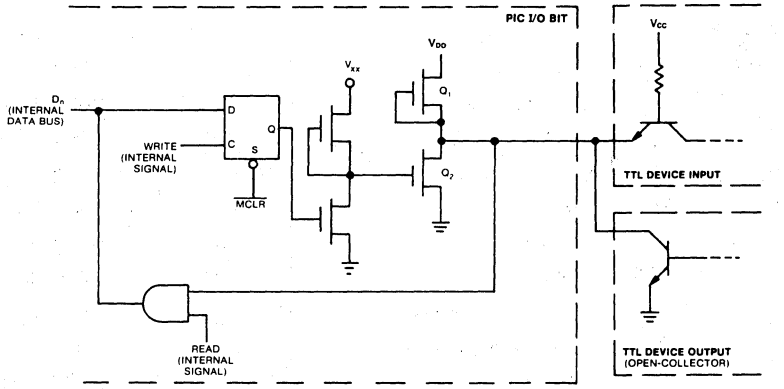
The following supplemental instructions summarized below represent specific applications of the basic PIC instructions. For example, the "CLEAR CARRY" supplemental instruction is equivalent to the basic instruction BCF 3,0 ("Bit Clear, File 3, Bit 0"). These instruction mnemonics are recognized by the PIC Cross Assembler (PICAL).

Instruction-Binary (Octal)	Name	Mnemonic, Operands	Equivalent Operation(s)	Status Affected
010 000 000 011 (2003)	Clear Carry	CLRC	BCF 3, 0	—
010 100 000 011 (2403)	Set Carry	SETC	BSF 3, 0	—
010 000 100 011 (2043)	Clear Digit Carry	CLRDC	BCF 3, 1	—
010 100 100 011 (2443)	Set Digit Carry	SETDC	BSF 3, 1	—
010 001 000 011 (2103)	Clear Zero	CLRZ	BCF 3, 2	—
010 101 000 011 (2503)	Set Zero	SETZ	BSF 3, 2	—
011 100 000 011 (3403)	Skip on Carry	SKPC	BTFSS 3, 0	—
011 000 000 011 (3003)	Skip on No Carry	SKPNC	BTFSC 3, 0	—
011 100 100 011 (3443)	Skip on Digit Carry	SKPDC	BTFSS 3, 1	—
011 000 100 011 (3043)	Skip on No Digit Carry	SKPNDC	BTFSC 3, 1	—
011 101 000 011 (3503)	Skip on Zero	SKPZ	BTFSS 3, 2	—
011 001 000 011 (3103)	Skip on No Zero	SKPNZ	BTFSC 3, 2	—
001 000 1ff fff (1040)	Test File	TSTF f	MOVF f, 1	Z
001 000 0ff fff (1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001 001 1ff fff (1140) 001 010 dff fff (1200)	Negate File	NEGF f,d	COMF f, 1 INCF f, d	Z
011 000 000 011 (3003) 001 010 dff fff (1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011 000 000 011 (3003) 000 011 dff fff (0300)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011 000 100 011 (3043) 001 010 dff fff (1200)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011 000 100 011 (3043) 000 011 dff fff (0300)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
101 kkk kkk kkk (5000)	Branch	B k	GOTO k	—
011 000 000 011 (3003) 101 kkk kkk kkk (5000)	Branch on Carry	BC k	BTFSC 3,0 GOTO k	—
011 100 000 011 (3403) 101 kkk kkk kkk (5000)	Branch on No Carry	BNC k	BTFSS 3,0 GOTO k	—
011 100 100 011 (3043) 101 kkk kkk kkk (5000)	Branch on Digit Carry	BDC k	BTFSC 3,1 GOTO k	—
011 001 000 011 (3443) 101 kkk kkk kkk (5000)	Branch on No Digit Carry	BNDC k	BTFSS 3,1 GOTO k	—
011 101 000 011 (3103) 101 kkk kkk kkk (5000)	Branch on Zero	BZ k	BTFSC 3,2 GOTO k	—
011 101 000 011 (3503) 101 kkk kkk kkk (5000)	Branch on No Zero	BNZ k	BTFSS 3,2 GOTO k	—

I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (PIC is outputting) or the output of an open collector TTL device (PIC is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a high level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source a minimum of 100μA. Care, however, should be exercised when using open collector devices due to the potentially high TTL leakage current which can exist in the high logic state.

TYPICAL INTERFACE-BIDIRECTIONAL I/O LINE



Programming Cautions

The use of the bidirectional I/O ports are subject to certain rules of operation. These rules must be carefully followed in the instruction sequences written for I/O operation.

Bidirectional I/O Ports

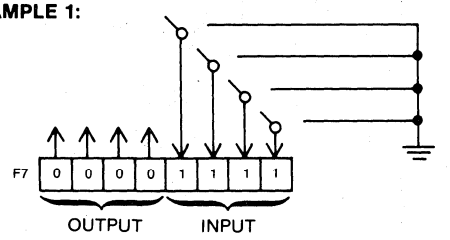
The bidirectional ports may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction. The outputs are latched and remain unchanged until the output latch is rewritten. **For use as an input port the output latch must be set in the high state.** Thus the external device inputs to the PIC circuit by forcing the latched output line to the low state or keeping the latched output high. This principle is the same whether operating on individual bits or the entire port.

Some instructions operate internally as input followed by output operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation, and re-output the result. Caution must be used when using these instructions. As an example a BSF operation on bit 5 of F7 (port RC) will cause all eight bits of F7 to be read into the CPU. Then the BSF operation takes place on bit 5 and F7 is re-output to the output latches. If another bit of F7 is used as an input (say bit 0) then bit 0 must be latched high. If during the BSF instruction on bit 5 an external device is forcing bit 0 to the low state then the intput/output nature of the BSF instruction will leave bit 0 latched low after execution. In this state bit 0 cannot be used as an input until it is again latched high by the programmer. Refer to the examples below.

Successive Operations on Bidirectional I/O Ports

Care must be exercised if successive instructions operate on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before the next instruction which causes that file to be read into the CPU (MOVF, BIT SET, BIT CLEAR, and BIT TEST) is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. This will happen if t_{pd} (See I/O Timing Diagram) is greater than $\frac{1}{4}t_{cy}$ (min). When in doubt, it is better to separate these instructions with a NOP or other instruction.

EXAMPLE 1:



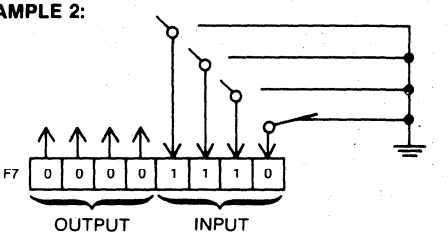
What is thought to be happening:

BSF 7,5

Read into CPU:	00001111
Set bit 5:	00101111
Write to F7:	00101111

If no inputs were low during the instruction execution, there would be no problem.

EXAMPLE 2:



What could happen if an input were low:

BSF 7,5

Read into CPU:	00001110
Set bit 5:	00101110
Write to F7:	00101110

In this case bit 0 is now latched low and is no longer useful as an input until set high again.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 125°C
Storage Temperature ..... −55°C to +150°C
Voltage on any pin with Respect to V_{SS} ..... −0.3V to +12.0V
Power Dissipation 1000mW
Power Dissipated by any one I/O pin (Note 1) 60mW
Power Dissipated by all I/O pins (Note 1) 600mW

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Standard Conditions (unless otherwise stated):

DC CHARACTERISTICS

Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Primary Supply Voltage	V_{DD}	4.5	—	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	—	10.0	V	(Note 2)
Primary Supply Current	I_{DD}	—	30	55	mA	No Load
Output Buffer Supply Current	I_{XX}	—	1	5	mA	No Load (Note 3)
Input Low Voltage	V_{IL}	−0.2	—	0.8	V	
Input High Voltage (except $\overline{MCLR}$, $\overline{RTCC}$/$\overline{RT}$ & OSC 1 when driven externally)	V_{IH1}	2.4	—	V_{DD}	V	
Input High Voltage ($\overline{MCLR}$, $\overline{RTCC}$/$\overline{RT}$ & OSC 1)	V_{IH2}	V_{DD}−1	—	V_{DD}	V	
Output High Voltage	V_{OH}	2.4	—	V_{DD}	V	I_{OH} = −100μA provided by internal pullups (Note 4)
Output Low Voltage (I/O only)	V_{OL1}	—	—	0.45	V	I_{OL} = 1.6mA, V_{XX} = 4.5V
		—	—	0.90	V	I_{OL} = 5.0mA, V_{XX} = 4.5V
		—	—	0.90	V	I_{OL} = 5.0mA, V_{XX} = 8.0V
		—	—	1.20	V	I_{OL} = 10.0mA, V_{XX} = 8.0V
		—	—	2.0	V	I_{OL} = 20.0mA, V_{XX} = 8.0V (Note 5)
Output Low Voltage A0-A8, (CLK OUT), HALT ACK	V_{OL2}	—	—	0.45	V	I_{OL} = 1.6mA (Note 5)
Input Leakage Current ($\overline{MCLR}$, $\overline{RTCC}$/$\overline{RT}$)	I_{LC}	−10	—	+10	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$ (Note 6)
Input Low Current (all I/O ports)	I_{IL}	−0.2	−0.6	−1.6	mA	V_{IL} = 0.4V internal pullup
Input High Current (all I/O ports)	I_{IH1}	−0.1	−0.4	—	mA	V_{IH} = 2.4V
Input High Current (HALT)	I_{IH2}	—	50	200	μA	V_{IH}=2.4V, internal pulldown

NOTES:

1. Power dissipation for I/O pins is calculated by
   $\Sigma (V_{CC} - V_{IL}) (|I_{IL}|) + \Sigma (V_{CC} - V_{OH}) (|I_{OH}|) + \Sigma (V_{OL}) (I_{OL})$.
   The term I/O refers to all interface pins; input, ouput or I/O.
2. V_{XX} supply drives only the I/O ports.
3. The maximum I_{XX} current will be drawn when all I/O ports are outputting a High.
4. Positive current indicates current into pin. Negative current indicates current out of pin.
5. Total I_{OL} for all output pins (I/O ports plus CLK OUT) must not exceed 225mA.
6. Also applies to OSC 1 pin in PIC 1656 mode.

Standard Conditions (unless otherwise stated):

AC CHARACTERISTICS

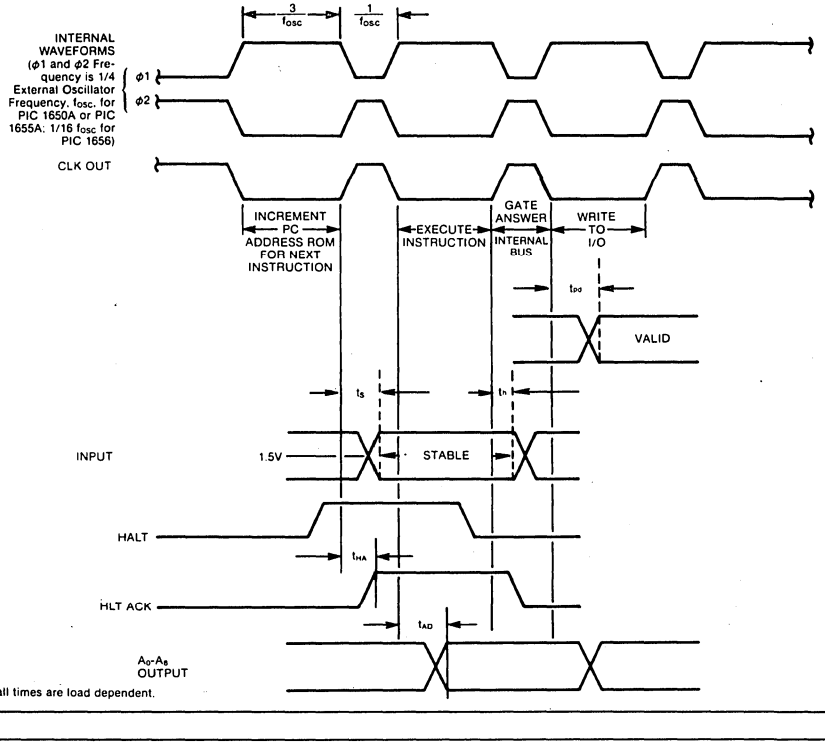
Operating Temperature T_A = 0°C to +70°C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Instruction Cycle Time	t_{CY}	4	—	20	μs	0.2MHz −1.0MHz external time base 1650A/1655A mode 0.8MHz −4.0MHz external time base 1656 mode (Note 1)
$\overline{RT}$/$\overline{RTCC}$ Input						
Period	t_{RT}	t_{CY}	—	—	—	
High Pulse Width	t_{RTH}	½t_{CY}	—	—	—	
Low Pulse Width	t_{RTL}	½t_{CY}	—	—	—	(Note 2)
I/O Ports						
Data Input Setup Time	t_S	—	—	¼t_{CY}−125	ns	
Data Input Hold Time	t_h	0	—	—	ns	
Data Output Propagation Delay	t_{pd}	—	500	800	ns	Capacitive load = 50pF
OSC Input						
External Input Impedance High (PIC 1650A, 55A mode)	R_{OSCH}	—	120	—	Ω	V_{osc} = 5V
External Input Impedance High (PIC 1656 mode)	R_{OSCH}	—	106	—	Ω	V_{osc} = 5V
External Input Impedance Low	R_{OSCL}	—	10^6	—	Ω	V_{osc} = 0.4V
						Applies to external OSC drive only.
HALT ACK Output						
Delay from ϕ2	t_{HA}	—	200	—	ns	
A0-A8 Output						
Delay from ϕ1	t_{AD}	—	350	—	ns	

NOTES:

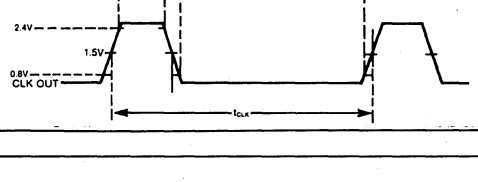
1. Instruction cycle period (t_{CY}) equals four times the input oscillator time base period for 1650A/1655A operation or sixteen times oscillator time base period for 1656 operation.
2. Due to the synchronous timing nature between CLK OUT and the sampling circuit used on the RT input, CLK OUT may be directly tied to the RT input without any loss of counts.

I/O TIMING

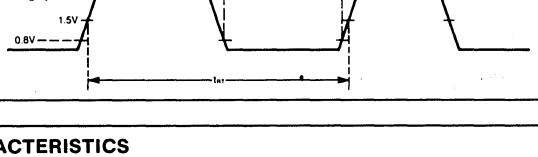


NOTE: Rise and fall times are load dependent.

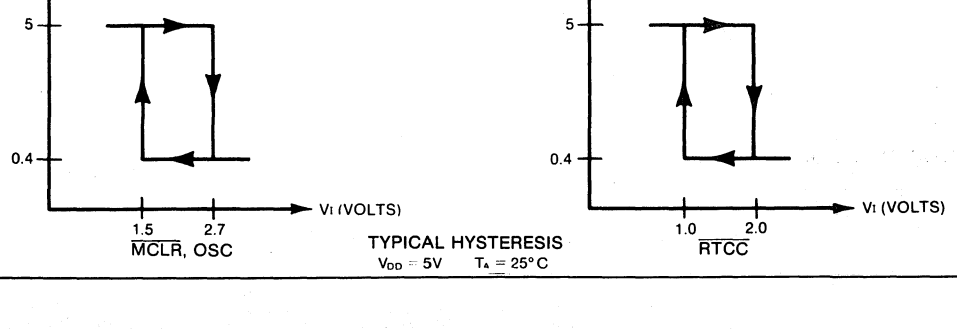
CLK OUT TIMING



RTCC/RT TIMING



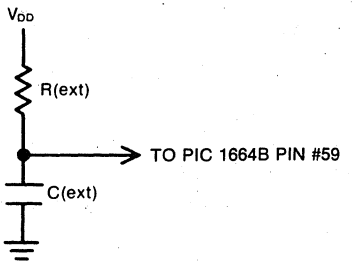
SCHMITT TRIGGER CHARACTERISTICS

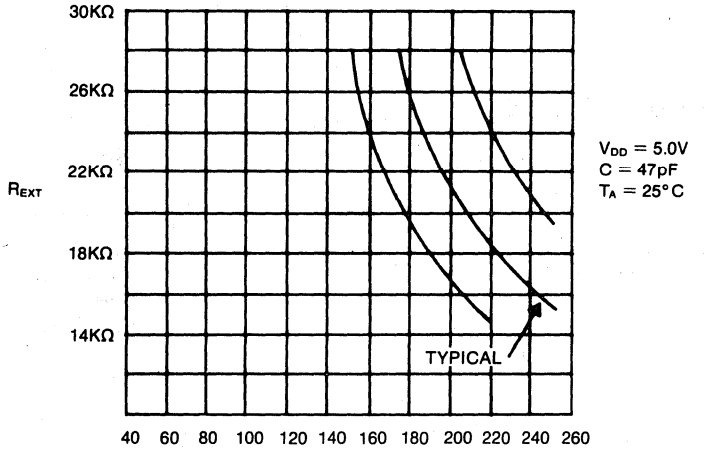


TYPICAL HYSTERESIS
V_{DD} = 5V T_A = 25°C

PIC 1650A, 1655A EMULATION OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

RC OPTION OPERATION

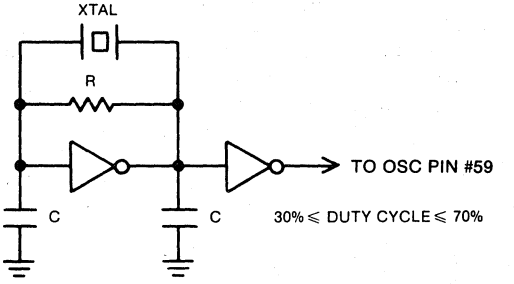




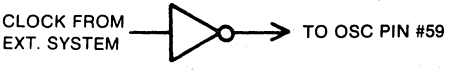
Oscillator Frequency With Typical Unit To Unit Variance

Unit to Unit Variation at V_{DD} = 5.0V, T_A = 25°C is ±25%
Variation from V_{DD} = 4.5V −7.0V referenced to 5V is −3%, +9%
Variation from T_A = 0°C −70°C referenced to 25°C is +3%, −5%

BUFFERED CRYSTAL INPUT OPERATION

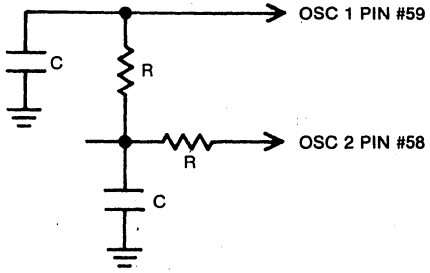


EXTERNAL CLOCK INPUT OPERATION

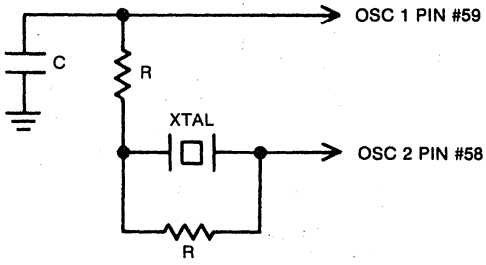


PIC 1656 EMULATION OSCILLATOR OPTIONS (TYPICAL CIRCUITS)

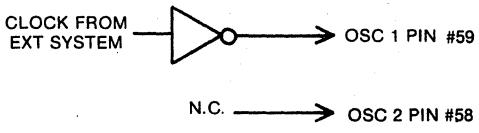
RC OPTION OPERATION



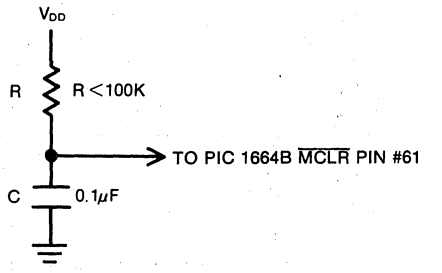
CRYSTAL INPUT OPERATION



EXTERNAL CLOCK INPUT OPERATION

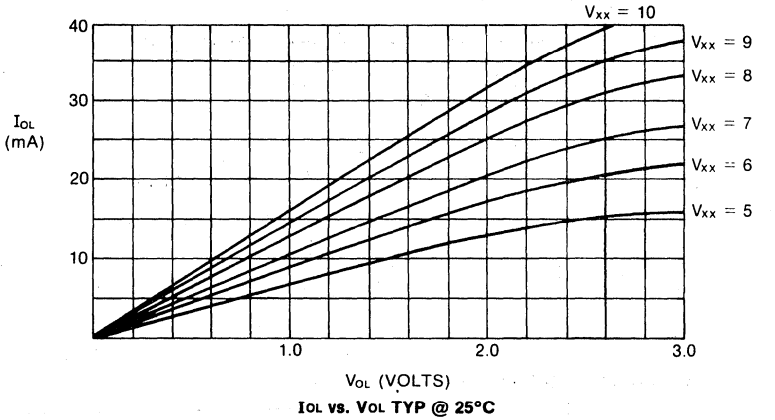


MASTER CLEAR



Master Clear requires >1.0ms delay before activation after power is applied to the V_{DD} pin. To acheive this, an external RC configuration as shown can be used (assuming V_{DD} is applied as a step function).

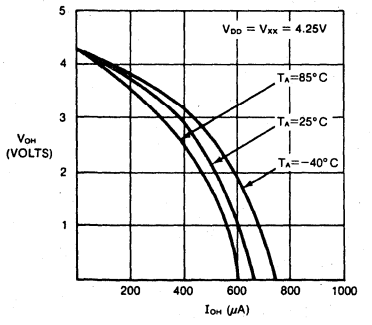
OUTPUT SINK CURRENT GRAPH



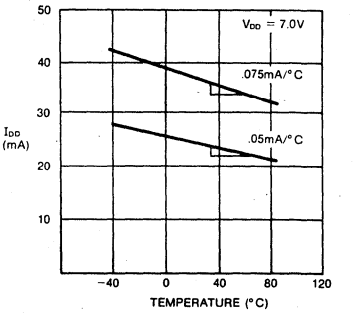
IOL vs. VOL TYP @ 25°C

The Output Sink Current is dependent on the V_{xx} supply and the output load. This chart shows the typical curves used to express the output drive capability.

VOH VS IOH (I/O PORTS)



POWER SUPPLY CURRENT VS TEMPERATURE



PIC 1650A/PIC 1655A EMULATION CAUTIONS

When emulating a PIC 1650A or PIC 1655A using a PICES development system certain precautions should be taken.

A. Be sure that the PICES Module being used is programmed for the PIC 1650A/PIC 1655A mode. (Refer to PICES Manual). The PIC 1664B contained within the module should have the MODE pin #22 set to a high state.

1. This causes the $\overline{\text{MCLR}}$ to force all I/O registers high.
2. The OSC 1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes disabled and the RTCC always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are all ones.

B. Make sure to only use two levels of stack within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 40 pin socket for the PIC 1650A and the 28 pin socket for the PIC 1655A module plugs.

E. Make sure that during an actual application that the $\overline{\text{MCLR}}$ input swings from a low to high level a minimum of 1msec after the supply voltage is applied.

F. If an external oscillator drive is used, be sure that it can drive the 120Ω input impedance of the OSC pin on the PIC 1650A and PIC 1655A.

G. The cable length and internal variations may cause some parameter values to differ between the PICES module and a production PIC 1650A and PIC 1655A.

PIC 1656 EMULATION CAUTIONS

When emulating a PIC 1656 using a PICES development system certain precautions should be taken.

A. Be sure that the PICES Module being used is programmed for the PIC 1656 mode. (Refer to PICES Manual). The PIC 1664B contained within the module should have the MODE pin #22 set to a low state.

1. This causes the $\overline{\text{MCLR}}$ to force F5 register high and F6 and F7 low.
2. The OSC 1 pin #59 becomes a single clock input pin.
3. The interrupt system becomes enabled and the RT always counts on the trailing edges.
4. Bits 3 through 7 on file register F3 are used for interrupt servicing.

B. All three levels of stack can be used within the program.

C. Make sure all I/O cautions contained in this spec sheet are used.

D. Be sure to use the 28 pin socket for the module plug.

E. Make sure that during an actual application that the $\overline{\text{MCLR}}$ input swings from a low to high level a minimum of 1msec after the supply voltage is applied.

F. If an external oscillator drive is used, be sure that it can drive the 120Ω input impedance of the OSC pin on the PIC 1656.

G. The cable length and internal variations may cause some parameter values to differ between the PICES module and a production PIC 1656.

PIC CUSTOMER ORDER FORM

Customer Name_____ Division_____

Address_____

City_____ State_____ Zip_____ Country_____

Telephone Number_____ Ext._____

Customer Contact_____ Title_____

PIC part number_____

Customer Part Number_____

Customer Marking Requirement_____

PIC Temperature Range Selection:

0°C to 70°C ☐ −40°C to 85°C ☐

Program ROM Pattern Media Paper Tape ☐ Prom _____ ☐ Other _____ ☐
Part Number

Refer to PICES and PFD Manuals for formats

Customer Purchase Order Number _____

Date of Purchase Order_____

Prototypes requested by _____

Customer Signature_____

Title _____

Date_____

PIC Development Systems

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
PIC DEVELOPMENT SYSTEM	In-circuit emulation and debug system. Can operate as stand alone system or as peripheral to host computer.	PICES	2-58
PIC FIELD DEMO SYSTEMS	Contains PIC 1664B, PROMs, and provision for on-board RC oscillator or external clock.	PFD 1000	2-60
		PFD 1010	2-60
PIC ASSEMBLER	Converts symbolic source programs for the PIC series into object code.	PICAL	2-61

PIC In-Circuit Emulation System

FEATURES

- Complete in-circuit emulation and debug capability
- Multiple system configurations to match user requirements
- Standard serial interface for system integration
- Powerful 16-bit microprocessor for system control
- Multiple breakpoints, single step, program trace and editing capabilities
- On-board diagnostics for system hardware troubleshooting

DESCRIPTION

The PICES is an in-circuit emulation and debug system designed to provide the user with a complete tool for testing, trouble-shooting, and modifying both the software program for the PIC circuit as well as the total system application. The PICES is a self-contained unit which can operate in a stand-alone configuration or as a peripheral device to a host processor.

ARCHITECTURE

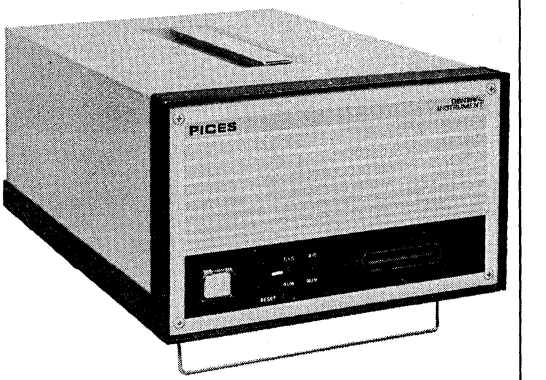
The PICES system contains two processors. The User Processor is a PIC 1664B ROM-less microcomputer with external RAM. With the RAM loaded with the user's application program, the PIC 1664B emulates the operation of the PIC 1650A, PIC 1655A, or PIC 1656. A 28 or 40 pin in-circuit emulation cable attaches the PIC 1664B to the application system. The Control Processor is a CP1600 sixteen bit microprocessor with 8K of program ROm and 1K of RAM. This processor controls the functions of the PICES including I/O interfacing, manipulation of the User Processor and interpretation and execution of the PICES command set.

OPERATION

STAND-ALONE MODE: The PICES is attached directly to a serial I/O device; typically a teletype. The user program is entered either using the paper tape reader/punch unit on the teletype or by manually setting each location in the PIC program memory to the desired value. Once the program memory is loaded, all PICES emulation and debug commands can be issued on the teletype keyboard and PICES responses are returned on the teletype printer. The serial interface can be either RS232C or current loop and the baud rate is switch selectable.

PERIPHERAL MODE: The PICES can be configured such that the unit itself is peripheral to another computer system. The PICES can be attached as an additional peripheral device or in series with the system TTY or CRT device. In this mode the user's computer facility can become a one station total development system. The computer text editor is used to develop the PIC source code. The Fortran PIC cross assembler will translate this source code into PIC machine code; the machine code is then downloaded into the PICES. All PICES commands are entered through the system terminal. Minor modifications can be done directly to the PICES. Major changes require re-editing the source code, re-assembling and loading of the PICES.

PIC IN-CIRCUIT EMULATION SYSTEM

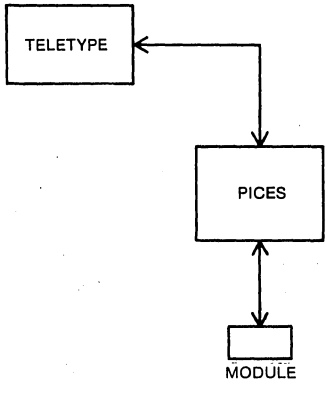


DATA MANUAL

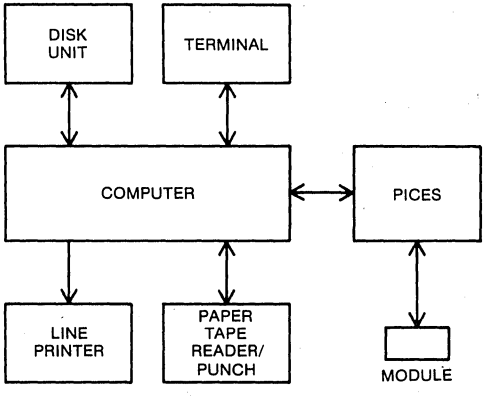
A detailed PICES Data Manual is available. This manual describes the installation and operation of the PICES system. Included in the manual are explanations of the command set with examples for illustration.

PICES CONFIGURATIONS

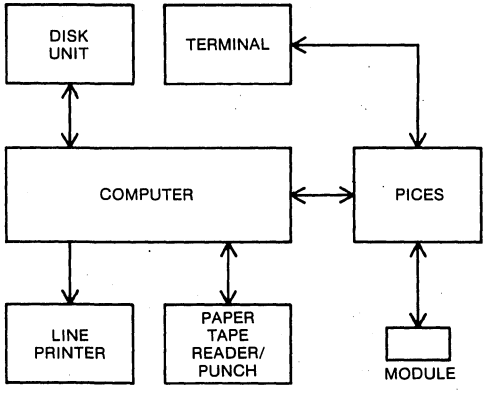
STAND ALONE MODE



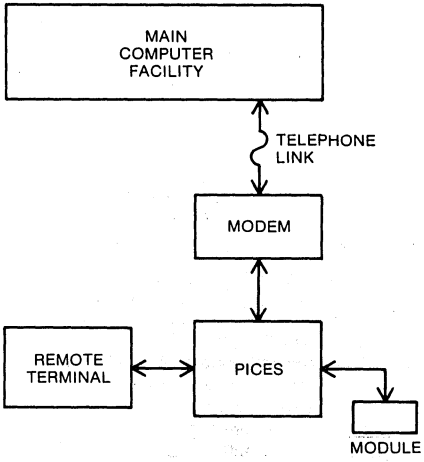
PERIPHERAL CONFIGURATION A



PERIPHERAL CONFIGURATION B



PERIPHERAL CONFIGURATION C



PIC Field Demo System

FEATURES

- Single +5V operation
- Adjustable on-board clock
- Optional external clock and reset
- 512 x 12 words of program storage
- Dimensions: 4" x 4⅜"
- In circuit emulation cable length: 14"
- PFD 1000 emulates PIC 1650A and PIC 1655A
- PFD 1010 emulates PIC 1656

DESCRIPTION

The PIC Field Demo Systems provide the user with a compact and portable method of evaluating and demonstrating application performance before the commitment is made to ROM masking of the PIC circuit. The PFD 1000/1010 systems each consist of a single printed circuit module containing a PIC 1664B ROM-less PIC circuit with external Erasable/Programmable Read Only Memory (EPROM) attached. The EPROM contains the user's application program. A 40 or 28 lead ribbon cable attaches to the PFD Module terminating with a DIP plug providing emulation of the PIC circuit in the application.

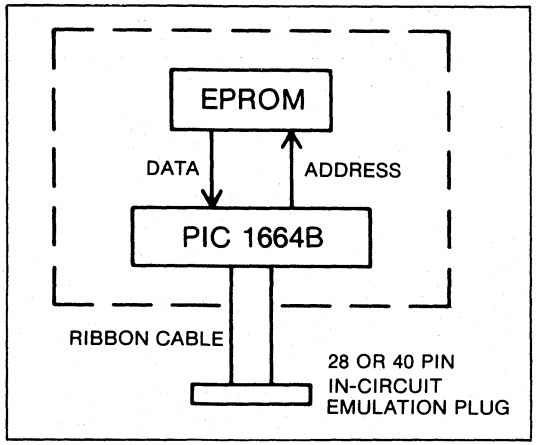
Provision for jumper options on the PFD Series module allows the user to select various modes of operation as appropriate to the application. Internal or external clock and power supply is available.

ORDERING INFORMATION

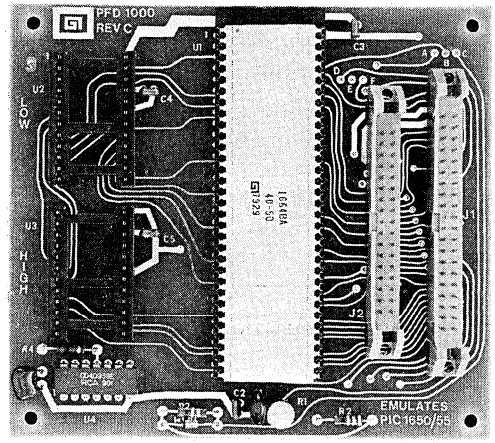
The PFD Module comes complete with a PIC 1664B ROM-less PIC emulator circuit, EPROMs and an in-circuit-emulation cable. Order the module to emulate the particular PIC circuit to be emulated.

DATA MANUAL

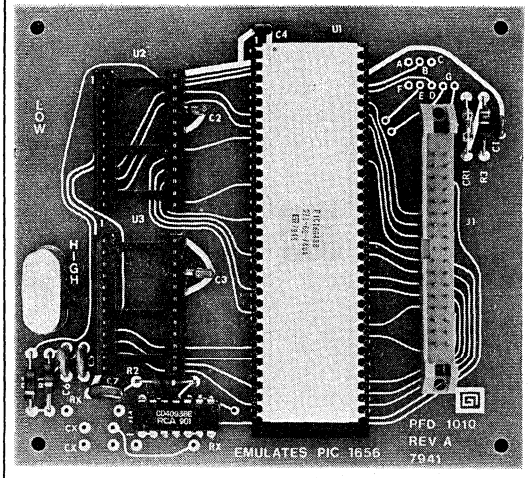
A complete description of the PFD 1000/1010 system is contained in the PIC Field Demo Systems Data Manual.



PIC FILED DEMO SYSTEM (PFD 1000)



PIC FILED DEMO SYSTEM (PFD 1010)



PIC Cross Assembler

FEATURES

- Symbolic machine operation codes (opcodes, mnemonics)
- Symbolic address assignment and reference
- Relative addressing
- Data creation statements
- Storage reservation statements
- Assembly listing control statements
- Character codes may be specified as ASCII or EBCDIC
- Addresses can be generated as constants
- Comments and remarks may be encoded for documentation
- Cross reference table listing

DESCRIPTION

The PICAL Cross Assembler is used for the General Instrument family of microcomputers including the PIC 1650A, 1655A, and 1656. The function of this Cross Assembler program is to translate the Symbolic Code into the machine code required by the actual processors. The assembler program is written in Fortran IV to achieve compatibility with most computer systems, including those manufactured by DEC, Data General, Hewlett-Packard, Xerox, and others. It is modular and may be executed in an overlay mode should memory restrictions make that necessary. The program is approximately 3400 Fortran card images in length, 20% of which are comments. The program is written in ANSI standard Fortran IV and no facility peculiar to one machine was utilized. This was done in order to eliminate Fortran compatibility problems.

The mnemonic Operation Codes are identical to those used in other PIC literature and in other software products. This has been done to eliminate any possible problems of program compatibility and to obviate the necessity of learning new assembly languages. In addition, several directives and features are implemented and described in the PICAL Users Manual.

The assembler is a two pass program that builds a symbol table, issues helpful error messages, produces an easily read program listing and symbol table, and outputs a computer readable object (load) module.

The assembler features macro capability, symbolic and relative addressing, forward references, complex expression evaluation, cross reference listing and a versatile set of directives.

The assembler program, written in Fortran, is usually supplied as 9 track, 1600 BPI, 80 column card image records, unblocked and unlabeled magnetic tapes in either EBCDIC or ASCII code. The label on the tape reel will clearly specify the information.

The program is also supplied in compiled version for appropriate media and machines, including the Data General μNova® system.

ASSEMBLER LANGUAGE

An assembly language program is written in symbolic machine language. It is comprised of statements. A statement is either a symbolic instruction, a directive statement, a macro statement, or a comment.

The symbolic machine instruction is a written specification for a particular machine operation expressed by symbolic operation codes and sometimes symbolic addresses or operands.

A directive statement is a statement which is not translated into a machine instruction, but rather is interpreted as a directive to the assembler program.

Statements are always written in a particular format. This format is depicted below.

LABEL FIELD	OPERATION FIELD	OPERAND FIELD	COMMENT FIELD

SYNTAX

The Assembler Language is a language like any other. That is, it has a character set, vocabulary, rules of grammar, and allows for individuals to define new words or elements. The rules that describe the language are termed the syntax of the language.

For an expression or statement in assembler language to be translated by the assembly program it must be written correctly in accord with the rules of syntax.

A **symbol** is a sequence of characters. The first character in a symbol must be alphabetic or the special characters ?, $, or &. Special characters except for the above three may not be used in a symbol. Imbedded blanks are not permitted. The user is cautioned not to use symbols that start with the ? character as the assembler generates "local" symbols starting with this character.

Only the first six characters of a symbol are used by the Assembler to define that symbol; the remaining characters are for documentation. The parameter that dictates the number of characters used to define a symbol may be changed in the Fortran Source code.

A **constant** is an invariant quantity. It may be an arithmetic value or a character code. There are several ways of specifying constants in this assembler language.

Octal constants may be defined as a sequence of numeric characters optionally preceded by a plus sign or a minus sign. If unsigned, the value is assumed to be positive. Decimal constants are defined in the same manner but preceded by a decimal point.

In most cases constants must be contained in one 8 bit word. A constant can contain an unsigned number with a value from 0 to 255. When a constant is negative its equivalent two's complement representation is generated and placed in the field specified. An eight bit two's complement number can range from −128 to +127. Whenever an attempt is made to place a constant in a field for which it is too large, an error message is generated by the assembler.

An **expression** is a sequence of one or more symbols, constants, or other expressions separated by the arithmetic operators +, −, *, /. Parentheses are used in the normal manner to establish the correct order of the arithmetic operators. Expressions are evaluated left to right with multiplication and division being performed before addition and subtraction.

The expression must resolve to a single unique value. All expressions are evaluated modulo 65536 and hence are all 16 bit quantities. In most cases the value of the final expression must be contained in a 12 bit word.

DIRECTIVES

The directives or pseudo-operations are written as ordinary statements in the assembler language, but rather than being translated into equivalent machine language, they are interpreted as commands to the assembler itself.

Through use of these directives, the Assembler will reserve memory space, define bytes of data, control the listing, assign values to symbols, etc.

The directives are:

ORG	Set Program Origin
END	End of Assembly
EQU	Equate a Symbol to an Expression
SET	Set a Symbol equal to an Expression
DATA	Data Definition
RES	Reserve Storage
ZERO	Reserve Storage and fill with zeros
PAGE	Advance Listing Form to next page
SPAC	Space lines on listing
TITLE	Set Program Heading
LIST	List the Elements Specified
OPTION	Set Program Options (same as LIST)
NLIST	Suppress listing of the Elements Specified
IF	Conditional Assembly Statement
ELSE	Conditional Assembly Statement Converse
ENDIF	End Conditional Assembly Code

MACROS

A macro is a sequence of instructions that can be inserted in the assembly source text by encoding a single instruction, the macro call. The macro definition is written only once and can be called any number of times. The macro definition may contain parameters which can be changed for each call. The macro facility simplifies the coding of programs, reduces the chance of programmer error, and makes programs easier to understand as the source code need only be changed in one location, the macro definition.

A macro definition consists of three parts: a heading, a body, and a terminator. This definition must precede any macro call. A macro may be redefined at any time with the latest definition of a macro name applying to a macro call. A standard assembler mnemonic (e.g. CLRF) may also be redefined by defining a macro with the name CLRF. In this case all subsequent uses of the CLRF instruction in the program will cause the macro to be expanded.

The PIC assembler which is precompiled for the Intel MDS® does not have a MACRO capability due to the possibly limited memory space available.

USING THE ASSEMBLER

The Assembler is written entirely in Fortran and is comprised of a main program and several subroutines. The main program appears first on the tape and the last subroutine is followed by a tape mark. The Assembler may be compiled from the tape.

The Assembler should be compiled and its object module stored on some secondary storage device. If desired, the Assembler may be compiled and linked to perform in the overlay mode. Communications between subprograms is via blank common and subroutine call parameters.

The Assembler is a two pass Assembler wherein the source code is scanned twice. During the first pass the labels are examined and placed into a symbol table. Certain errors may be detected during Pass One; these will be displayed on the output listing.

During Pass Two, the object code is completed, symbolic addresses resolved, a listing and object module are produced. Certain errors, not detected during Pass One may be detected and displayed on the listing.

At the end of the Assembly process a symbol table or cross reference table may be displayed.

The following steps are taken to assemble a source program:

1. Write a program utilizing the instruction mnemonics of the PIC Instruction Set and directives. Encode the argument fields with constants, labels, symbolic addresses, etc.
2. Transfer the source program to some computer readable medium; cards, tape, etc. This medium should correspond to the input device expected by the Assembler. On some systems device assignments may be changed during the course of an assembly by utilizing proper system control cards.
3. Load the source code.
4. Execute the Assembler Program.
5. Get listing and object module as output.

During Pass Two of the assembly process a program listing is produced. The listing displays all information pertaining to the assembled program, both assembled data and the users original source statements.

The listing may be used as a documentation tool through the inclusion of the comments and remarks that describe the function of the particular program segment.

The main purpose of the listing is to convey all pertinent information about the assembled program, i.e. the memory addresses and their contents. The load module, also produced during Pass Two, contains the address and content information but in a format that can be read by people only with great effort.

TYPICAL ASSEMBLER LISTING

```
LINE    ADDR   B1    B2      TEST CHECKSUM

   1                                TITLE  'TEST CHECKSUM'
   2                                LIST   P=1655,X,E
   3  000000  0000            START NOP
   4  000001  0000  0000            MOV    F0
*** OPCODE ERROR
   5  000003  0070                  MOVWF  30
   6  000004  0041            START2 MOVWF  1
   7  000005                  START3
   8  000005  0043                  MOVWF  3
   9                                ORG    20
  10  000020  0001  0002            DATA   1,2,3
  11  000022  0003
  12  000023                        RES    2
  13  000025                        ZERO   3
  14                                IF     START
  15                                IORWF  FR
  16                                ADDWF  F10
  17                                ELSE
  18  000030  0551                  ANDWF  F9
  19                                ENDIF
  20  000031  0041                  MOVWF  1
  21  000032  0043                  MOVWF  3
  22  000033  0044                  MOVWF  4
  23  000034  5002                  GOTO   START+2
  24                                ORG    30
  25  000030  5030                  GOTO   1
  26  000031  6031                  MOVLW  1
  27  000032  0041                  MOVWF  1
  28  000033  0042                  MOVWF  2
  29  000034  0043                  MOVWF  3
  30  000035  0044                  MOVWF  4
  31  000036  0045                  MOVWF  5
*** INVALID FILE REGISTER
  32  000037  0047                  MOVWF  7
  33  000040  0050                  MOVWF  10
  34                                                              )
  35  000041  1005                  MOVF   5,W
  36  000042  1006                  MOVF   6,F
*** INVALID FILE REGISTER
  37  000043  1047                  MOVF   7
  38  000044  1010                  MOVF   10,W
  39                                                              )
  40  000045  3345                  BTFSC  5,7
  41  000046  3005                  BTFSC  5,0
  42  000047  3006                  BTFSC  6,0
*** INVALID FILE REGISTER
  43  000050  3346                  BTFSC  6,7
*** INVALID FILE REGISTER
  44  000051  3007                  BTFSC  7,0
  45  000052  3347                  BTFSC  7,7
  46  000053  3010                  BTFSC  10,0
  47  000054  3350                  BTFSC  10,7
  48                                                              )
  49                                                              )
  50                                ORG    777
  51  000777  5000                  GOTO   START
  52                                                              )
  53                                                              )
  54  001000                        END


ASSEMBLER ERRORS =    5
```

USERS MANUAL

A complete description of the PICAL Cross Assembler program with detailed explanations of how it is used is contained in the PICAL Users Manual.

GENERAL INSTRUMENT

Series 1600

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
16 BIT MICROPROCESSOR	Third generation minicomputer architecture with 8 general purpose registers.	CP1600	2-64
		CP1610	2-64
D/A CONVERTER	Contains 4 x 10 bit D/A registers.	DAC 1600	2-71
I/O BUFFER	A programmable buffer with 16 bidirectional lines.	IOB 1680	2-75
ANALOG MULTIPLEXER	Binary addressed mux, includes on-chip address latch.	MUX 1600	2-81
READ ONLY MEMORY	2048 x 10 bits.	RO-3-9504	2-83

16-Bit Microprocessor

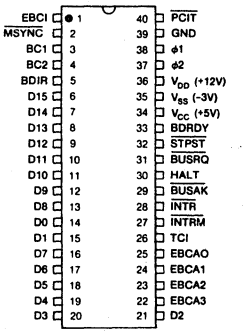
FEATURES

- 8 program accessible 16-bit general purpose registers
- 86 basic instructions
- 4 addressing modes: immediate, direct, indirect, relative
- Conditional branching on status word and 16 external conditions
- Unlimited interrupt nesting and priority resolution
- 16-bit logic and 2's complement arithmetic
- Status logic and word: carry, overflow, sign, zero
- Direct memory access (DMA) for high speed data transfer
- 64K memory using single address
- TTL compatible/simple bus structure
- CP1600: 600ns cycle time, 3.3MHz 2-phase clock
- CP1610: 1μs cycle time, 2MHz 2-phase clock

PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View



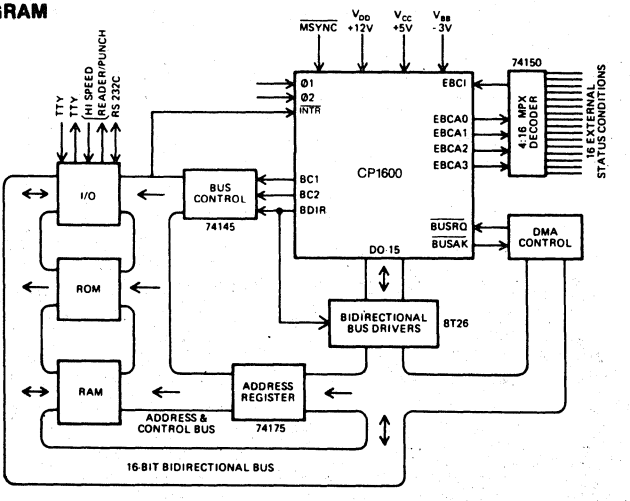
DESCRIPTION

The CP1600/CP1610 are compatible members of the Series 1600 Microprocessor products family. Each is a complete, 16-bit, single chip, high speed MOS-LSI Microprocessor. The Series 1600 family is fabricated with General Instrument's N-Channel Ion-Implant process, insuring high performance with proven reliability and production history. All members of the Series 1600 family are fully compatible with the CP1600/CP1610.

The Microprocessor has been designed for high speed data processing and real time applications. Typical applications include programmable TV games, home computer systems/home information centers, programmable calculator systems, peripheral controllers, process controllers, intelligent terminals and instruments, data acquisition and digital communications processors, numerical control systems and many general purpose mini-computer applications.The Microprocessor can readily support a variety of peripheral equipment such as TTY, CRT display, tape reader/punch, A/D & D/A converter, keyboard, cassette tape, floppy disk, and RS-232C data communication lines.

The CP1600/CP1610 utilize third generation minicomputer architecture with eight general purpose registers to achieve a versatile, sophisticated microcomputer system. The 16-bit word enables fast and efficient processing of alphanumeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of program memory, data memory, or peripheral devices. This single address space concept, combined with a powerful instruction set, provides an efficient solution to microcomputer and many minicomputer-based product requirements.

CP1600 SYSTEM DIAGRAM



PROCESSOR SIGNALS

DATA BUS

D0-D15
Input/Output/High Impedance

Data 0-15: 16-bit bidirectional bus used to transfer data, addresses, and instructions between the microprocessor, memory, and peripheral devices.

PROCESSOR CONTROL

$\overline{\text{STPST}}$
Input
STop-STart: Edge-triggered by negative transition; used to control the running condition of the microprocessor.

HALT
Output
HALT: indicates that the microprocessor is in a stopped mode.

$\overline{\text{MSYNC}}$
Input
Master SYNC: Active low input synchronizes the microprocessor to the $\phi 1$, $\phi 2$ clocks during power-up initialization.

EBCA 0-3
Outputs
External Branch Condition Addresses 0-3: Address for one-of-16 external digital state tests via the BEXT (Branch on EXTernal) instruction.

EBCI
Input
External Branch Condition Input: Return signal from the one-of-16 selection made by EBCA 0-3.

BUS CONTROL

BDIR, BC1, BC2
Outputs
Bus DIRection, Bus Controls 1, 2: Bus control signals externally decoded to define the state of bus operations (see State Flow Diagram).

$\overline{\text{BUSRQ}}$
Input

$\overline{\text{BUSAK}}$
Output
BUS ReQuest, BUS AcKnowledge: BUSRQ* requests the microprocessor to relinquish control of the bus indefinitely. BUSAK* informs devices that the bus has been released.

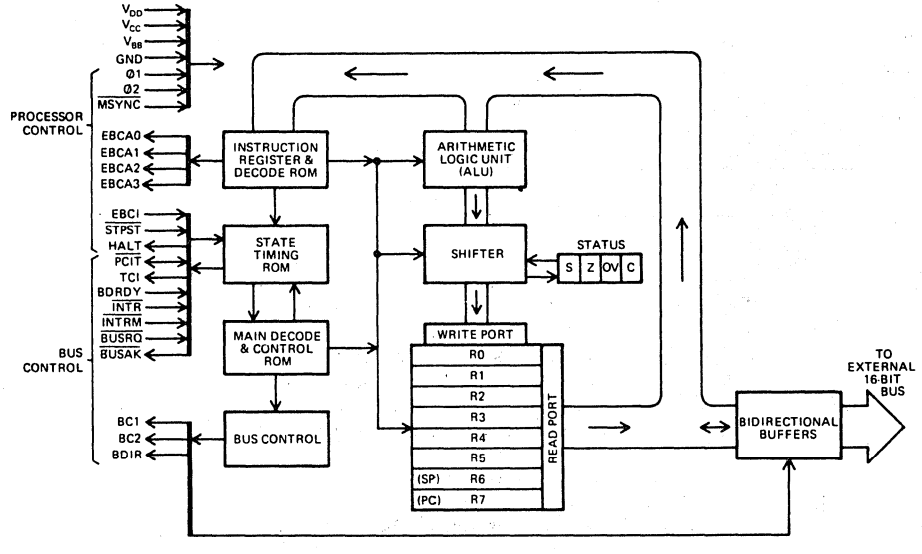
BDRDY
Input
Bus Data ReaDY: causes the microprocessor to "wait" and resynchronize to slow memory and peripheral devices.

$\overline{\text{INTR}}$, $\overline{\text{INTRM}}$
INTeRupt, INTeRupt Masked: request the microprocessor to service an interrupt upon completion of current instruction.

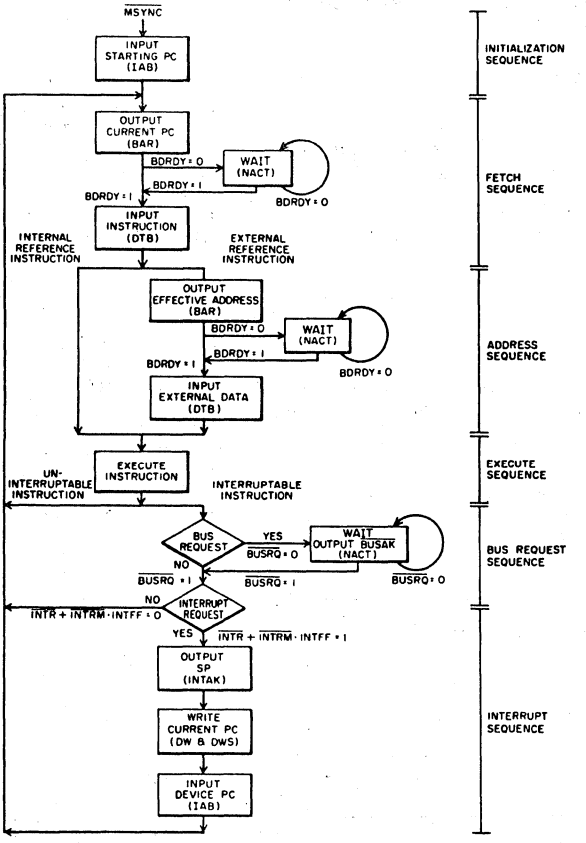
TCI
Output
Terminate Current Interrupt: pulse outputted by the microprocessor in response to the TCI instruction.

$\overline{\text{PCIT}}$
Input/output
Program Counter Inhibit/Trap: As an input, inhibits incrementation of the Program Counter during the instruction fetch sequence. As an output, generates a pulse during execution of a Software INterrupt (SIN) instruction.

CP1600 INTERNAL BLOCK DIAGRAM



SIMPLIFIED STATE FLOW DIAGRAM



BUS CONTROL SIGNALS

BDIR	BC2	BC1	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = high impedance
0	0	1	ADAR	Address Data to Address Register, D0-D15 = high impedance
0	1	0	IAB	Interrupt Address to Bus, D0-D15 = Input
0	1	1	DTB	Data To Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DW	Data Write
1	1	0	DWS	Data Write Strobe
1	1	1	INTAK	INTerrupt AcKnowledge

INSTRUCTION SET (SUMMARY LISTING)

		Mnemonics	Operation	Microcycles				Comments
INTERNAL REFERENCE INSTRUCTIONS	Register to Register	MOVR	MOVe Register	6/7				
		TSTR	TeST Register	6/7				MOVR to itself
		JR	Jump to address in Register	7				MOVR to PC
		ADDR	ADD contents of Registers	6				
		SUBR	SUBtract contents of Registers	6				
		CMPR	CoMPare Registers by subtr.	6				Results not stored
		ANDR	logical AND Registers	6				
		XORR	eXclusive OR Registers	6				
		CLRR	CLeaR Register	6				XORR with itself
	Single Register	INCR	INCrement Register	6				
		DECR	DECrement Register	6				
		COMR	COMplement Register	6				One's Complement
		NEGR	NEGate Register	6				Two's Complement
		ADCR	ADd Carry Bit to Register	6				
		GSWD	Get Status WorD	6				
		NOP	No OPeration	6				
		SIN	Software INterrupt	6				Pulse to $\overline{PCIT}$ pin
		RSWD	Return Status WorD	6				
	Register Shift	SWAP	SWAP 8-bit bytes	6			Add two cycles for 2-position shift.	Not interruptable. One or two position shift capability. Two position SWAP not supported.
		SLL	Shift Logical Left	6				
		RLC	Rotate Left thru Carry	6				
		SLLC	Shift Logical Left thru Carry	6				
		SLR	Shift Logical Right	6				
		SAR	Shift Arithmetic Right	6				
		RRC	Rotate Right thru Carry	6				
		SARC	Shift Arithmetic Right thru Carry	6				
	Control Instructions	HLT	HaLT	4				
		SDBD	Set Double Byte Data	4				Must precede external reference to double byte data
		EIS	Enable Interrupt System	4				
		DIS	Disable Interrupt System	4				
		TCI	Terminate Current Interrupt	4				Not interruptable
		CLRC	CLeaR Carry to zero	4				
		SETC	SET Carry to one	4				
	Jump Instructions	J	Jump	12				
		JE	Jump, Enable, interrupt	12				
		JD	Jump, Disable interrupt	12				
		JSR	Jump, Save Return	12				Return Address saved in R4, 5 or 6.
		JSRE	Jump, Save Return & Enable	12				
		JSRD	Jump, Save Return & Disable interrupt	12				
EXTERNAL REFERENCE INSTRUCTIONS	Conditional Branch Instructions	B	unconditional Branch	9*			Add 2 cycles if test condition is true, except *	
		NOPP	No OPeration	7*				Two words
		BC (BLGE)	Branch on Carry	7				C=1
		BNC (BLLT)	Branch on No Carry	7				C=0
		BOV	Branch on OVerflow	7				OV=1
		BNOV	Branch on No OVerflow	7				OV=0
		BPL	Branch on PLus	7				S=0
		BMI	Branch on Minus	7				S=1
		BZE (BEQ)	Branch on ZEro or EQual	7				Z=1
		BNZE (BNEQ)	Branch if Not ZEro or Not EQual	7				Z=0
		BLT	Branch if Less Than	7				S∀OV=1
		BGE	Branch if Greater than or Equal	7				S∀OV=0
		BLE	Branch if Less than or Equal	7				ZV(S∀OV)=1
		BGT	Branch if Greater Than	7				ZV(S∀OV)=0
		BUSC	Branch if Sign≠Carry	7				C∀S=1
		BESC	Branch if Sign=Carry	7				C∀S=0
		BEXT	Branch if External condition is True	7				4 LSB of instruction are decoded select 1 of 16 external conditions.
				Dir.	Imm.	Indir.	Stack	
	I/O	MVO	MoVe Out	11	9	9	9	Not interruptable
		PSHR	PuSH Register to stack	—	—	—	9	PSHR=MVO@R6. Not interruptable
		MVI	MoVe In	10	8	8	11	
		PULR	PULl from stack to Register	—	—	—	11	PULR=MVI@R6.
	Arithmetic & Logic	ADD	ADD	10	8	8	11	
		SUB	SUBtract	10	8	8	11	
		CMP	CoMPare	10	8	8	11	Result not saved
		AND	logical AND	10	8	8	11	
		XOR	eXclusive OR	10	8	8	11	

Displacement in PC+1
PC←PC±Displacement

1 MICROCYCLE=2 CLOCK CYCLES

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD}, V_{CC}, GND and all other input/output voltages with respect to V_{BB} . . . . . −0.3V to +18.0V
Storage Temperature . . . . . −55°C to +150°C
Operating Temperature . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions: (unless otherwise noted)

V_{DD}=+12V±5%, 70mA(typ), 110mA(max.) V_{BB}= −3V±10%, 0.2mA(typ), 2mA(max.)
V_{CC}=+5V±5%, 12mA(typ), 25mA(max.) Operating Temperature (T_A)=0°C to +70°C

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
High	V_{IHC}	10.4	—	V_{DD}	V	
Low	V_{ILC}	0	—	0.6	V	
Input Current	I_C	—	—	15	mA	$V_{IHC}=(V_{DD}-1)V$
Logic Inputs						
Low	V_{IL}	0	—	0.65	V	
High (All Lines except BDRDY)	V_{IH}	2.4	—	V_{CC}	V	
High (Bus Data Ready Line See Note)	V_{IHB}	3.0	—	V_{CC}	V	
Logic Outputs						
High	V_{OH}	2.4	V_{CC}	—	V	I_{OH} = 100μA
Low (Data Bus Lines D0-D15)	V_{OL}	—	—	0.5	V	I_{OL} = 1.6mA
Low (Bus Control Lines, BC1,BC2,BDIR)	V_{OL}	—	—	0.45	V	I_{OL} = 2.0mA
Low (All Others)	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
AC CHARACTERISTICS						
Clock Pulse Inputs, φ1 or φ2						
Pulse Width	$t_{\phi 2}$, $t_{\phi 2}$	120		—	ns	
Skew (φ1, φ2 delay)	t_{12}, t_{21}	0	—	—	ns	
Clock Period	t_{CY}	0.3	—	2.0	μs	
Rise & Fall Times	tr, tf	—	—	15	ns	
Master SYNC:						
Delay from φ	tms	—	—	30	ns	
D0-D15 Bus Signals						
Output delay from φ1 (float to output)	t_{BO}	—	—	120	ns	1 TTL Load & 25 pF
Output delay from φ2 (output to float)	t_{BF}	—	50	—	ns	
Input setup time before φ1	t_{B1}	0	—	—	ns	
Input hold time after φ1	t_{B2}	10	—	—	ns	
Bus Control Signals BC1,BC2,BDIR						
Output delay from φ1	t_{DC}	—	—	120	ns	
Skew	—	—	—	30	ns	
BUSAK Output delay from φ1	t_{BU}	—	150	—	ns	
TCI Output delay from φ1	t_{TO}	—	200	—	ns	
TCI Pulse Width	t_{TW}	—	300	—	ns	
EBCA output delay from BEXT input	t_{DE}	—	—	150	ns	
EBCA wait time for EBCI input	t_{AI}	—	—	400	ns	
CAPACITANCE						TA = +25°C; V_{DD} = +12V; V_{CC} = +5V; V_{BB} = −3V; $t\phi 1 = t\phi 2$ = 120ns
φ1, φ2 Clock Input capacitance	Cφ1, Cφ2	—	20	30	pF	
D0-D15	—	—	8	15	pF	
All Other	—	—	5	10	pF	

**Typical values are at +25°C and nominal voltages.

NOTE: The Bus Data ReaDY(BDRDY) line is sampled during time period TSI after a BAR or ADAR bus control signal. BDRDY must go low requesting a wait state 50 ns before the end of TS1 and remain low for 50 ns minimum. BDRDY may go high asynchronously. In response to BDRDY, the CPU will extend bus cycles by adding additional microcycles up to a maximum of 40 μsec duration.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD}, V_{CC}, GND and all other input/output voltages with respect to V_{BB} . . . . . −0.3V to +18.0V
Storage Temperature . . . . . −55°C to +150°C
Operating Temperature . . . . . 0°C to +70°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

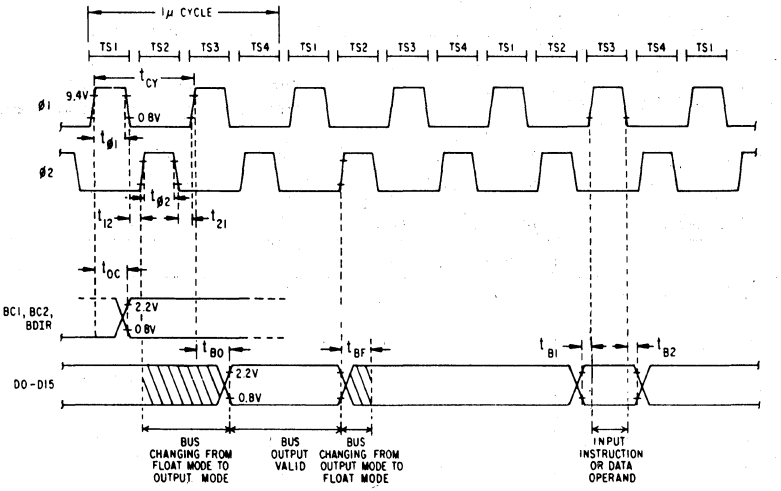
Standard Conditions: (unless otherwise noted)
V_{DD}=+11V±5%, 70mA(typ), 110mA(max.) V_{BB} = −2.2V ± 5%, 0.2mA(typ), 2mA(max.)
V_{CC}=+5V±5%, 12mA(typ), 25mA(max.) Operating Temperature (T_A)=0°C to +70°C

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
High	V_{IHC}	10.0	–	V_{DD}	V	
Low	V_{ILC}	0	–	0.6	V	
Input current	—	—	—	15	mA	$V_{IHC} = (V_{DD} - 1)V$
Logic Inputs						
Low	V_{IL}	0	–	0.65	V	
High (All Lines except BDRDY)	V_{IH}	2.4	–	V_{CC}	V	
High (Bus Data Ready Line See Note)	V_{IHB}	3.0	–	V_{CC}	V	
Logic Outputs						
High	V_{OH}	2.4	V_{CC}	—	V	I_{OH} = 100μA
Low (Data Bus Lines D0-D15)	V_{OL}	–	–	0.5	V	I_{OL} = 1.6mA
Low (Bus Control Lines, BC1,BC2,BDIR)	V_{OL}	–	–	0.45	V	I_{OL} = 2.0mA
Low (All Others)	V_{OL}	–	–	0.45	V	I_{OL} = 1.6mA
AC CHARACTERISTICS						
Clock Pulse Inputs, φ1 or φ2						
Pulse Width	$t_{\phi 2}$, $t_{\phi 2}$	250		–	ns	
Skew (φ1, φ2 delay)	t_{12}, t_{21}	0	–	–	ns	
Clock Period	t_{cy}	0.5	–	2.0	μs	
Rise & Fall Times	tr, tf	–	–	15	ns	
Master SYNC:						
Delay from φ	tms	–	–	30	ns	
D0-D15 Bus Signals						
Output delay from φ1 (float to output)	t_{BO}	–	–	100	ns	1 TTL Load & 100pF
Output delay from φ2 (output to float)	t_{BF}	–	50	–	ns	
Input setup time before φ1	t_{B1}	0	–	–	ns	
Input hold time after φ1	t_{B2}	10	–	–	ns	
Bus Control Signals BC1,BC2,BDIR						
Output delay from φ1	t_{DC}	–	–	100	ns	
Skew	—	—	—	30	ns	
BUSAK Output delay from φ1	t_{BU}	–	150	–	ns	
TCI Output delay from φ1	t_{TO}	–	200	–	ns	
TCI Pulse Width	t_{TW}	–	300	–	ns	
EBCA output delay from BEXT input	t_{DE}	–	–	150	ns	
EBCA wait time for EBCI input	t_{AI}	–	–	400	ns	
CAPACITANCE						TA = +25°C; V_{DD} = +12V; V_{CC} = +5V; V_{BB} = −3V; tφ1 = tφ2 = 120ns
φ1, φ2 Clock Input capacitance	Cφ1, Cφ2	—	20	30	pF	
D0-D15	—	—	8	15	pF	
All Other	—	—	5	10	pF	

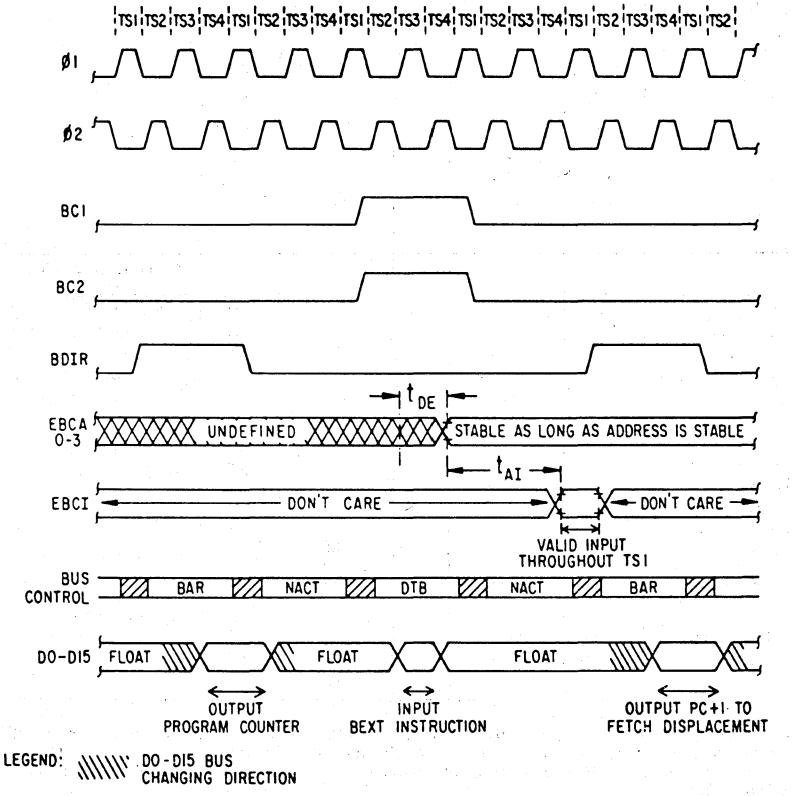
**Typical values are at +25°C and nominal voltages.

NOTE: The Bus Data ReaDY(BDRDY) line is sampled during time period TSI after a BAR or ADAR bus control signal. BDRDY must go low requesting a wait state 50 ns before the end of TS1 and remain low for 50 ns minimum. BDRDY may go high asynchronously. In response to BDRDY, the CPU will extend bus cycles by adding additional microcycles up to a maximum of 40 μsec duration.

CLOCK AND BUS TIMING



TYPICAL INSTRUCTION SEQUENCE (EXTERNAL BRANCH TIMING)



Dual Digital to Analog Converter

DESCRIPTION

The DAC1600 Digital to Analog Converter has been designed to serve as a powerful, yet economic interface to a process control loop. The DAC1600 provides two 10-bit Pulse Width Modulated outputs and an array of switch inputs and light driver outputs. Essentially the DAC1600 contains four registers which can be loaded or read through a 10-bit I/O data port. Fig. 1 shows the data base information in these registers.

ANALOG OUTPUTS

The value of the analog outputs SP and VO are determined respectively by the ten-bit numbers loaded in the Set Point Register and the Valve Register. An output is a pulse train with a period of approximately 1kHz (1MHz/1024) whose high/low ratio is inversely related to the 10-bit value stored in the register. (See Fig. 2).

The high/low ratio is unaffected by temperature and supply variations and is the basis of the 10-bit D/A accuracy. The length of the high or low portions of the pulse will never be in error by more than a fraction of an LSB.

If the chip output (SP or VO) is passed through a low pass filter the result will be approximately equal to the desired analog voltage. However, it will not be accurate because, while the output ratio is accurate, the chip's output voltage levels are not, and would thereby degrade the accuracy of the signal. The chip's output should be used to drive a good switch which, in conjunction with a voltage reference and filtering will yield an analog voltage having 10-bit accuracy.

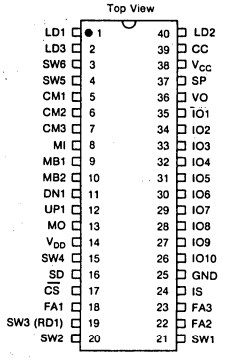
VALVE REGISTER (Manual Mode)

In addition to being a register, the Valve Register (B) is also an UP/DOWN counter. By setting MI (Manual Interrupt) to a "1" and either UP or DN to a "1", the B register will be slewed up or down. This allows an operator to manually adjust the B register value. The design allows bumpless, balanceless transfers between computer and manual control. In order to provide both a precise degree of manual control and an ability to slew the B register through a substantial change, a variable slewing rate has been incorporated in the chip.

PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View



MODE REGISTER

The first five bits of Mode Register (A) may be used to store the mode of control. Manual Interrupt is in bit 1. Bits M2, M3, M4 and M5 can be read or loaded via the I/O bus or set by inputs from three switch inputs CM1, CM2, or CM3. The condition of these bits is encoded and output on light drivers MB1 and MB2. The Mode Register may be used to inform the operator of computer determined conditions or inform the computer of operator actions.

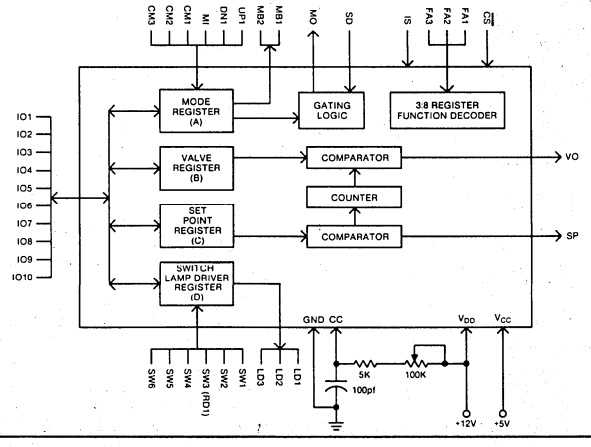
SWITCH/LAMP DRIVER REGISTER

The Switch/Lamp Driver Register contains three light drivers which can be used for panel alarm lights. It also stores six switch inputs.

ADDITIONAL ALARM FEATURE

Light driver M0 outputs a 2 cps signal which can flash a light to attract an operator's attention.

BLOCK DIAGRAM



PIN FUNCTIONS

I01-10: 10 bit bidirectional data bus. Data can be loaded synchronously or asynchronously. Data are read onto the I/O bus without strobing.

MI: Manual input line. It forces the chip into a manual mode of operation.

$\overline{CS}$: Chip select line. It is low active for synchronous data transfer, high active for asynchronous data transfer.

IS: Input strobe line. It loads one of the four internal registers defined by FA1-3, when $\overline{CS}$ is low. If the chip is in the manual mode via MI, the ability to load one of the four registers, namely, the valve register, is unconditionally inhibited independent of the $\overline{CS}$ signal.

FA1-3: Function select lines. It is used to specify one of the four registers and whether an input or output function is to be performed. See Table 2 for definition.

CM1-3: Control mode lines. A pulse on one of these lines will alter the bit M3, M4 or M5 in the mode register. See Table 3.

UP1, DN1, RD1: Up counting, down counting and reversing lines. They are used to control the direction of counting serially in the valve register during the manual mode. Overflow or underflow of the register is prevented by internal circuitry. See Table 4 for definition.

SD: DAC1600 shed signal. It is used in conjunction with manual input line to form different manual mode outputs. See Table 5.

MO: DAC1600 manual mode output. It oscillates around 2Hz whenever MI is low and SD is high. See Table 5.

MB1, MB2: Mode bit-lines. They are used to indicate the status of the mode register. See Table 6.

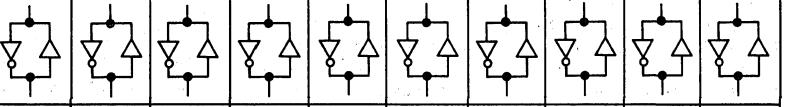
VO: Valve register output. It is a 10 bit pulse width modulated waveform. See Fig. 2

SP: Set point register output. It is a 10 bit pulse width modulated waveform. See Fig. 2.

CC: DAC1600 counter clock input.

SW1-SW6: They are used by CPU as switch word. SW3 (RD1) is also used in reversing the direction of counting in valve register during manual mode.

LD1-LD3: Panel lamp driver outputs.

	IO-10	IO-9	IO-8	IO-7	IO-6	IO-5	IO-4	IO-3	IO-2	IO-1
I/O Buffer										
Register A (mode register)	1	1	1	UP1+	DN1+	M5	M4	M3	M2	M1+
Register B (valve register)	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1
Register C (set point register)	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1
Register D (switch/lamp driver register)	0	SW1+	SW2+	SW3+	SW4+	SW5+	SW6+	LD3	LD2	LD1

+Read only locations (asynchronous input signals)

Fig. 1 REGISTERS DATA BASE

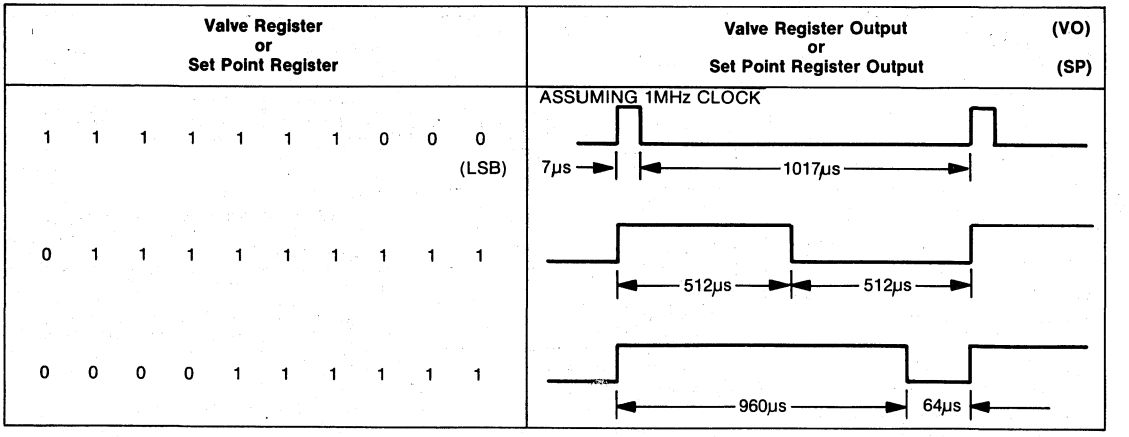


Fig. 2 PULSE WIDTH MODULATED OUTPUT WAVEFORMS

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS*

V_{DD}, V_{CC} and all other input/output voltages with respect to GND ..... −0.3V to +18.0V

Storage Temperature ..... −55°C to +150°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted) T_A = 0°C to 75°C V_{DD} = +12V ±5% V_{CC} = +5V ±5%

Symbol	Characteristic	Min.	Max	Units	Conditions
V_{IL}	Input Low Voltage	-0.5	+0.65	V	*
V_{IH}	Input High Voltage	2.2	V_{CC}	V	*
I_{IN}	Input Current	—	' 10	µA	V_{IN} = 0V to 5.25V
I_{LOH}	Output Lkg. Curr.	—	10	µA	$\overline{CS}$ = 2.2V IO (1-10) = 4.0V
I_{LOL}	Output Lkg. Curr.	—	-10	µA	$\overline{CS}$ = 2.2V; V_{CC} = 5.25 V; IO (1-10) = 0.4V
C_{IN}	Input Capac	—	8	pF	f = 1MHz
C_{OUT}	Output Capac	—	10	pF	f = 1MHz @ V_{OUT} = 0.0V Tri-State Mode
V_{OL}	Output Low Voltage	—	0.45	V	*I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.7	V_{CC}	V	*I_{OH} = 300µA, C_L = 100pF
I_{CC}	Supply Current	—	5	mA	
I_{DD}	Supply Current	—	25	mA	No Load

* Applies to TTL compatible inputs and outputs. See Table 1 for other inputs and outputs.

Table 1: THE FOLLOWING TABLE DEFINES INTERNAL PULL UP CURRENT SOURCES

Signal	In / Out	Pull Up	Comp	Loading
FA1,2,3	In	To +5V	TTL	⩽1ma @ .4V
LD1	Out	—	—	Load Type A
LD2	Out	—	—	Load Type A
MI	In	None	Comp Type 1	
M0	Out	—	—	Load Type A
CM1	In	None	Comp Type 1	
CM2	In	None	Comp Type 1	
CM3	In	None	Comp Type 1	
MB1	Out	—	—	Load Type A
MB2	Out	—	—	Load Type A
SW3 (RD1)	In	To +5V	TTL	⩽1ma @ .4V
SW2	In	To +5V	TTL	⩽1ma @ .4V
SW1	In	To +5V	TTL	⩽1ma @ .4V
V0	Out	—	—	Load Type B
SP	Out	—	—	Load Type A
UP1	In	None	Comp Type 1	
SW5	In	None	Comp Type 1	
DN1	In	None	Comp Type 1	
SW6	In	None	Comp Type 1	
SW4	In	None	Comp Type 1	
LD3	Out	—	—	Load Type A
SD	In	To +5V	TTL	⩽1ma @ .4V
CC	In	Series RC to Common		
IS	In	To +5V	TTL	⩽1ma @ .4V
$\overline{CS}$	In	To +5V	TTL	⩽1ma @ .4V
I01, -10	In/Out	Tri State	—	Load Type C

COMPATIBILITY

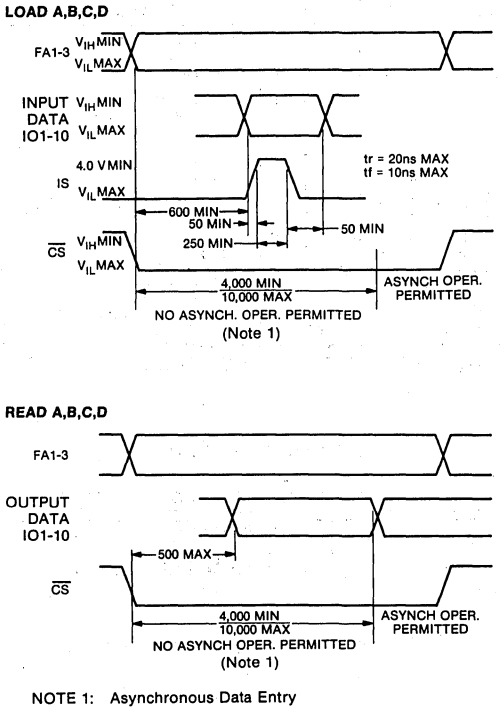
Comp. Type 1 — High ..... 4V to 12V; Low 0.4V

LOADING

Load Type A — Source ..... 2.5 mA @ 4V Min; Sink ..... 300 µA @ 0.4V Max

Load Type B — Source ..... 10 µA @ 9V Min; Sink ..... 1mA @ 1.2V Max

Load Type C — Sink ..... 1.6 mA 0.45V Max; Source ..... 300 µA @ 2.7V Min; Cap ..... 100 pF Max Load



NOTE 1: Asynchronous Data Entry

Data transfer in and out of the chip is made via the 10-bit bidirectional data bus (I/O 1-10). Data may also be entered asynchronously with respect to $\overline{CS}$ and IS. Asynchrous data entry during I/O data transfers is inhibited by an internal "lockout" signal derived from the $\overline{CS}$ signal. When $\overline{CS}$ falls to zero, a delay of from 4µs to 10µs is generated. Asynchronous inputs are inhibited from entry during this time.

Fig. 3 TIMING DIAGRAM

Table 2 REGISTER AND FUNCTION SELECT

FA				
3	2	1	Operation	Condition
0	0	0	Load 'A'	
0	0	1	Load 'B'	MI+ = 0
0	1	0	Load 'C'	
0	1	1	Load 'D'	
1	0	0	Read 'A'	
1	0	1	Read 'B'	
1	1	0	Read 'C'	
1	1	1	Read 'D'	

Table 3 MODE CONTROL

CM						
3	2	1	M5	M4	M3	M2
		⎍	1	0	0	0
	⎍		0	1	0	0
⎍			0	0	1	0

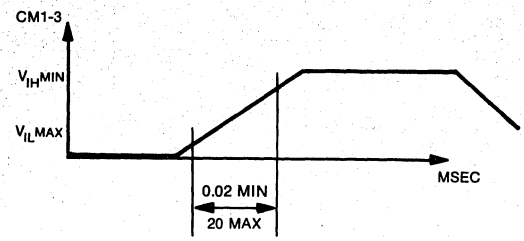


Table 4 MANUAL MODE FUNCTION CONTROL

MI	$\overline{CS}$	UP1	DN1	RDI	Operation
1	1	0	0	0	No Op
1	1	0	0	1	No Op.
1	1	0	1	0	Incr "B"
1	1	0	1	1	Decr "B"
1	1	1	0	0	Decr "B"
1	1	1	0	1	Incr "B"
1	1	1	1	0	Indeterminate
1	1	1	1	1	Indeterminate
1	0*	X	X	X	No Op.
0	0	X	X	X	As specified by FA1-3
0	1	X	X	X	No Op.

INCR/DECR speed is controlled by an internal variable frequency clock. The clocking rates are as follows:

16Hz for 2 seconds
64Hz for 2 seconds
128Hz thereafter until UP1 or DN1 are deactivated.

*If $\overline{CS}$ remains low for longer than 10 μsec. normal operation (per UP/DN) will resume.

Table 5 MANUAL MODE OUTPUT

MI	SD	MO
0	0	0
0	1	⎍⎍⎍⎍ f = 2Hz
1	0	1
1	1	1

Table 6 MODE REGISTER STATUS

				MB	
M5	M4	M3	M2	2	1
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

Input/Output Buffer

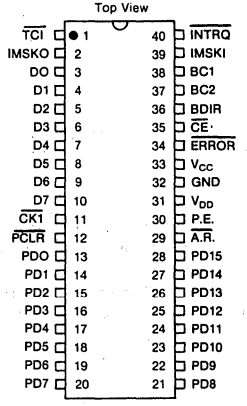
FEATURES

- Single 16-Bit Port or Dual 8-Bit Ports for Bidirectional Input/Output
- Parity Check Logic on Both Ports
- Three Levels of Priority Interrupt Logic
- 'Real Time' Presetable 16-Bit Timer
- Capability to Monitor Peripheral Error Status
- Three Interrupt Vectors for Error, I/O and Timer
- Automatic Handshake Logic and Signals
- Control Register
- TTL Compatible

PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View

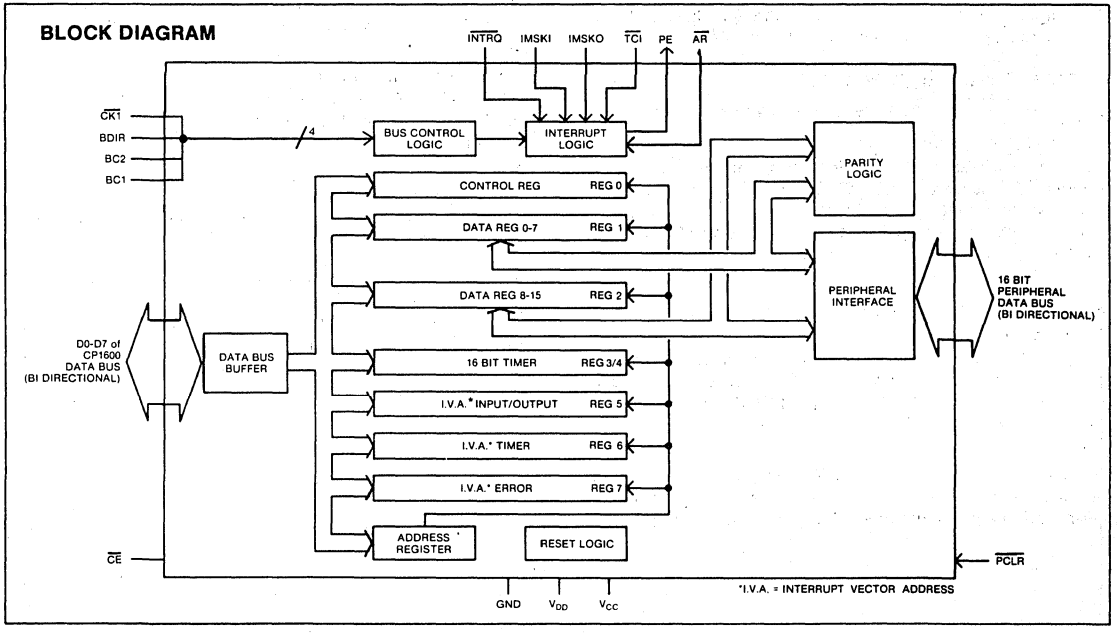


DESCRIPTION

The IOB1680 is a byte oriented programmable input/output buffer which provides comprehensive interfacing facilities for the CP1600 microprocessor with a minimum of additional components. The circuit is fabricated in General Instrument N-Channel Ion Implant GIANT II process insuring high performance with proven reliability and production history.

The IOB1680 enables efficient interfacing between a peripheral and the CP1600 by the use of six 8-bit registers and a 16-bit programmable timer. Two of the 8-bit registers are a buffer store between the CP1600 and the bidirectional I/O lines to peripheral, latching any data sent to them from the CP1600. Three other 8-bit registers hold the Interrupt Vector Addresses associated with I/O, Error Status and the Timer. The Control Register governs the operation and characteristics of the IOB1680 and provides a convenient means for the CP1600 to monitor I/O status information. The 16-bit timer gives the IOB1680 a real time capability which is suitable for confirming system security and for timing peripheral activities. These registers are initialized after power clear by the CP1600 program writing the required interrupt vector addresses into the appropriate registers. The interrupt vectors may also be altered at any time by program.

BLOCK DIAGRAM



IOB1680/CP1600 SIGNALS

Data Bus:

D0-D7 (Input/Output/High Impedance)
DATA 0-7: The bidirectional data lines D0-D7 are used to transmit data and address information between the Series 1600 Microprocessors and the IOB1680. These correspond to the lower 8-bits of the Series 1600 Microprocessor's data bus. These data lines have tristate capability, being in the high impedance state except when transferring data or status information from the IOB1680 under control of the control bus signals BDIR, BC1 and BC2.

Bus Control Signals

BDIR, BC1, BC2 (Inputs)
Bus DIRection, Bus Control 1 and 2: Bus control signals from the CP1600 which define the state of data bus operations. These signals are decoded internally by the IOB1680 to control its operation.

$\overline{TCI}$ (Input)
Terminate Current Interrupt: A pulse output by the CP1600 in response to the TCI instruction to indicate the end of the current interrupt service routine.

$\overline{INTRQ}$ (Output)
INTerrupt ReQuest: This output is pulled low to a logic '0' by the IOB1680 to request an interrupt from the series 1600 Microprocessor. This is an open drain output capable of sinking 1.6mA with an output voltage 0.5V. Because of the open drain feature the $\overline{INTRQ}$ output of several IOB1680s can be wired ORed together.

$\overline{CK1}$ (Input)
ClocK 1: This clock defines when the bus control signals BDIR, BC1 and BC2 are valid and is used in the IOB1680 to strobe their decode signals. It is also used to increment the timer.

$\overline{CE}$ (Input)
Chip Enable: This low true address input enables the IOB1680 for data read and write operations.

IMSKI/MSK0 (Input/Output)
Interrupt MaSK In, Interrupt MaSK Out: These two signals are used to form the interrupt priority daisy chain and prevent a lower priority device from requesting an interrupt while a higher device is being serviced. The IMSKI input of the IOB1680 which is to have highest priority must be connected to GND.

IOB1680 PERIPHERAL SIGNALS

Data

PD0-PD15 (Input/Output)
Peripheral Data 0-15: Communication of data to and from the peripheral device is via this 16 bit highway. Each output can sink 1.6mA for an output voltage of 0.5V. In the high state each output can source 100μA. These lines can be used as wire ORed inputs by 'pulling down' the line to a logic '0' sinking the 100μA externally.

Peripheral Control Signals:

PE (Output)
Peripheral Enable: This output is a function of the Ready bit of the control register. When it is at a logic '0' no action is required by the peripheral, a '1' indicates that peripheral activity has been requested by the CP1600.

$\overline{AR}$ (Input)
Attention Request: This input from the peripheral device is normally high at a logic '1' and is taken low to a logic '0' by the peripheral to request attention. This edge triggers the Ready bit of the control register forcing it to a logic "1", causing an interrupt request to be made via the $\overline{INTRQ}$ output if the peripheral interrupt enable bit of the control register is set. If the interrupt is disabled the Ready bit of the control register can be used in 'polling' handshake routines.

$\overline{ERROR}$ (Input)
ERROR: The error status of the peripheral is indicated by this input; being low indicating an error condition, e.g. tape low.

$\overline{PCLR}$ (Input)
Power CLeaR: Initializes registers.

INTERNAL CONTROL SIGNALS

Control Register:

The Control Register can be written and read under program control. The function of the individual bits are:

Bit 7—Parity Status for Peripheral Data 0-7:
The parity of the low order byte of the Peripheral Data bus is indicated by this Control bit, a logic '1' indicates even parity while a '0' indicates odd.

Bit 6—Parity Status for Peripheral Data 8-15:
Similar to bit 7, but indicates the parity of the high order byte of Peripheral Data.

Bit 5—Timer Clock Enable (TCE):
The clock to the 16-bit timer is controlled via TCE, the clock is enabled by setting TCE to a logic '1'. The timer can only request an interrupt when its clock is enabled by TCE.

Bit 4—Timer Interrupt Enable (TIE):
For the timer to cause an interrupt request on the $\overline{INTRQ}$ output TIE must be set to a logic '1', a '0' disables the timer interrupt logic.

Bit 3—Peripheral Interrupt Enable (PIE):
PIE must be set to a logic '1' to enable interrupt requests on the $\overline{INTRQ}$ output as a result of peripheral Attention Request or Error Status conditions.

Bit 2—Data Width Select (DWSL):
The re-enabling of the peripheral by automatic handshake can be chosen to occur with 8 or 16-bits wide data; DWSL being an '0' indicates an 8-bit wide data word while a '1' indicates a sixteen bit wide data word.

Bit 1—Error Summary
The ERROR STATUS of the peripheral is indicated by this bit of the Control Register, being a logic '0' shows an error condition. This will cause an interrupt request on the $\overline{INTRQ}$ output if PIE is set to a '1'.

Bit 0—Ready
This READY bit indicates the operational status of the peripheral. When it is a logic '0' the peripheral is active while a logic '1' indicates that the peripheral is idle and requiring service. The $\overline{AR}$ input going low indicates to the Ready bit the end of a peripheral activity and thereby causes the Ready bit to be set. In this condition, if the PIE bit is set, an interrupt request results via the $\overline{INTRQ}$ output. Reading or writing to the Peripheral Data lines causes the resetting of this Ready bit re-enabling the peripheral activity.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and V_{CC} and all other input/output voltages with respect to GND ..... -0.3V to +18V
Storage Temperature ..... -55°C to +150°C
Operating Temperature ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

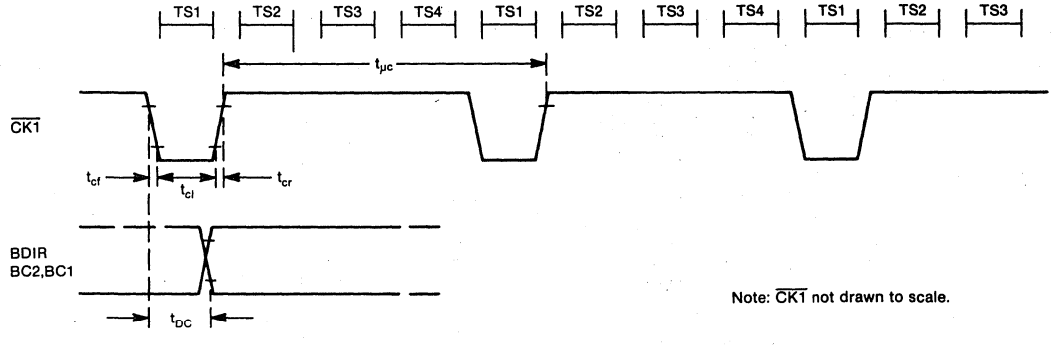
Standard Conditions (unless otherwise noted)

All voltages referenced to GND
V_{DD} = +12V ±5%
V_{CC} = +5V ±5%
Operating Temperature (T_A) = 0°C to +70°C

Characteristic		Symbol	Min	Typ**	Max	Unit	Condition
DC CHARACTERISTICS							
Clock Input:	High	V_{ihc}	2.4	—	V_{DD}	V	
	Low	V_{ilc}	0	—	.5	V	
Logic Inputs:	High	V_{ih}	2.4	—	V_{CC}	V	
	Low	V_{il}	0	—	.65	V	
Logic Outputs:	High	V_{oh}	2.4	V_{CC}	—	V	I_{oh} = 100μA
	Low	V_{ol}	—	—	.5	V	I_{ol} = 1.6mA
AC CHARACTERISTICS							
Clock Inputs							
$\overline{CK1}$	Clock period	tμc	0.4	—	4.0	μs	
	Clock width	tcl	70	—	—	ns	
	Rise & Fall times	tcr,tcf	—	—	10	ns	
CAPACITANCE (T_A = 25°C, V_{DD} = +12V, V_{CC} = +5V)							
Input Capacitance:	D0-D7	C_{in}	—	6	12	pF	V_{in} = 0V
	All others		—	5	10	pF	V_{in} = 0V
Output Capacitance:		C_{out}	—	8	15	pF	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



Note: $\overline{CK1}$ not drawn to scale.

CIRCUIT DESCRIPTION

This circuit is designed to provide all the data buffering and control functions required when interfacing the Series 1600 Microprocessor System to a simple peripheral device. Data is transferred to and from the peripheral on 16 bidirectional lines, each of which can be considered to be an input or output. The transfer of information with the CP1600 is accomplished via an 8-bit highway, the 16-bits being transferred as two 8-bit bytes. The register addresses are assigned CP1600 memory locations, as follows (N is an arbitrary starting address):

Register Address	Description
N	Control Register
N + 1	Data Register Low Order 8-bits
N + 2	Data Register High Order 8-bits
N + 3	Timer Low Order 8-bits
N + 4	Timer High Order 8-bits
N + 5	Peripheral Interrupt Address Vector
N + 6	Timer Interrupt Address Vector
N + 7	Error Interrupt Address Vector

8-Bit Data Registers

These two 8-bit registers are the buffer store between the CP1600 and the peripheral interface. These registers, when addressed, accept data from the CP1600 data bus during a Move Out (MVO) instruction to the peripheral lines on the IOB1680.

During a CP1600 Move In (MVI) instruction, the data present on the IOB1680 peripheral lines is transferred to the CP1600 data bus. If the registers have not been set to a '1' prior to the Move In instruction, the data read will be the wire OR of the peripheral data and that contained in the registers.

These two registers have consecutive word addresses N + 1 and N + 2. The high order byte is held in register N + 2.

16-Bit Binary Counter-Timer

This 16-bit down counter can be set under program control to give any count length up to 64K. Since only 8-bits are available to transfer data between the CP1600 and the IOB1680 the counter must be set as two 8-bit bytes, these bytes having word addresses N + 3 and N + 4. The clock for the timer is the Series 1600 Microprocessor System clock divided by 8. The clock input to the counter is enabled when the 'timer clock enable' bit of the control register is set to a '1', being disabled when this bit is reset to a '0'.

Everytime the count reaches zero the timer signals 'end of count' which will generate an interrupt request via the $\overline{\text{INTRQ}}$ output of the IOB1680 if both the 'timer interrupt enable' and 'timer clock enable' bits of the control register are both set to a '1'. The clock to the timer is still enabled after this interrupt request has been made and remains so even after it has been serviced, assuming that the service routine did not disable it by resetting the TCE bit of the control register. After requesting an interrupt therefore the counter begins from a count of 64K, giving the IOB1680 a Real Time Clock capability.

The timer has the lowest priority on the IOB1680 daisy chain. The peripheral error summary has the highest priority.

When the timer is set under program control the 'end of count' logic is reset clearing any previously unserviced interrupt requests from the timer. The acknowledge flip flop and the control register are unaffected.

It is not possible to read the 'current' state of the timer as it is counting in 'real time' and therefore asynchronously with any program running on the CP1600. A typical operating sequence is:

1. Load two bytes of counter.
2. Set 'timer interrupt enable' and 'timer count enable' bits of Control Register.

If an interrupt is required only once after the preset count the service routing would reset the 'timer clock enable' bit of the Control register disabling the timer clock and interrupt capability. If, however, the interrupt was required on a regular 'real time' basis then the service routine would leave the 'timer interrupt enable' and 'timer clock enable' bits set.

8-Bit Interrupt Vector Address Registers

The start address of the interrupt service routines for the error status, peripheral and timer are held in these three registers. The 8-bit Interrupt Vector Addresses are written into these registers during system initialization. When an interrupt request ($\overline{\text{INTRQ}}$), generated from the IOB1680 is acknowledged by an INTAK from the CP1600, the subsequent IAB signal on the control bus causes the contents of the appropriate interrupt vector address register to be strobed onto the lower 8-bits of the CP1600 data bus. This data is used as the program counter start address of the interrupt service routine.

The word addresses of these registers are N + 5, N +6 and N + 7. This corresponds to the peripheral, timer and error respectively.

Power Clear Status of Circuit

Reset logic sets the initial state of the chip upon application of Power Clear. In this condition the states of the on chip registers are:

(a) **Data Registers.**
These are set to a logic '1' so that the peripheral input/output interface is high at a logic '1', this allows the peripheral lines to be used as inputs without any setting up procedure.

(b) **Timer.**
This is set to its maximum count length of 64K, all bits set to a logic '1'.

(c) **Interrupt Vector Address Registers.**
These registers have all their bits reset to a '0' by the power on reset logic.

Control Register.

(i) Bit 0 - Ready. This bit is set to a logic '1' indicating that no activity is required by the peripheral.

(ii) Bit 1 - Error Summary. This is a hard wired input indicating the status of the peripheral and is unaffected by the power on reset logic.

(iii) Bit 2 - Data Width Select. This bit is reset to a logic '0', selecting the data width of the interface to be 8-bits.

(iv) Bit 3 - Peripheral Interrupt Enable.
Bit 4 - Timer Interrupt Enable.
Both bits 3 and 4 are reset to a '0' at power on, disabling interrupts from the peripheral, and the timer.

(v) Bit 5 - Timer Clock Enable. During power up this bit is reset to a logic '0' disabling the counter clock.

(vi) Bit 6 - Parity Data 8-15.
Bit 7 - Parity Data 0-7.
Both these bits will be at a logic '1' showing even parity as the data register bits are all set to a '1'. This assumes no inputs from the peripheral; if this is not so, these bits will settle to a state depending upon the wire OR condition of the data registers and the peripheral inputs.

Interrupt Logic

The interrupt priority of the peripheral error status, peripheral interface and the timer is established by a daisy chain. The peripheral error status has the highest priority and the timer the lowest.

If a number of IOB1680s are being used then they can be connected in a daisy chain using the signals IMSKI, IMSKO and $\overline{\text{TCI}}$ to define their priority. An interrupt request is made by the IOB1680 pulling down, to a logic '0', the $\overline{\text{INTRQ}}$ output. This output is open drain enabling wire OR capability. The acknowledgement to this request is an INTAK signal via the Series 1600 Microprocessor control bus. Each IOB1680 decodes this signal which sets an acknowledge flip flop in the interface of the interrupting device, causing the IMSKO output of that device to go to a '1'. This propagates to all lower priority devices causing their IMSKI inputs to go to a '1', thus disabling their interrupt capability.

When an IAB is valid on the control bus only the highest priority interrupting device must strobe its Interrupt Vector Address onto the Data Bus. Thus the IMSKI input of a device controls its IAB decode. The IAB signal is only enabled on the IOB1680 which has its IMSKI input at a logic '0' and its acknowledge flip flop set.

If two devices interrupt simultaneously they will both be acknowledged by an INTAK since this is decoded on each chip. However, the IMSKO output of the higher priority device going to a '1' will force the IMSKI input of the lower priority interrupting device to a '1'. The IMSKI input of the lower priority device being set to a '1' disables the IAB decode of the control bus thereby resolving simultaneous interrupts.

The negative edge of the TCI signal from Series 1600 Microprocessor resets the interrupt logic of the highest priority device whose interrupt logic has been set by an interrupt request and acknowledged by an INTAK.

The IMSKI/IMSKO daisy chain has a propagation delay which allows a maximum of eight IOB1680s to be daisy chained in series.

The IMSKI input to the highest priority device should be connected to Gnd.

Control Logic

The CP1600 control bus signals BDIR, BC1, BC2 are decoded to perform the internal control functions required.

Parity Logic

The peripheral interface is constantly monitored and the parity of bits 0-7 and 8-15 checked. Depending on the parity of these two words, bits 6 and 7 of the control register are updated. These bits can be conveniently accessed by the CP1600 for use in branch instructions.

Branching on Parity

Bits 6 and 7 of the IOB1680 Control register contain the parity status of the upper and lower eight bits of the peripheral interface respectively. The positioning enables the standard branch instructions of the CP1600 to be conveniently utilized. A typical example is:

```
MVI CTRLRS, R;Fetch Control Register
RLC R2, 2
BNC     ;Branch if lower eight bits have odd parity
BC      ;Branch if lower eight bits have even parity
BNOV    ;Branch if higher eight bits have odd parity
BOV     ;Branch if higher eight bits have even parity
```

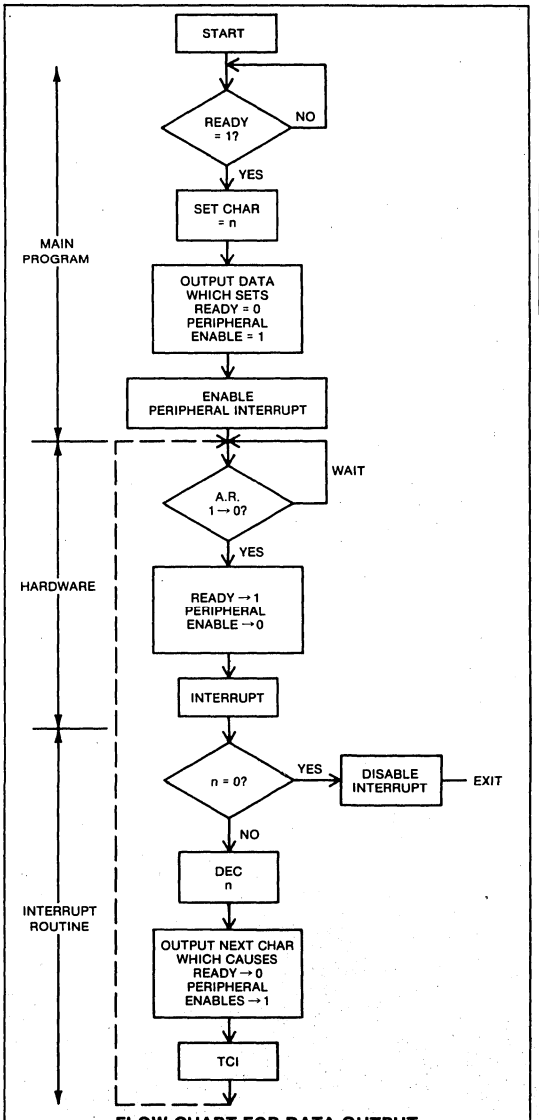
The IOB1680 as an Output Device

The power clear reset logic of the IOB1680 sets the $\overline{\text{Ready}}$ bit of the Control Register to a '1', causing the Peripheral Enable/$\overline{\text{Ready}}$ output to go to a '0', a condition that requires no activity from the peripheral. This power clear reset logic also disables the IOB1680's ability to request an interrupt on the status of the peripheral by resetting the Peripheral Interrupt Enable bit of the Control Register to a '0'.

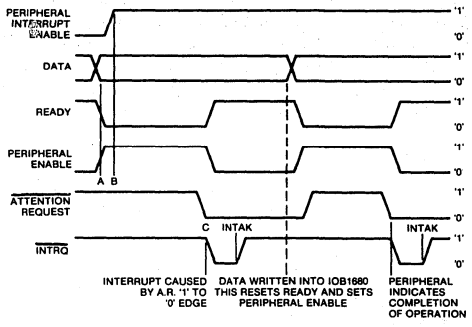
A flow chart for a typical output operation is shown to the right; the waveform diagram corresponding to this operation is also shown to the right.

The main program setting up the output operation would go through the following sequence of operations.

1. The Ready bit of the Control Register would be tested to ensure that the peripheral was indeed inactive. This would be so initially after power clear.
2. If condition (1) above is met, memory location CHAR of the CP1600 would be set to the number of output operations required. This is shown as 'SET CHAR = n'.
3. Send data from CP1600 to IOB1680 using MVO instruct. This operation resets the Ready bit to a '0' causing the Peripheral Enable/$\overline{\text{Ready}}$ output to go to a '1', requesting an operation by the peripheral device. This is shown at A in the waveform diagram.
4. The Peripheral Interrupt Enable (PIE) bit of the Control Register is now set to a '1' by programmer allowing the IOB1680 to request interrupts from the CP1600 via the INTRQ* output. Enabling the PIE bit after sending the data to the peripheral ensures that no 'false' interrupts are generated.
5. After the data has been sent to the peripheral (3) above, the IOB1680 hardware monitors the status of the Attention Request input. A '1' to '0' edge on the input sets the Ready bit to a '1' and the Peripheral Enable/$\overline{\text{Ready}}$ output to a '0', stopping the peripheral activity. The PIE bit and the Ready bit both being set to a '1' causes an interrupt request to be generated via the $\overline{\text{INTRQ}}$ output, if no higher priority devices are interrupting. Refer to C in the waveform diagram.
6. When the CP1600 accepts the interrupt it starts the interrupt sequence by issuing the INTAK acknowledge signal which resets the $\overline{\text{INTRQ}}$ output to its inactive state. The subsequent IAB signal causes the Interrupt Vector Address for the peripheral device to be strobed onto the data bus and then used as the start address for its service routine.
   Once entered, the service routine might go through the following sequence.
7. Decrement n, the number of output operations required (buffer length).
8. Test the resulting value n.
   (a) If it is zero the output operations are completed. Reset the PIE bit to disable the interrupt capability of the IOB1680 and EXIT.
   (b) If n is not zero output the next data to the IOB1680. This resets Ready to a '0' and Peripheral Interrupt Enable/$\overline{\text{Ready}}$ to a '1', re-enabling the peripheral activity automatically.
   The peripheral acknowledges this operation by returning the Attention Request input to a '1', the timing of this signal is not too critical as the it edge triggers the Ready bit of the control register by a 1-0 transition.
9. The interrupt is terminated by TCI instruction which resets the acknowledge flip flop in the IOB1680 interface logic.



FLOW CHART FOR DATA OUTPUT



TIMING DIAGRAM FOR MVO INSTRUCTION (Data from CP1600 to IOB1680)

The IOB1680 as an Input Device

The power clear status of the IOB1680 for input is the same as for output which is described under the section 'The IOB1680 as an Output Device'.

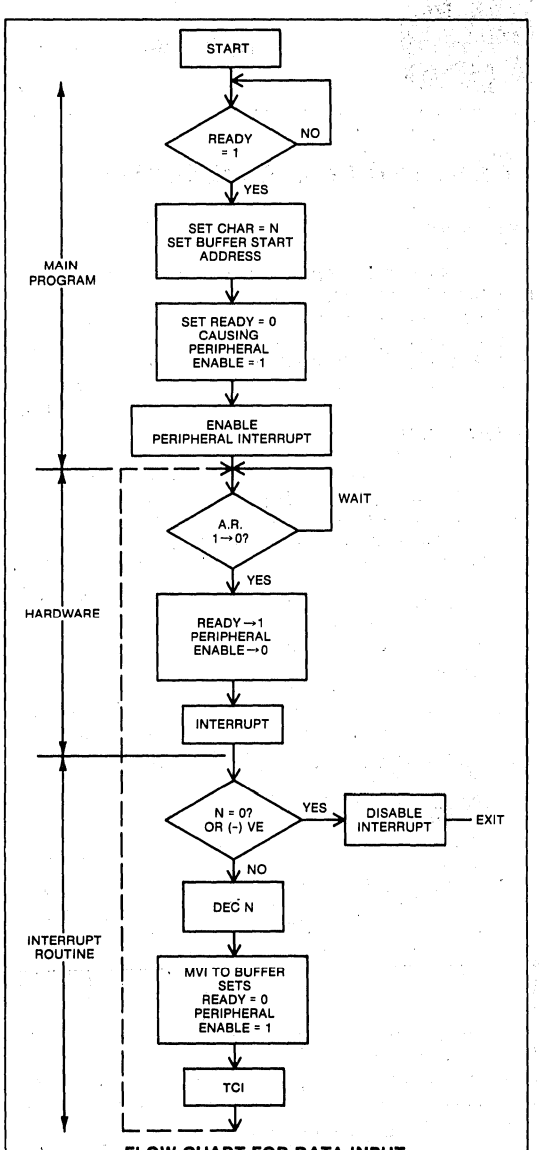
A flow chart for a typical input operation and the corresponding waveform diagram is shown to the right.

The main program setting up the input operation would probably go through the following sequence:

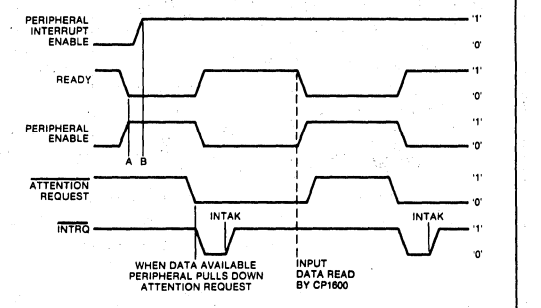
1. Test the Ready bit of the Control Register to ensure that the peripheral device is inactive. After power clear this will be its condition, i.e. set to '1'.
2. If condition (1) is true a CP1600 memory location will be set to contain the number of input operations required. Another memory location will be set to the input buffer start address. This is shown as 'SET CHAR = N, SET BUFFER START ADDRESS'.
3. The Ready bit of the Control Register should now be reset to a '0' by program. This causes the Peripheral Enable/$\overline{\text{Ready}}$ output to go to a '1', requesting an operation from the peripheral device. On the waveform diagram, this is point A.
4. The Peripheral Interrupt Enable bit, PIE, of the Control Register is now set to a '1' by program. This allows the IOB1680 to request interrupts from the CP1600 via the $\overline{\text{INTRQ}}$ output (see point B). Enabling the PIE bit after the Ready Bit ensures that initially no false interrupts are generated.
5. After the Ready bit has been reset by program, (3) above, hardware on the IOB1680 monitors the Attention Request input. A '1' to '0' edge on this input causes the Ready bit to be set to a '1' and the Peripheral Enable/$\overline{\text{Ready}}$ output to go to a '0'. The change in state of the output stops the peripheral operation. As both the PIE bit and Ready bit of the Control Register are set an interrupt request will be generated via the $\overline{\text{INTRQ}}$ output if no higher priority devices are interrupting.
6. When this interrupt is accepted by the CP1600 the acknowledge signal, INTAK, will reset the $\overline{\text{INTRQ}}$ output to its inactive state. The subsequent IAB signal will cause the Interrupt Vector Address associated with the peripheral to be strobed onto the data bus. This address will be used as the start address for the peripheral's interrupt service routine.

   A typical service routine for the peripheral could be:

7. Test value of N. the number of input operations required
   (a) if it is zero all the required input operations have been completed. Reset the PIE bit of the Control Register to a '0' to disable the interrupt capability of the IOB1680 and EXIT.
   (b) if not zero increment the buffer address and decrement N.
8. Move data from the IOB1680 and CP1600 by a MVI instruction. This resets the Ready bit to a '0' and sets the Peripheral Enable/$\overline{\text{Ready}}$ output to a '1', re-enabling the peripheral. The handshake from the peripheral in response to this action is to return the Attention Request input high to a '1'. This timing, however, is not too critical as the input edge triggers the Ready bit.
9. The interrupt is terminated by a TCI instruction which resets the acknowledge flip flop in the IOB1680 interface.



FLOW CHART FOR DATA INPUT



TIMING DIAGRAM FOR MVI INSTRUCTION (DATA FROM IOB1680 TO CP1600)

18 Channel Analog Multiplexer

FEATURES

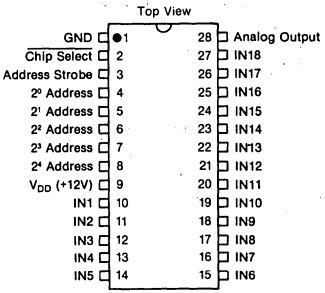
- Connects 1 of 18 analog inputs to analog output pin
- Address latch on-chip
- 0 to 6 volt input range
- Single +12V supply
- Analog output controlled by chip select signal

DESCRIPTION

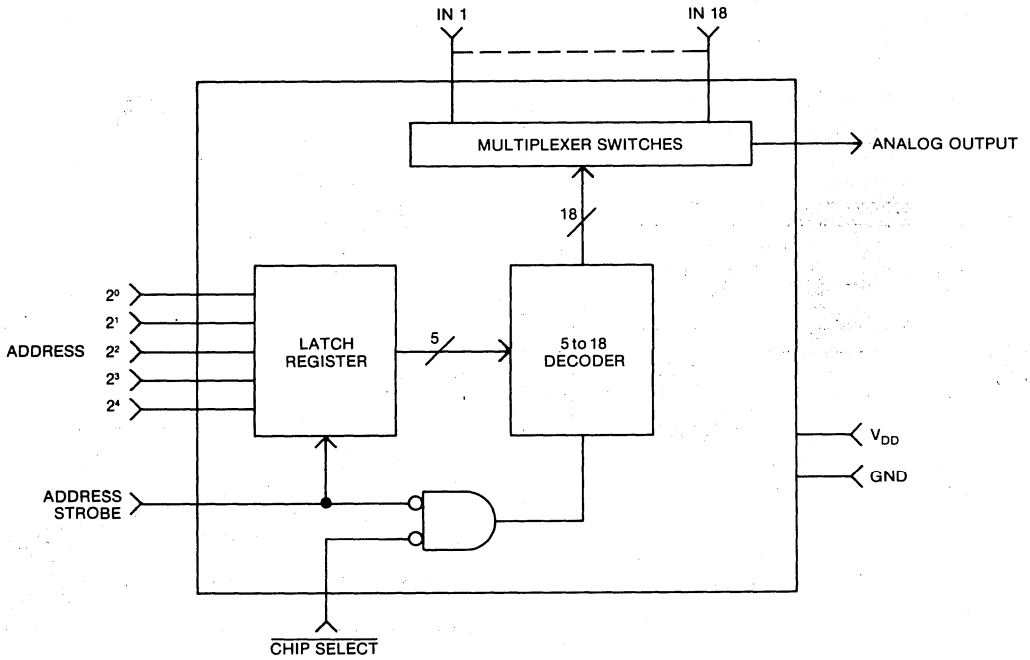
The MUX1600 is a binary addressed 18 channel analog multiplexer fabricated in General Instrument's advanced N-channel Ion Implant process. Featuring on-chip address latches and separate address strobe and chip select signals, the MUX1600 operates from a single +12 Volt supply.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and all other input/output voltages with respect to GND ..... -0.3V to +18V
Storage Temperature ..... -55°C to +150°C
Operating Temperature ..... 0°C to +70°C

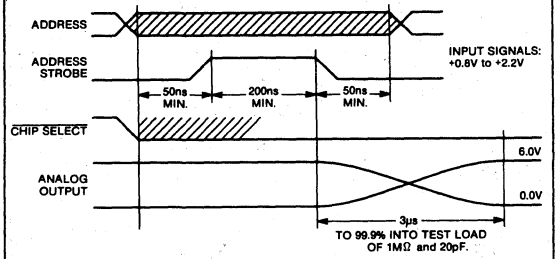
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

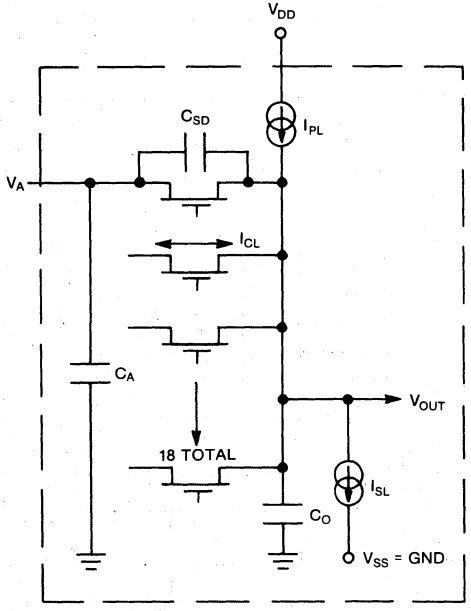
All voltages referenced to GND
V_{DD} = +12V ± 5%
Operating Temperature (T_A) = 0°C to +75°C

Characteristic	Symbol	Min	Typ	Max	Unit	Condition
Input Load Current (all digital inputs)	I_{IN}	—	—	±10	µA	V_{IN} = 0V to 5.25V
Power Supply Current	I_{DD}	—	—	8	mA	All digital inputs = 5.25V
Input Low Voltage	V_{IL}	-0.5	—	0.80	V	
Input High Voltage	V_{IH}	2.2	—	V_{DD}	V	
Analog Input Voltage	V_A	0.0	—	6.0	V	
Channel on Resistance	R_{ON}	—	—	600	Ω	V_A = 0V to 6V
Channel leakage (each channel)	I_{CL}	—	—	5	nA	V_A - V_{OUT} = 6V
V_{DD} Leakage	I_{PL}	—	—	10	nA	V_{DD} - V_{OUT} = 17V
Source to Drain Capacitance	C_{SD}	—	—	5	pF	f = 1 MHz
Analog Input Cap.	C_A	—	—	5	pF	f = 1 MHz
Analog Output Cap.	C_O	—	—	20	pF	f = 1 MHz
Digital Input Cap.	C_D	—	—	5	pF	f = 1 MHz
Substrate Leakage	I_{SL}	—	—	410	nA	V_O - V_{SS} = 6V
18 I_{CL} + I_{PL} + I_{SL}	I_{LT}	—	—	500	nA	V_O - V_{SS} = 6V

SWITCHING CHARACTERISTICS



LEAKAGE CURRENT DIAGRAM



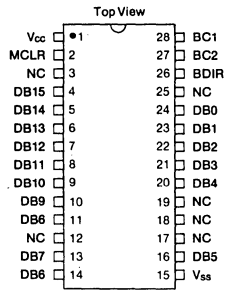
20480 Bit Static Read Only Memory

FEATURES

- 2048 × 10 bit ROM organization
- Address and data on single 16 bit tristate bus
- 5 bit programmable chip select
- Internal address status and data bits latched
- 300 ns typical data access time
- 1.8μs complete cycle time
- TTL compatible I/O
- Single +5 Volt power supply
- Ideal for microprocessors with multiplexed I/O bus for address and data.
- Totally automated custom programming
- 16 bit programmable initialization and interrupt response addresses output to I/O bus

PIN CONFIGURATIONS

28 LEAD DUAL IN LINE



DESCRIPTION

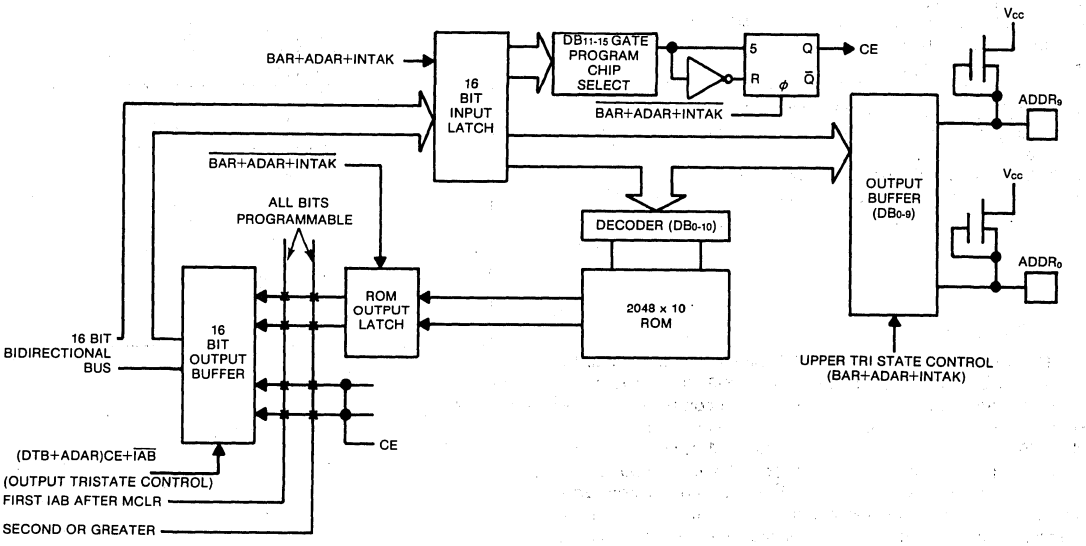
The RO-3-9504 is a unique 20,480 bit ROM employing a single 16 bit address and data tristate bus. The RO-3-9504 increases the power of single bus microprocessors or microcontrollers by providing separate latched address and control lines for static RAM chips. The RO-3-9504 internally decodes ROM via an 11-bit word address and a 5-bit chip select code. Ten bit data is outputted on the lower 10 bits of the I/O bus. In addition there are two programmable 16-bit interrupt response codes, one for the first interrupt after master clear and one for all other interrupts. These codes are output to the I/O bus in response to control codes, which do not require a chip select code. The RO-3-9504 contains a 10 bit latch and address port. The address is latched by a control code on the three mode control lines. The stored address is copied from bits 0 through 9 on the data bus.

The RO-3-9504 has two programmable features, in addition to the 2048 word by 10-bit ROM. A five bit chip select code decodes data bits 11 through 15 in order to generate the internal chip enable signal. Second, the two 16-bit interrupt response codes are programmable.

PIN FUNCTIONS

DB0-DB15	Bidirectional, tristate data and address bus, high output impedance for NACT control code.
BC1, BC2 BDIR	Bus control 1 and 2, and bus direction control signals determine chip mode control.
V_{CC}	+5 Volts
V_{SS}	Ground
MCLR	Master clear, sets all outputs to high impedance state when low.

BLOCK DIAGRAM RO-3-9504



NOTES:

1. Input data and internal chip enable latched by control codes = BAR + ADAR + INTAK
2. Internal chip enable signal cleared by = BAR + ADAR + INTAR
3. Internal RAM enable signal flip flop set by PB11-15 all zeros, cleared by = BAR + ADAR + INTAK
4. RAM enable plus DWS creates low on Read/Write line.
5. RAM enable plus DTB, ADAR or DWS creates enable output signal.
6. DTB or ADAR plus internal chip enable puts output ROM data to tristate bus.
7. Maximum skew time between control code transitions is 40 nsec to avoid false states.
8. Enable R/W and ADDRO — 9 lines normally high impedance outputs. When circuits are enabled, active pull up transistors turned on to allow wires or connection to other chips. RAM control signals and output addresses revert to high impedance state in 2 and 0 - 3μsec respectively. After master clear, chip enable and RAM enable flip-flops turned off and all outputs in high impedance states.

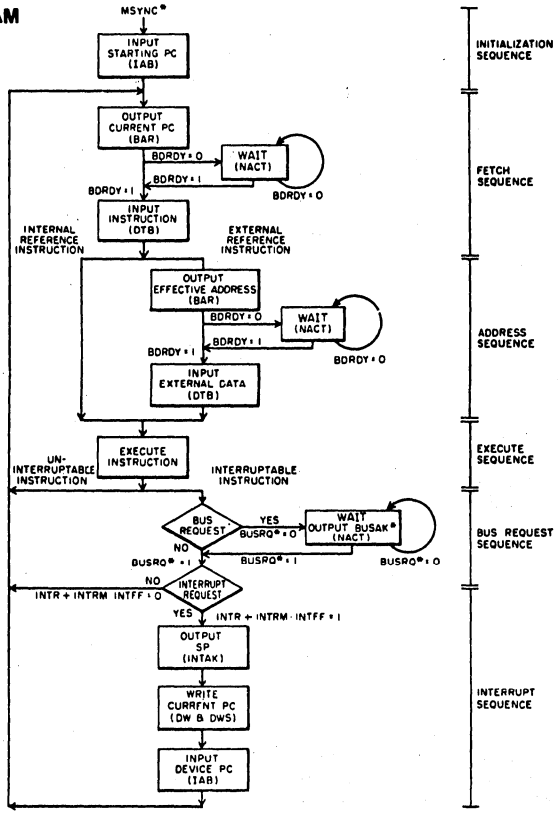
OPERATING MODES

The RO-3-9504 is designed to enhance the system operation of 16-bit Microprocessors that use a single multiplexed bus for data and memory addresses, such as the GI CP1600, the Intel 8085 and the Fairchild 9440. The state diagram shows recommended sequence for initialization, program storage with RAM addressing, and interrupt handling.

The three mode control lines BC1, BC2 and BDIR create 8 functions. As shown in figure one, these functions are chosen to simplify program and data storage in the ROM. Functionally the RO-3-9504 performs the following functions in a microprocessor system:

For the IAB (Interrupt Address to Bus) commands to work properly, an address must first be loaded into the chip to disable the internally latched chip enable code.

SIMPLIFIED STATE FLOW DIAGRAM



BUS CONTROL SIGNALS

BDIR	BC1	BC2	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = high impedance
0	0	1	IAB	Interrupt Address to Bus, D0-D15 = Input
0	1	0	ADAR	Address Data to Address Register, D0-D15 = high impedance
0	1	1	DTB	Data to Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DWS	—
1	1	0	DW	—
1	1	1	INTAK	—

ELECTRICAL CHARACTERISTICS

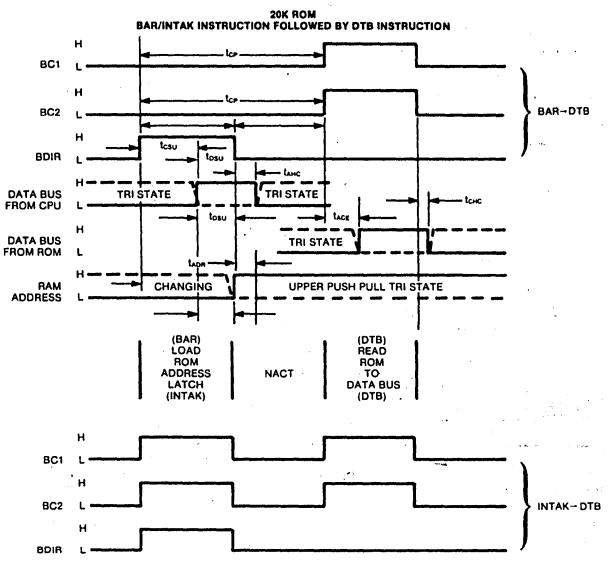
Maximum Ratings*

Temperature Under Bias ..... 0°C to +40°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages
with respect to V_{SS} ..... −0.2V to +9.0V
V_{CC} with respect to V_{SS} ..... −0.2V to +9.0V

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

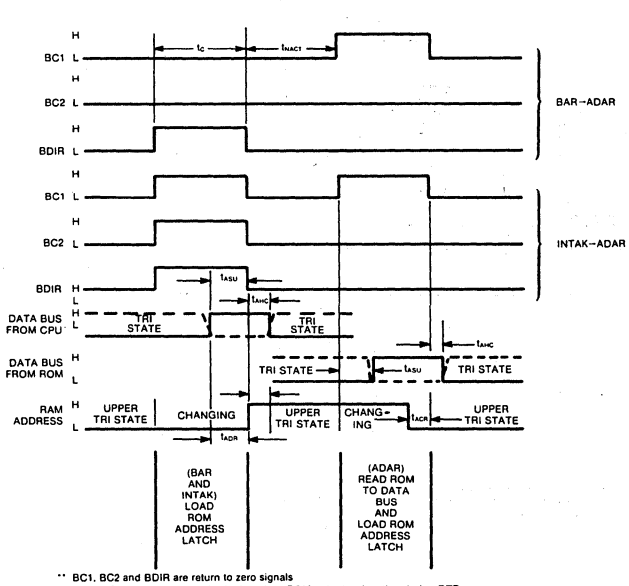
Standard Conditions (unless otherwise noted)
T_A = 0°C to 40°C
V_{CC} = +4.75V to +5.25V
V_{SS} = 0.0V

Characteristics	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Inputs						
Input Logic Low	V_{IL}	0	—	0.7	V	
Input Logic High	V_{IH}	2.4	—	V_{CC}	V	
Input Leakage	I_{IL}	—	—	10	μa	$V_{IN} = V_{CC}$
CPU BUS Outputs						
Output Logic Low	V_{OL}	0	—	0.5	V	1TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	V	+100pF
Supply Current						
V_{CC} Supply	—	—	—	120	mA	V_{CC} = 5.25V at 40°C
AC CHARACTERISTICS						
Inputs						
Address Set Up	t_{AS}	300	—	—	ns	
Address Overlap	t_{AO}	—	50	—	ns	
Write Set Up	t_{WS}	300	—	—	ns	
Write Overlap	t_{WO}	—	50	—	ns	
CPU BUS Outputs						
Turn ON delay	t_{DA}	—	—	300	ns	1TTL Load
Turn OFF delay	t_{DO}	—	—	200	ns	+100pF



* Minimum hold time after DTB before going tristate. Maximum time to tristate = 300ns.
** BC1, BC2 and BDIR are return to zero signals
*** Upper tristate means that the upper push pull output device is disabled and an internal load resistor will hold the output positive
**** Proper CE address must be latched to allow ROM output to function during DTB
***** Since chip is assumed to be selected R/W and RAM enable remain in the high state

Fig. 1



** BC1, BC2 and BDIR are return to zero signals
*** Proper CE address must be latched to allow ROM output to function during DTB
**** Since chip is assumed to be selected R/W and RAM enable remain in the high state

Fig. 2

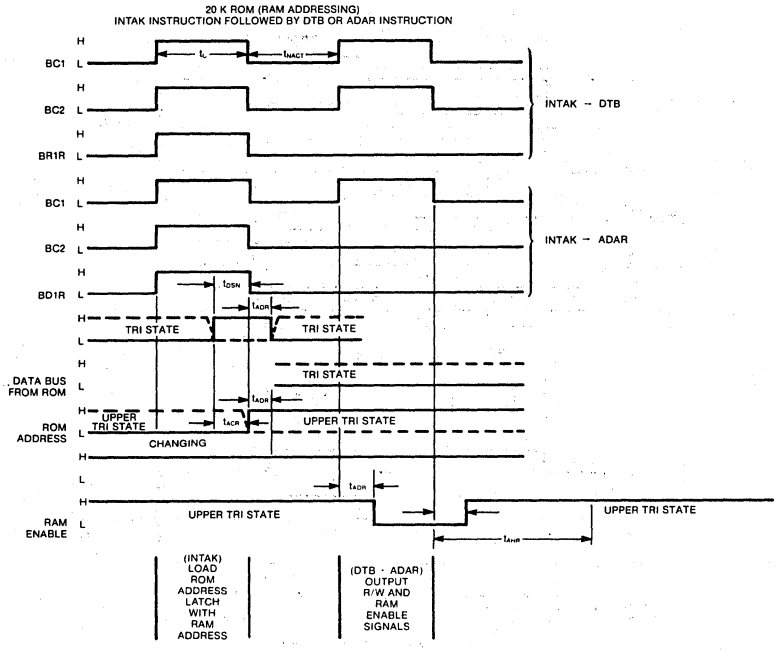
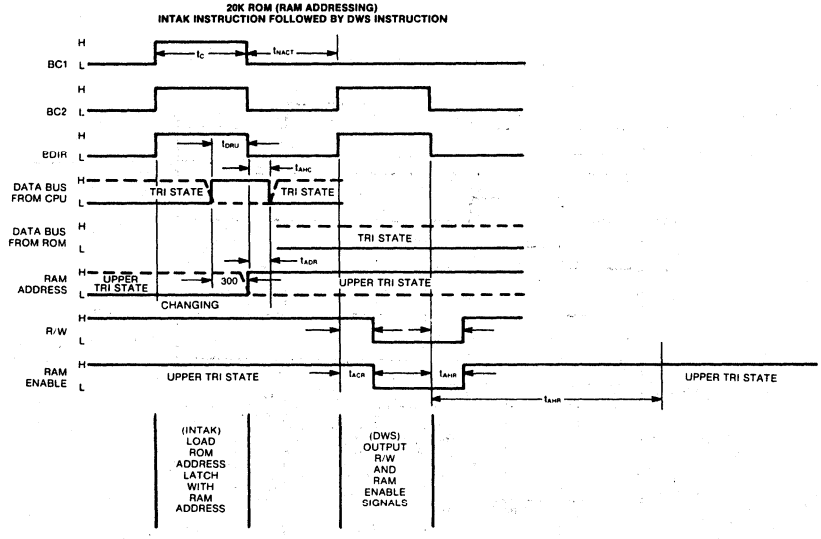
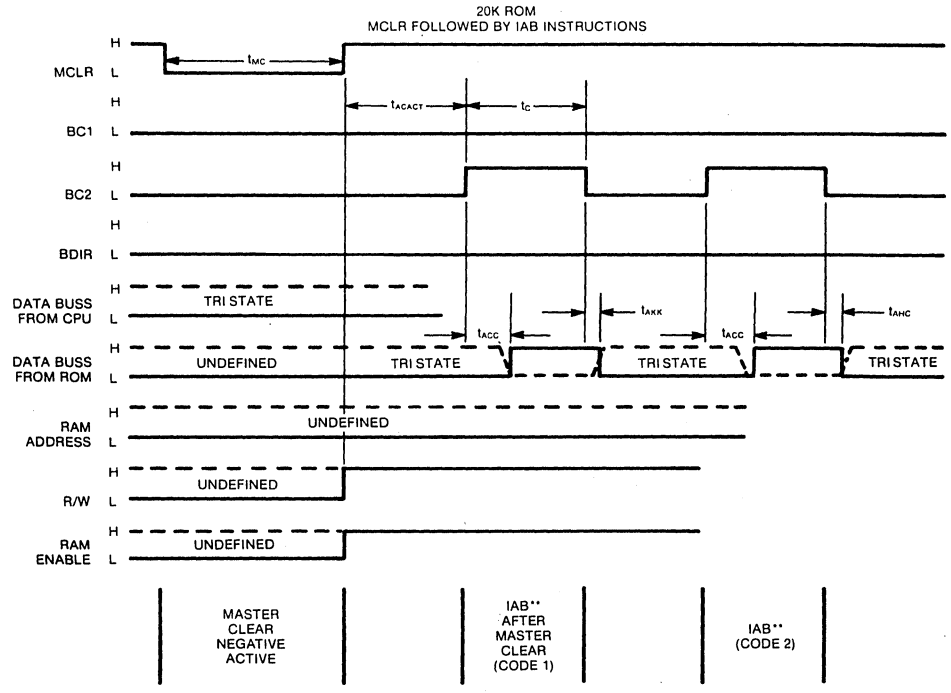


Fig. 3



* Maximum time to upper tri state condition
** RAM address has DB_{11} thru DB_{15} Logic '0'
*** BAR or ADAR can be used instead of INTAK to load RAM address. If ADAR is used remember RAM address will be provided from ROM output to data bus if chip previously enabled.
(All time in nSec)

Fig. 4



* Minimum hold time after IAB before going tri state. Maximum time to tri state = 300ns

** The first IAB after master clear will present a 16 bit programmable code to the data bus. Subsequent IAB instructions will output a second code that is gate programmable on ROM chip.

(All time in nsec)

Fig. 5

ROM 3

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
		Read Only Memories	
5K ROM	5,120 bits organized 512 x 10	RO-3-5120	3-4
16K ROM	16,384 bits organized 2,048 x 8	RO-3-8316A	3-6
		RO-3-8316B	3-6
		RO-3-9316A	3-6
		RO-3-9316B	3-6
		RO-3-9316C	3-6
32K ROM	32,768 bits organized 4,096 x 8	RO-3-9332A	3-11
		RO-3-9332B	3-11
64K ROM	65,536 bits organized 8,192 x 8	RO-3-9364B	3-14
		Keyboard Encoders	
KEYBOARD ENCODERS	2,376 bits organized as 88 keys x 3 modes x 9 bits.	AY-5-2376	3-18
	3,600 bits organized as 90 keys x 4 modes x 10 bits.	AY-5-3600	3-23
		AY-5-3600-PRO	3-29
CAPACITIVE KEYBOARD ENCODER	4,592 bits organized as 112 keys x 4 modes x 10 bits, plus 112 bits for internal programming of "function" keys.	AY-3-4592	3-32
		Character Generator	
CHARACTER GENERATOR	2,560 bits organized as 64 - 5 x 8 characters.	RO-3-2513	3-44

GENERAL INSTRUMENT

Read Only Memories

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
5K ROM	5,120 bits organized 512 x 10	RO-3-5120	3-4
16K ROM	16,384 bits organized 2,048 x 8	RO-3-8316A	3-6
		RO-3-8316B	3-6
		RO-3-9316A	3-6
		RO-3-9316B	3-6
		RO-3-9316C	3-6
32K ROM	32,768 bits organized 4,096 x 8	RO-3-9332A	3-11
		RO-3-9332B	3-11
64K ROM	65,536 bits organized 8,192 x 8	RO-3-9364B	3-14

5120 Bit Static Read Only Memory

FEATURES

- 512×10 Organization
- Single +5 Volt Supply
- TTL/DTL Compatible
- Static Operation—no clocks required
- 500ns Maximum Access Time
- 150mW Typical Power
- Three-State Outputs—under control of 'Output Inhibit' signal
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

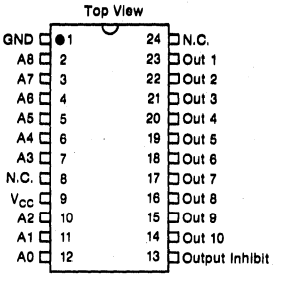
DESCRIPTION

The General Instrument RO-3-5120 is a 5120 bit static Read-Only-Memory. It is organized as 512 ten bit words and requires 9 bits of addressing. An 'Output Inhibit' function is provided to simplify the connection of several ROMs to a common bus. The RO-3-5120 is constructed on a single monolithic chip utilizing low-voltage N-channel ion implant technology.

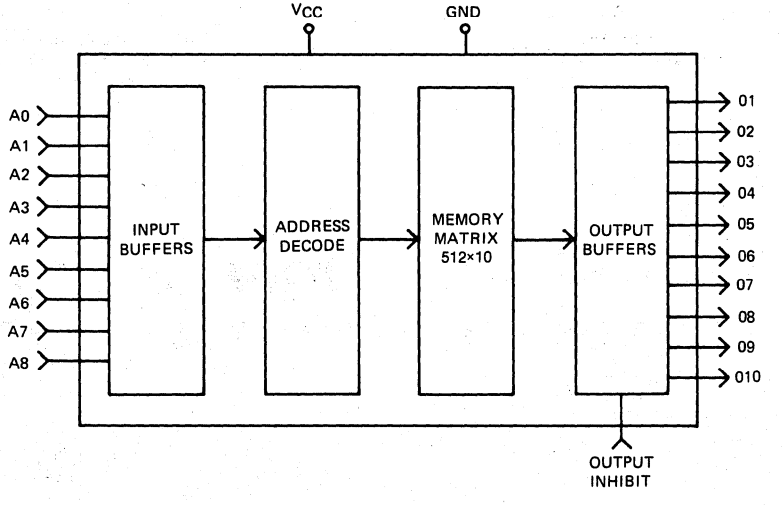
A separate publication, "RO-3-5120 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table data format for custom programming of the RO-3-5120 memory.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRIC CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

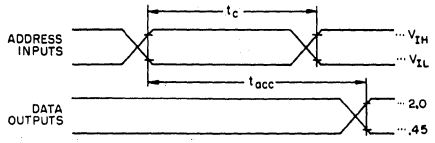
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL Load, $C_{L\ TOTAL}$ = 50pF

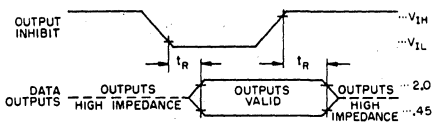
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current	I_{CC}	—	30	45	mA	Outputs Open
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	500	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Data Outputs						
Access Time	t_{ACC}	—	350	500	ns	
Inhibit Response Time	t_R	—	—	230	ns	
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT—OUTPUT INHIBIT AT LOGIC '0')



INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

16384 Bit Static Read Only Memories

FEATURES

- 2048 x 8 Organization—ideal for microprocessor memory systems
- Single +5 Volt Supply
- TTL Compatible—all inputs and outputs
- Static Operation—no clocks required
- 850ns Maximum Access Time: RO-3-8316A/9316A
- 450ns Maximum Access Time: RO-3-8316B/9316B
- 350ns Maximum Access Time: RO-3-9316C
- Three-Stage Outputs—under the control of three mask-programmable Chip Select inputs to simplify memory expansion
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

The General Instrument RO-3-8316A/8316B and RO-3-9316A/9316B/9316C are 16,384 static Read Only Memories organized as 2048 eight bit words and are ideally suited for microprocessor memory applications. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-8316A/8316B and RO-3-9316A/9136B/9316C offer the best combination of high performance, large bit storage, and simple interfacing.

The RO-3-8316A/8316B are direct replacements in pin connection and operation for the Intel 8316A and 2316A.

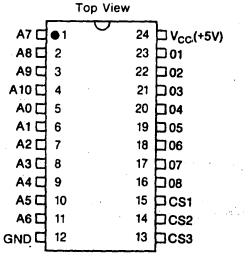
The RO-3-9316A/9316B/9316C pin configuration is identical to that of the Intel 2716 16K EPROM.

A separate publication, "RO-3-8316/9316 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table format for custom programming.

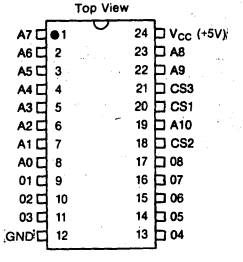
PIN CONFIGURATION

24 LEAD DUAL IN LINE

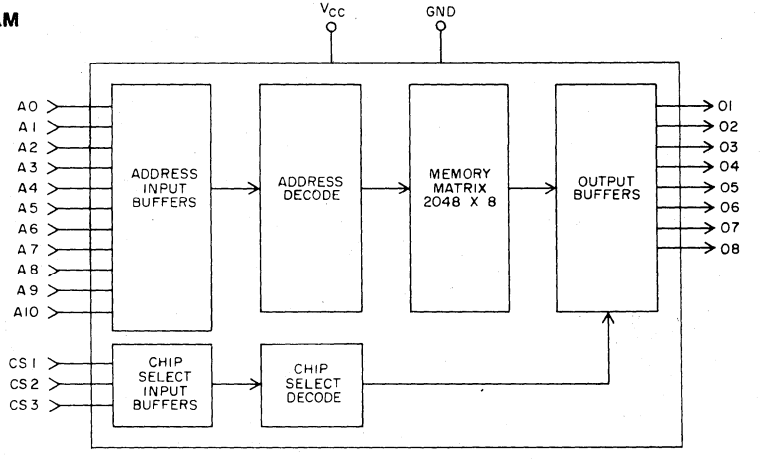
RO-3-8316A/8316B



RO-3-9316A/9316B/9316C



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, $C_{L\ TOTAL}$ = 100pF.

RO-3-8316A/9316A, RO-3-8316B/9316B, and RO-3-9316C

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Select Inputs						
Logic "1"	V_{IH}	2.0	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.4	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
RO-3-8316A/9316A	I_{CC}	—	50	85	mA	Outputs open
RO-3-8316B/9316B	I_{CC}	—	65	95	mA	Outputs open
RO-3-9316C	I_{CC}	—	—	105	mA	Outputs open
RO-3-8316A/9316A						
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	800	—	—	ns	
Capacitance	C_I	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	600	850	ns	
Chip Select Response Time	T_R'	—	200	300	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz
RO-3-8316B/9316B						
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	400	—	—	ns	
Capacitance	C_I	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	350	450	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz
RO-3-9316C						
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	300	—	—	ns	
Capacitance	C_I	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	250	350	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz

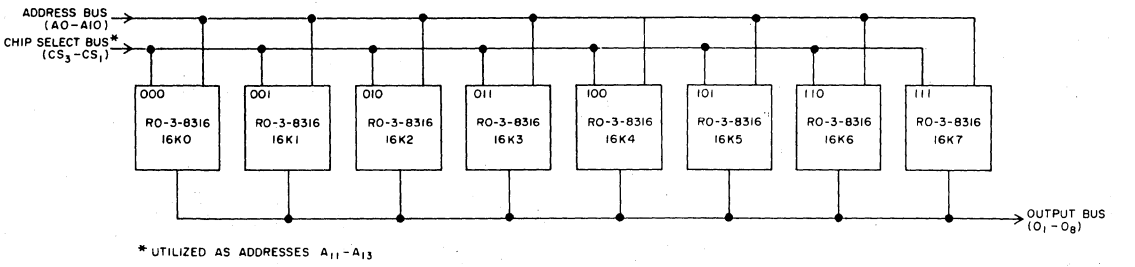
**Typical values are at +25° C and nominal voltages.

TYPICAL SYSTEM APPLICATION

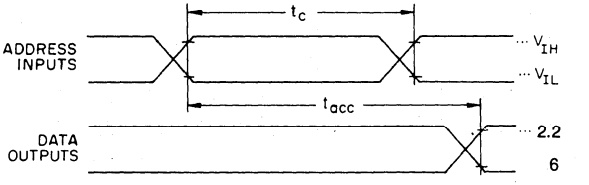
A complete system of 16K words of ROM (8 bits/word) is easily obtained without any external address decoding by making use of programmable chip select features and by wiring the outputs of eight different RO-3-8316's as shown in the figure below.

CHIP SELECT TABLE

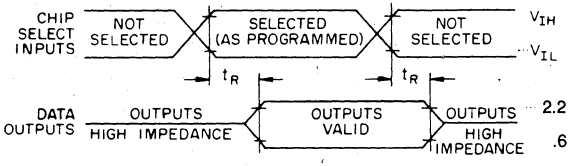
CS3	CS2	CS1	DEVICE SELECTED
0	0	0	16K0
0	0	1	16K1
0	1	0	16K2
0	1	1	16K3
1	0	0	16K4
1	0	1	16K5
1	1	0	16K6
1	1	1	16K7



TIMING DIAGRAMS

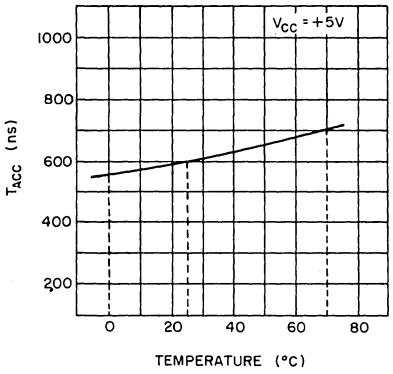


ACCESS TIME (ADDRESS TO OUTPUT—CHIP SELECTED)

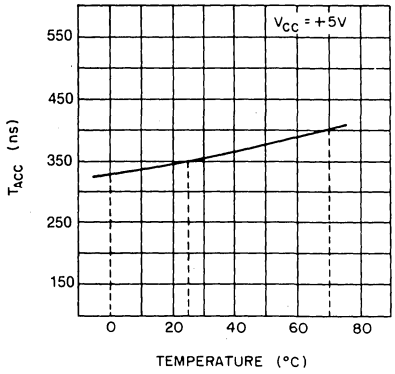


CHIP SELECT RESPONSE TIME (ADDRESS INPUTS STABLE)

TYPICAL CHARACTERISTIC CURVES

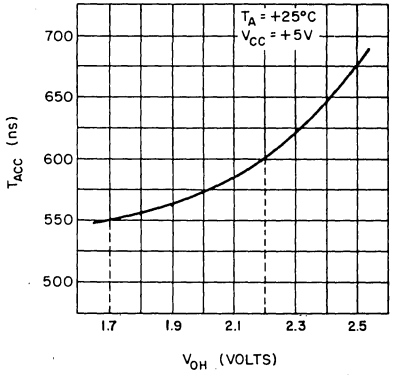


RO-3-8316A/9316A

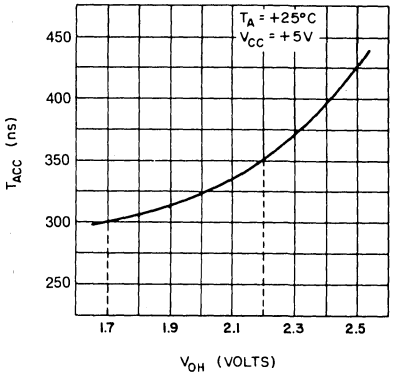


RO-3-8316B/9316B

Fig.1 ACCESS TIME VS. TEMPERATURE

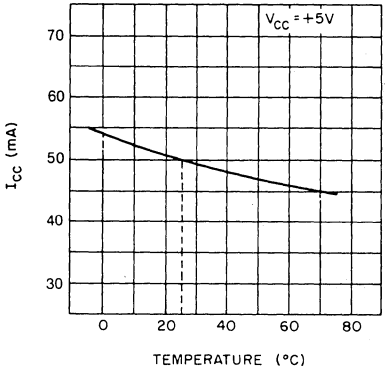


RO-3-8316A/9316A

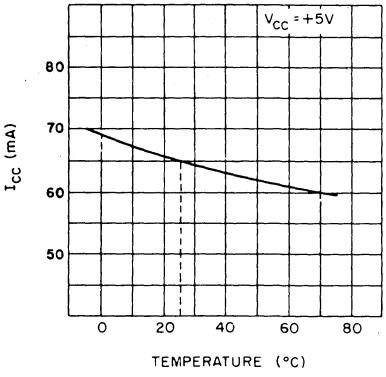


RO-3-8316B/9316B

Fig.2 ACCESS TIME VS. OUTPUT VOLTAGE



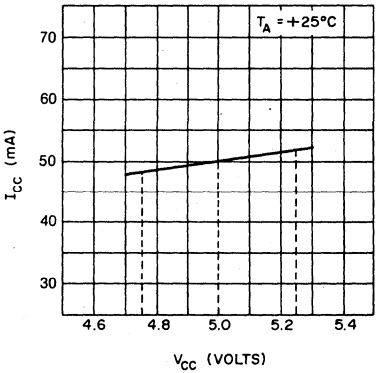
RO-3-8316A/9316A



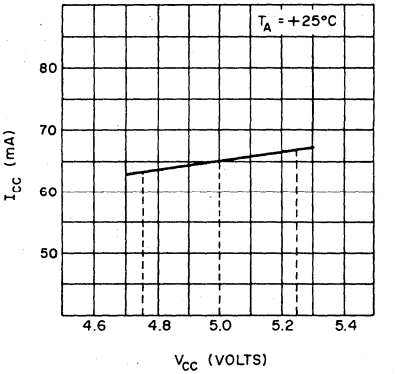
RO-3-8316B/9316B

Fig.3 POWER SUPPLY CURRENT VS. TEMPERATURE

TYPICAL CHARACTERISTIC CURVES

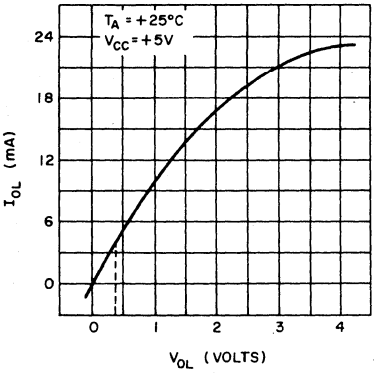


RO-3-8316A/9316A



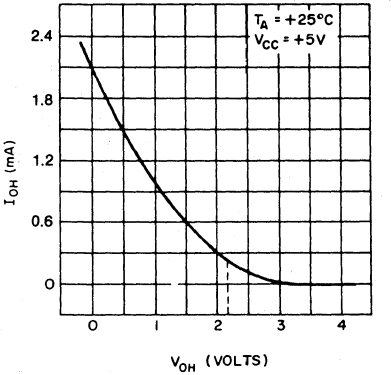
RO-3-8316B/9316B

Fig.4 POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



RO-3-8316A/8316B, RO-3-9316A/9316B

Fig.5 OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



RO-3-8316A/8316B, RO-3-9316A/9316B

Fig.6 OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE

32768 Bit Static Read Only Memory

FEATURES

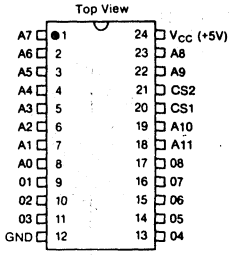
- 4096 × 8 Organization—ideal for microprocessor memory systems
- Single +5 Volt Supply
- TTL Compatible—all inputs and outputs
- Static Operation—no clocks required
- 850ns Maximum Access Time: RO-3-9332A
- 450ns Maximum Access Time: RO-3-9332B
- Three-State Outputs—under the control of two mask-programmable Chip Select inputs to simplify memory expansion
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

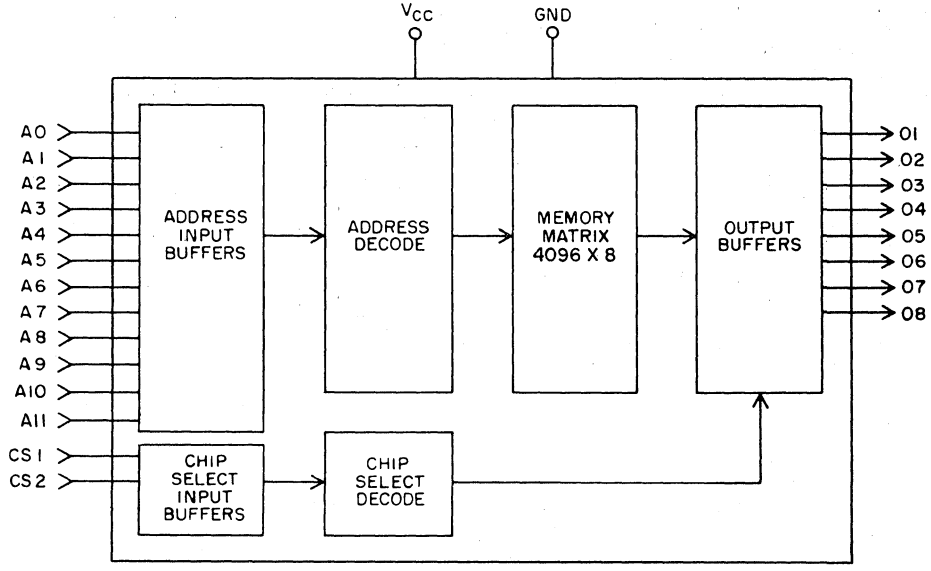
The General Instrument RO-3-9332A/9332B are 32,768 bit static Read Only Memories organized as 4096 eight bit words and are ideally suited for microprocessor memory applications. Fabricated in GI's advance GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-9332A/9332B offer the best combination of high performance, large bit storage, and simple interfacing of any MOS Read-Only Memories available today.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ROM

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±10%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: Two TTL Loads, $C_{L\ TOTAL}$ = 100pF

RO-3-9332A/9332B

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Select Inputs						
Logic "1"	V_{IH}	2.0	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.4	—	—	V	I_{OH} = 200μA
Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 3.2mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
RO-3-9332A	I_{CC}	—	—	60	mA	Outputs open
RO-3-9332B	I_{CC}	—	—	125	mA	Outputs open
RO-3-9332C	I_{CC}	—	—	140	mA	Outputs open

RO-3-9332A

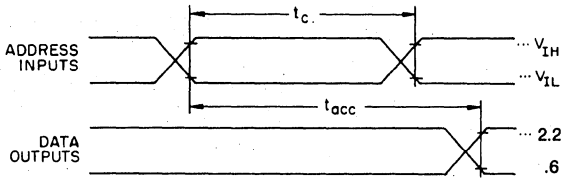
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	800	—	—	ns	
Capacitance	C_1	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	600	850	ns	
Chip Select Response Time	T_R	—	200	300	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz

RO-3-9332B

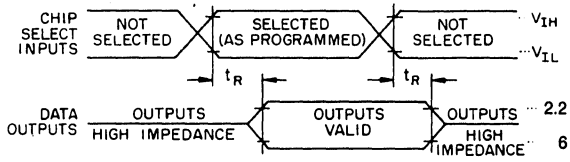
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	450	—	—	ns	
Capacitance	C_1	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	350	450	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT—CHIP SELECTED)



CHIP SELECT RESPONSE TIME (ADDRESS INPUTS STABLE)

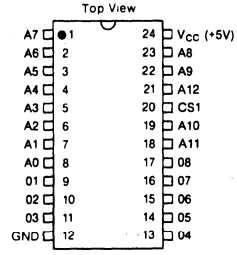
65536 Bit Static Read Only Memory

FEATURES

- 8192 x 8 Organization—ideal for microprocessor memory systems
- Single +5 Volt Supply
- TTL Compatible—all inputs and outputs
- Edge-activated
- 450ns Maximum Access Time
- Three-State Outputs
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

PIN CONFIGURATION

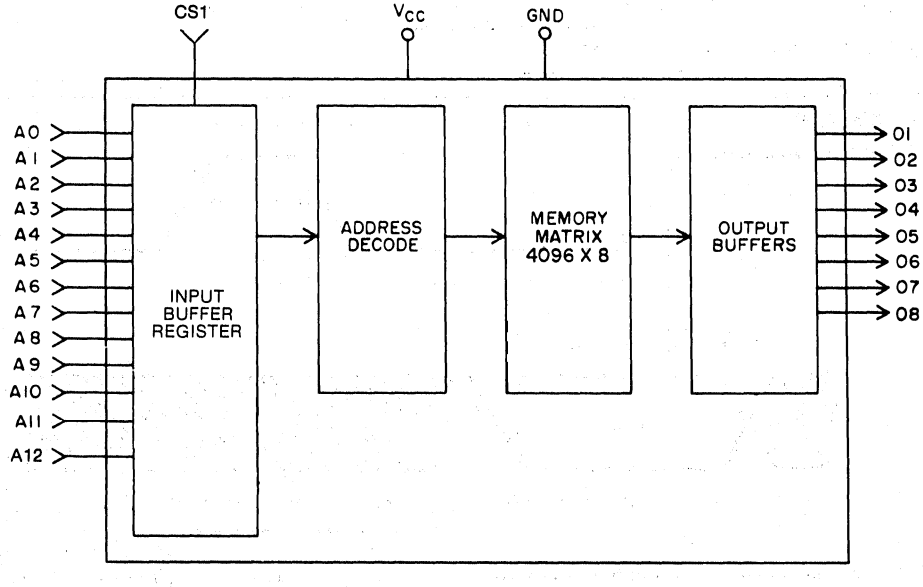
24 LEAD DUAL IN LINE



DESCRIPTION

The General Instrument RO-3-9364B is a 65,536 bit static Read Only Memory organized as 8192 eight bit words and is ideally suited for microprocessor memory applications. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-9364B offers the best combination of high performance, large bit storage, and simple interfacing.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) ..... −0.5V +7.0V
Storage Temperature ..... −65°C to +150°C
Operating Temperature (T_A) ..... 0°C to +70°C

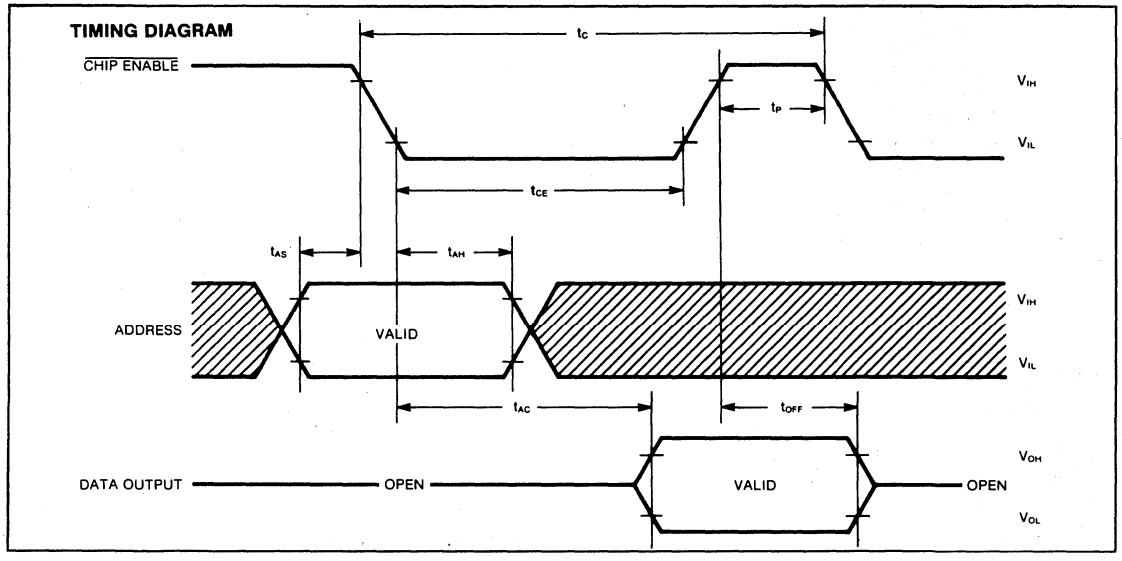
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC}=+5 Volts ±10%
Operating Temperature (T_A)=0°C to +70°C
Output Loading: two TTL Loads, $C_{L\ TOTAL}$=100pF

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Enable Inputs						
Logic "1"	V_{IH}	2.0	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.4	—	—	V	I_{OH}=200μA
Logic "0"	V_{OL}	—	—	0.4	V	I_{OL}=3.2mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
I_{CC} (Active)	—	—	—	50	mA	Output Loading=1MΩ and 100pF
I_{CC} (Standby)	—	—	—	10	mA	$\overline{CE}$ at Minimum Cycle Time $\overline{CE}$=Logic "1"
AC CHARACTERISTICS						
Cycle Time	t_C	400	—	—	ns	All outputs Driving two TTL Loads and 100pF
$\overline{CE}$ Pulse Width	t_{CE}	300	—	—	ns	
$\overline{CE}$ Precharge Time	t_P	100	—	—	ns	
$\overline{CE}$ Access Time	t_{AC}	—	—	300	ns	
Output Turn Off Time	t_{OFF}	—	—	75	ns	
Address Set Up Time	t_{AS}	0	—	—	ns	
Address Hold Time	t_{AH}	75	—	—	ns	
CAPACITANCE						
Input Capacitance	C_I	—	—	7	pF	f=1MHz
Output Capacitance	C_O	—	—	10	pF	f=1MHz

**Typical values are at +25°C and nominal voltages.



ROM

Keyboard Encoders

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
KEYBOARD ENCODERS	2,376 bits organized as 88 keys x 3 modes x 9 bits.	AY-5-2376	3-18
	3,600 bits organized as 90 keys x 4 modes x 10 bits.	AY-5-3600	3-23
		AY-5-3600-PRO	3-29
CAPACITIVE KEYBOARD ENCODER	4,592 bits organized as 112 keys x 4 modes x 10 bits, plus 112 bits for internal programming of "function" keys.	AY-3-4592	3-32

Keyboard Encoder

FEATURES

- One integrated circuit required for complete keyboard assembly
- Outputs directly compatible with TTL/DTL or MOS logic arrays
- External control provided for output polarity selection
- External control provided for selection of odd or even parity
- Two key roll-over operation
- N-key lockout
- Programmable coding with a single mask change
- Self-contained oscillator circuit
- Externally controlled delay network provided to eliminate the effect of contact bounce
- Static charge protection on all input and output terminals
- Entire circuit protected by a layer of glass passivation

DESCRIPTION

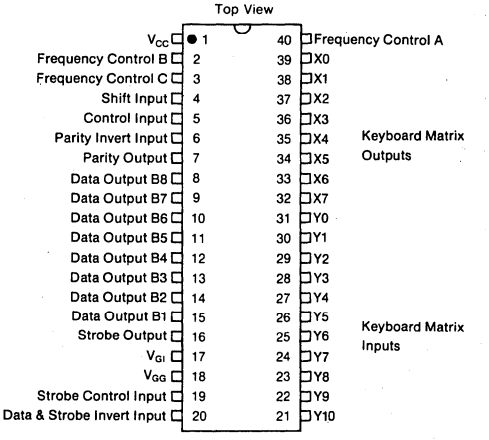
The General Instrument AY-5-2376 is a 2376 Bit Read Only Memory with all the logic necessary to encode single pole single throw keyboard closures into a usable 9-bit code. Data and strobe outputs are directly compatible with TTL/DTL or MOS logic arrays without the use of any special interface components.

The AY-5-2376 is fabricated with MTNS technology and contains 2942 P-channel enhancement mode transistors on a single monolithic chip.

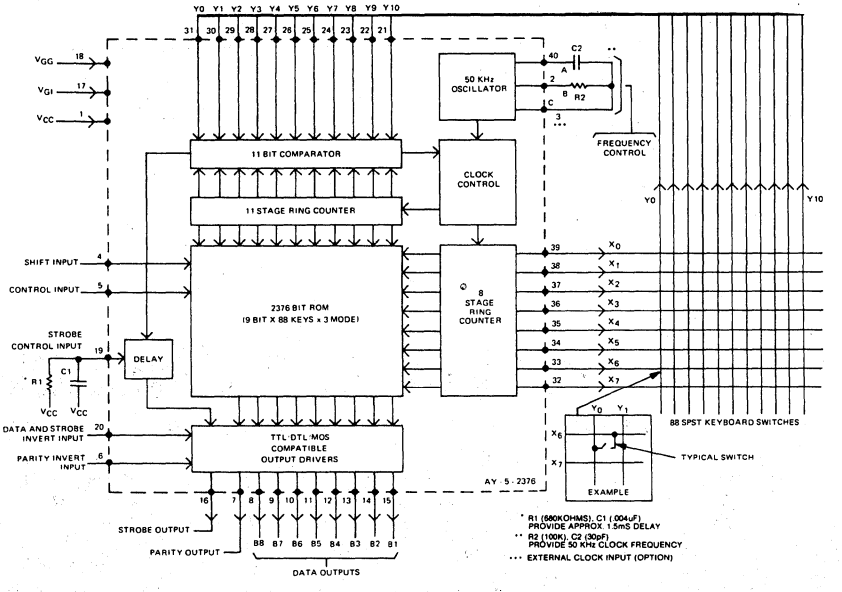
PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View



BLOCK DIAGRAM



OPERATION

The AY-5-2376 contains (see Block Diagram) a 2376-bit ROM, 8-stage and 11-stage ring counters, an 11-bit comparator, an oscillator circuit, an externally controllable delay network for eliminating the effect of contact bounce, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 264 by 9 bit memory arranged into three 88-word by 9-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the three 88-word groups; the 88-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

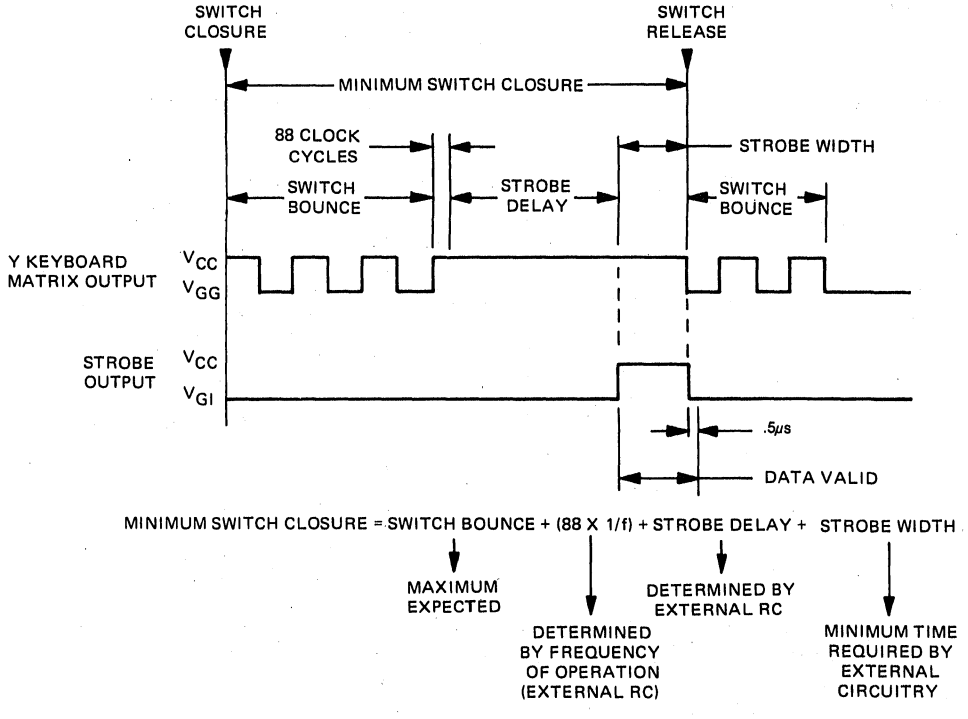
The external outputs of the 8-stage ring counter and the external inputs to the 11-bit comparator are wired to the keyboard to form an X-Y matrix with the 88-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM; the absence of a Strobe Output indicates that the Data Outputs are 'not valid' at this time.

When a key is depressed, a single path is completed between one output of the 8-stage ring counter (X0 thru X7) and one input of the 11-bit comparator (Y0-Y10). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 11-stage ring counter. When this occurs, the comparator generates a signal to the clock control and 9, the Strobe Output (via the delay network). The clock control stops the clocks to the ring counters and the Data Outputs (B1-B9) stabilize with the selected 9-bit code, indicated by a 'valid' signal on the Strobe Output. The Data Outputs remain stable until the key is released.

As an added feature two inputs are provided for external polarity control of the Data Outputs. Parity Invert (pin 6) provides polarity control of the Parity Output (pin 7) while the Data and Strobe Invert Input (pin 20) provides for polarity control of Data Outputs B1 thru B8 (pins 8 thru 15) and the Strobe Output (pin 16).

ROM

TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings

V_{GI} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Logic input voltages (with respect to V_{CC}) . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

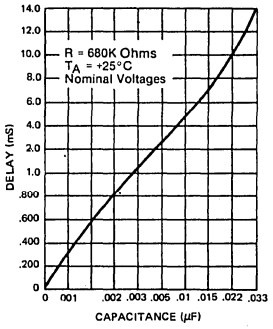
V_{CC} = +5 Volts ± 0.5 Volts, (V_{CC} = Substrate Voltage)
V_{GG} = −12 Volts ± 1.0 Volts, V_{GI} = GND. Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	KHz	See Block diagram footnote** for typical R - C values
Data Input (Shift, Control, Parity invert, data & strobe invert).						
Logic "0" Level	V_{I0}	V_{GG}	—	+0.8	V	
Logic "1" Level	V_{I1}	V_{CC}−1.5	—	V_{CC}+0.3	V	
			—			
Shift & Control Input Current	$I_{INS,C}$	15	36	60	μA	V_I=+5V
		8	16	30	μA	V_I= 0V
Data, Parity Invert Input Current	$I_{IND,P}$	—	.01	1	μA	V_I=−5V to +5V
X Output (X_0-X_7)						
Logic "1" Output Current	I_{XI}	—	0	—	μA	$V_{OUT} = V_{CC}$
		80	150	400	μA	$V_{OUT} = V_{CC}$ −1.3V
		140	300	800	μA	$V_{OUT} = V_{CC}$ −2.0V
		250	700	1500	μA	$V_{OUT} = V_{CC}$ −5V
		500	1500	3000	μA	$V_{OUT} = V_{CC}$ — 10V
Logic "0" Output Current	I_{XO}	15	30	80	μA	$V_{OUT} = V_{CC}$
		13	27	65	μA	$V_{OUT} = V_{CC}$ −1.3V
		12	25	60	μA	$V_{OUT} = V_{CC}$ −2.0V
		5	10	40	μA	$V_{OUT} = V_{CC}$ −5V
		—	1	20	μA	$V_{OUT} = V_{CC}$ −10V
Y Input (Y_0-Y_{10})						
Trip Level	V_Y	V_{CC} −5	V_{CC} −3	V_{CC}−2	V	Y Input Going Positive
Hysteresis	ΔV_Y	.5	.9	1.4	V	Note 1 Note 2
Selected Y Input Current	I_{YS}	30	60	160	μA	$V_{IN} = V_{CC}$
		26	54	130	μA	$V_{IN} = V_{CC}$ −1.3V
		24	50	120	μA	$V_{IN} = V_{CC}$ −2.0V
		10	20	80	μA	$V_{IN} = V_{CC}$ −5V
		—	2	20	μA	$V_{IN} = V_{CC}$ −10V
Unselected Y Input Current	I_{YU}	15	30	80	μA	$V_{IN} = V_{CC}$
		13	27	65	μA	$V_{IN} = V_{CC}$ −1.3V
		12	25	60	μA	$V_{IN} = V_{CC}$ −2.0V
		5	10	40	μA	$V_{IN} = V_{CC}$ −10V
Input Capacitance	C_{IN}	—	3	10	pF	at 0V
Switch Characteristics						
Minimum Switch Closure Contact Closure Resistance	—	—	—	—	—	See Timing Diagram
	Z_{CC}	—	—	300	Ω	
	Z_{CO}	1×10^7	—	—	Ω	
Strobe Delay						
Trip Level (Pin 19)	V_{SD}	V_{CC}−4	V_{CC}−3	V_{CC}−2	V	
Hysteresis	V_{SD}	.5	.9	1.4	V	See Note 1
Quiescent Voltage (Pin 19)		−3	−5	−8	V	With 680K to V_{SS}
Data Output (B_1-B_8)						
Logic "0"	—	—	—	0.4	V	I_{OL} = 1.6ma
Logic "1"	—	V_{CC}−1	—	—	V	I_{OH}−100μa
Power						
I_{CC}	—	—	5	10	mA	V_{CC} = +5V
I_{GG}	—	—	5	10	mA	V_{GG} = −12V

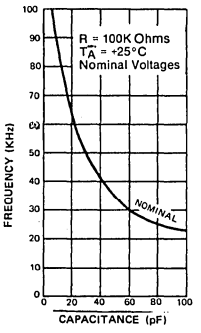
**Typical values at +25°C and nominal voltages.

NOTE 1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Guaranteed number of X & Y loads which may be applied to an X output = eleven.

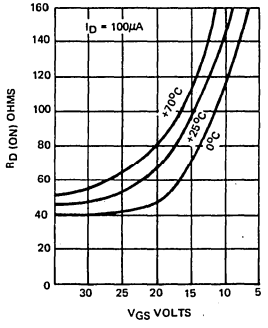
TYPICAL CHARACTERISTIC CURVES



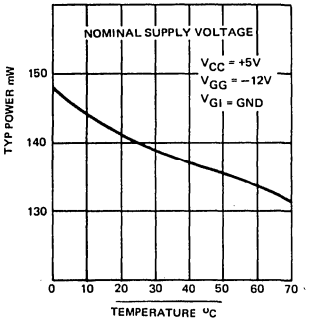
STROBE DELAY C1



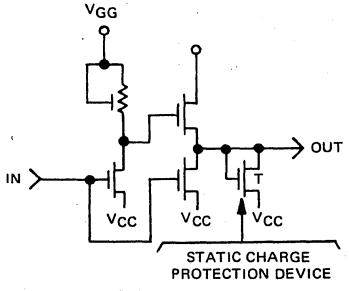
OSCILLATOR FREQUENCY VS. C2



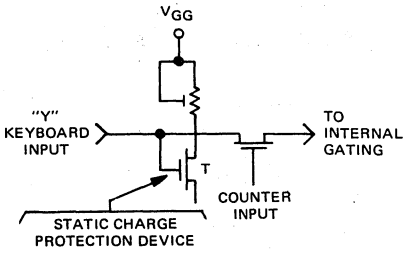
TYPICAL OUTPUT ON RESISTANCE (R_{DON}) VS. GATE BIAS VOLTAGE (V_{GS})



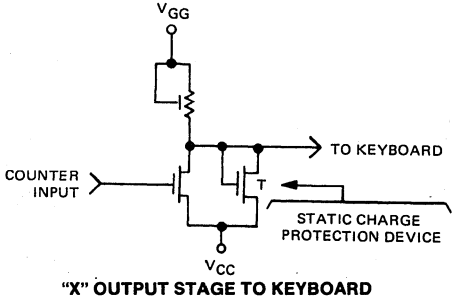
TYPICAL POWER CONSUMPTION (mW) VS. TEMP (°C)



OUTPUT DRIVER



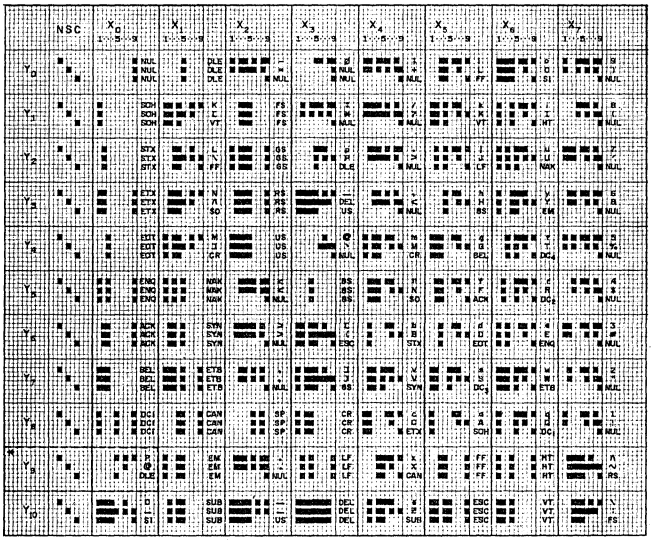
"Y" INPUT STAGE FROM KEYBOARD



"X" OUTPUT STAGE TO KEYBOARD

ROM

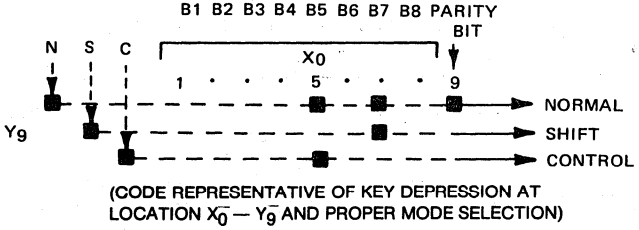
STANDARD CODE ASSIGNMENT CHART



Illustrated using a Logic "O" on the Data and Strobe Invert Input (Pin 20) and the Parity Invert Input (Pin 6).

NOTE 1: This code is an 8 bit ASCII code (B1-B8). Output B9 is included as an odd parity bit operating on outputs B1-B7.

*EXAMPLE



(CODE REPRESENTATIVE OF KEY DEPRESSION AT LOCATION $X_{\overline{0}}$ — $Y_{\overline{9}}$ AND PROPER MODE SELECTION)

N = NORMAL MODE
S = SHIFT MODE
C = CONTROL MODE
■ = OUTPUT LOGIC "1". (SEE DATA B1 – B8)
LOGIC "1" = +5V
LOGIC "0" = GND

TRUTH TABLES

DATA (B1-B8) INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	CODE ASSIGNMENT CHART	DATA OUTPUTS (B1-B8)
1	1	0
0	1	1
1	0	1
0	0	0

PARITY INVERT TRUTH TABLE

PARITY INVERT INPUT (PIN 6)	CODE ASSIGNMENT CHART	PARITY OUTPUT (PIN 7)
1	1	0
0	1	1
1	0	1
0	0	0

STROBE INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	INTERNAL STROBE	STROBE OUTPUT (PIN 16)
1	1	0
0	0	0
1	0	1
0	1	1

MODE SELECTION

$\overline{S}$ $\overline{C}$ = N
$\overline{S}$ $\overline{C}$ = S
$\overline{S}$ C = C
S C = C

Keyboard Encoder

FEATURES

- One integrated circuit required for complete keyboard assembly
- N key rollover or lock out operation
- Quad mode operation
- Lock out/rollover selection under external control (option)
- Self-contained or slave oscillator circuit
- 10 output data bits available
- Outputs directly compatible with TTL/DTL or MOS logic arrays
- Output data buffer register included
- Output enable provided (option)
- External data complement control provided (option)
- Pulse or level data ready output signal provided (option)
- "Any Key Down" output provided (option)
- Externally controlled delay network provided to eliminate the effect of contact bounce
- Programmable coding with a single mask change
- Static charge protection on all input and output terminals
- Entire circuit protected by a layer of glass passivation

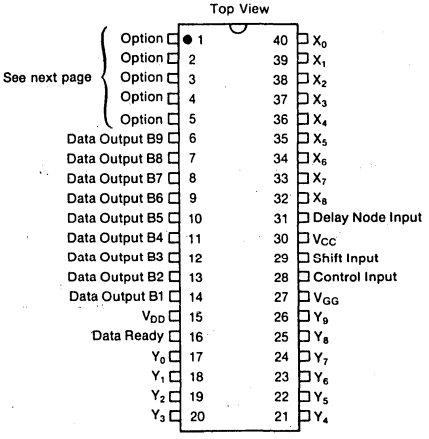
DESCRIPTION

The General Instrument AY-5-3600 is a Keyboard Encoder containing a 3600 bit Read Only Memory and all the logic necessary to encode single pole single throw keyboard closures into a usable 10 bit code. Data, Any Key Down and Data Ready outputs are directly compatible with TTL/DTL or MOS logic arrays without the need for any special interface components.

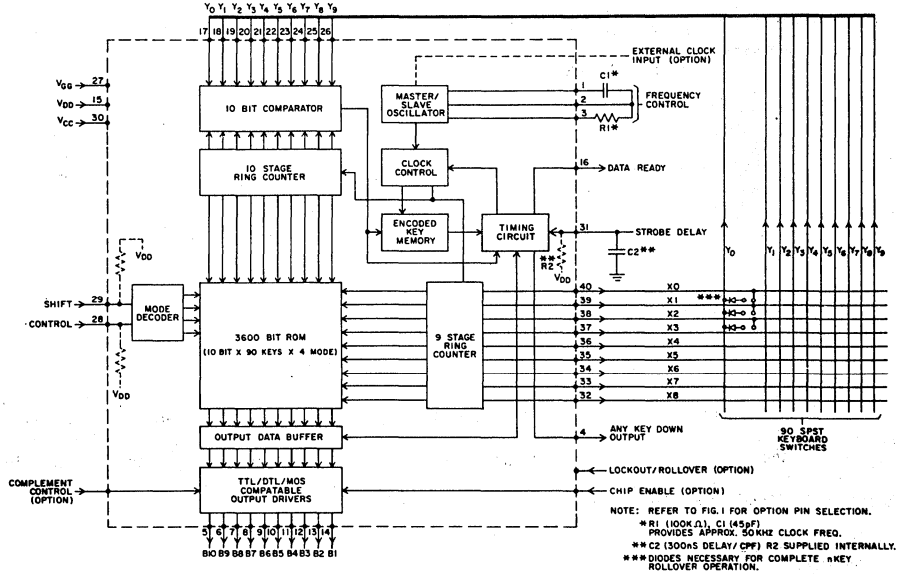
The AY-5-3600 is fabricated with MTNS technology and contains 5000 P channel enhancement mode transistors on a single monolithic chip.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



CUSTOM CODING INFORMATION

The custom coding information for General Instrument's AY-5-3600 Keyboard Encoder ROM should be transmitted to General Instrument in the form of 80 column punched cards. Each ROM pattern requires 92 cards (1 title card, 1 circuit option card and 90 ROM pattern cards). (See Note 1)

If it is not possible to supply punched cards, then the Truth Table should be completed (See Note 1). However, there would be a substantial savings in both the coding charge and turn-around time if punched cards were used. Upon receipt of the punched cards or the Truth Table, General Instrument will prepare a computer-generated Truth Table which will be returned to the user for verification.

NOTE 1: Card and Truth Table format available upon request.

PIN OPTIONS

Pins 6-40 of the AY-5-3600 are permanently assigned. The functions assigned to pins 1-5 depend on which functional options are selected from the following:

External Clock
—requires one package pin to input an external clock source.
Internal Oscillator
—requires three package pins interconnected with an external RC network to develop the clock required.
Lockout/Rollover (LO/RO)
—requires one package pin to externally select N-Key Lockout or N-Key Rollover. LO = +5V, RO = GND.
Complement Control (CC)
—requires one package pin to externally control the logic state of the data bits (B1-B10) and, if required, the Data Ready output.
Chip Enable (CE)
—requires one package pin to control the data bits (B1-B10) and, if required, the Data Ready and Any Key Output.
Any Key Output (AKO)
—requires one package pin to indicate a key depression.
Output Data Bit 10 (B10)
—requires one package pin when ten data bits are required to encode each key.

Select the pin options desired:
External Clock + 4 of the following functions
OR
Internal Oscillator + 2 of the following functions
LO/RO, CC, CE, AKO, BIO

The following chart lists the pin assignments according to the functions selected above:

PIN 1	PIN 2	PIN 3	PIN 4	PIN 5
External Clock	LO/RO	CC	CE	AKO
External Clock	LO/RO	CC	CE	BIO
External Clock	LO/RO	CC	AKO	BIO
External Clock	LO/RO	CE	AKO	BIO
External Clock	CC	CE	AKO	BIO
Internal Oscillator			LO/RO	CC
			LO/RO	CE
			LO/RO	AKO
			LO/RO	BIO
			CC	CE
			CC	AKO
			CC	BIO
			CE	AKO
			CE	BIO
			AKO	BIO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Logic input voltages (with respect to V_{CC}) . . . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature Range. . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts
V_{GG} = −12 Volts ±1.0 Volts, V_{DD} = GND
(V_{CC} = Substrate Voltage)
Operating Temperature (T_A)= 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	kHz	See Block diagram footnote* for typical R-C values
External Clock Width		7	—	—	μs	
Clock Input	V_{I0}	V_{GG}	—	.15	V	
	V_{I1}	$V_{CC}-1.4$	—	$V_{CC}+0.3$	V	
Data Input (Shift, Control, Complement Control, Lockout/Rollover, Chip Enable & External Clock)						
Logic "0" Level	V_{I0}	V_{GG}	—	+0.75	V	
Logic "1" Level	V_{I1}	$V_{CC}-1.1$	—	$V_{CC}+0.3$	V	
Shift & Control Input Current	I_{NSC}	75	95	120	μA	$V_I = +5V$
X Output (X_0-X_8)						
Logic "1" Output Current	I_{X1}	40	170	400	μA	$V_{OUT} = V_{CC}$ (See Note 2)
		600	1300	2500	μA	$V_{OUT} = V_{CC}-1.3V$
		900	1600	3500	μA	$V_{OUT} = V_{CC}-2.0V$
		1500	3800	6000	μA	$V_{OUT} = V_{CC}-5V$
		3000	6000	10000	μA	$V_{OUT} = V_{CC}-10V$
Logic "0" Output Current	1_{XO}	8	15	50	μA	$V_{OUT} = V_{CC}$
		6	11	35	μA	$V_{OUT} = V_{CC}-1.3V$
		5	10	30	μA	$V_{OUT} = V_{CC}-2.0V$
		2	5	15	μA	$V_{OUT} = V_{CC}-5V$
		—	0.5	5	μA	$V_{OUT} = V_{CC}-10V$
Y Input (Y_0-Y_9)						
Trip Level	V_Y	$V_{CC}-5$	$V_{CC}-3$	$V_{CC}-2$	V	Y Input Going Positive (See Note 2)
Hysteresis	ΔV_Y	0.5	0.9	1.4	V	(See Note 1)
Selected Y Input Current	I_{YS}	18	36	100	μA	$V_{IN} = V_{CC}$
		14	28	90	μA	$V_{IN} = V_{CC}-1.3V$
		13	25	80	μA	$V_{IN} = V_{CC}-2.0V$
		6	12	60	μA	$V_{IN} = V_{CC}-5V$
		—	1	30	μA	$V_{IN} = V_{CC}-10V$
Unselected Y Input Current	I_{YU}	9	18	50	μA	$V_{IN} = V_{CC}$
		7	14	45	μA	$V_{IN} = V_{CC}-1.3V$
		6	13	40	μA	$V_{IN} = V_{CC}-2.0V$
		3	6	30	μA	$V_{IN} = V_{CC}-5V$
		—	0.5	15	μA	$V_{IN} = V_{CC}-10V$
Input Capacitance	C_{IN}	—	3	10	pF	at 0V (All Inputs)
X-Y Precharge Characteristics	ϕP	1500	3500	5000	μA	$V = V_{CC}$
		200	600	1500	μA	$V = V_{CC}-5$ (See Note 2)
Switch Characteristics						
Minimum Switch Closure	—	—	—	—	—	See Timing Diagram
Contact Closure Resistance	Z_{CC}	—	—	300	Ω	
	Z_{CO}	1×10^7	—	—	Ω	
Strobe Delay						
Trip Level (Pin 31)	V_{SD}	$V_{CC}-4$	$V_{CC}-3$	$V_{CC}-2$	V	
Hysteresis	V_{SD}	0.5	0.9	1.4	V	(See Note 1)
Quiescent Voltage (Pin 31)		−3	−5	−9	V	With Internal Switched Resistor
Data Output (B1-B10), Any Key Down Output, Data Ready						
Logic "0"	—	—	—	.55	V	$I_{OL} = .25mA$
	—	—	—	0.8	V	$I_{OL} = 1.6mA$
Logic "1"	—	$V_{CC}-1.3$	—	—	V	$I_{OH} = .95mA$
Power						
I_{CC}	—	—	8	13	mA	$V_{CC} = +5V$
I_{GG}	—	—	8	13	mA	$V_{GG} = -12V$

**Typical values are at +25°C and nominal voltages.

NOTE
1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Precharge of X outputs and Y inputs occurs during each scanned clock cycle.

ROM

OPERATION

The AY-5-3600 contains (see Block Diagram) a 3600 bit ROM, 9-stage and 10-stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for n key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 360 by 10 bit memory arranged into four 90-word by 10-bit groups. The appropriate levels on the Shift and Control Inputs selects one of the four 90-word groups; the 90-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control Inputs with the two ring counters.

The external outputs of the 9-stage ring counter and the external inputs to the 10-bit comparator are wired to the keyboard to form an X-Y matrix with the 90-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM, thereby scanning the key switches for key closures.

When a key is depressed, a single path is completed between one output of the 9-stage ring counter (X0 thru X8) and one input of the 10-bit comparator (Y_0-Y_9). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10-stage ring counter.

N KEY ROLLOVER

— When a match occurs, and the key has not been encoded, the switch bounce delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears, a one is stored in the encoded key memory and the scan sequence is resumed. If a match occurs at another key location, the sequence is repeated thus encoding the next key. If the match occurs for an already encoded key, the match is not recognized. The code of the last key encoded remains in the output data buffer.

N KEY LOCKOUT

— When a match occurs, the delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears and the remaining keys are locked out by halting the scan sequence. The scan sequence is resumed upon key release. The output data buffer stores the code of the last key encoded.

SPECIAL PATTERNS

— Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to 10 bits can be programmed into the AY-5-3600 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes. The ASCII code in conjunction with internal oscillator, 10 data outputs and any key down output, is available as a standard pattern (See Figure 2).

ROM

TIMING DIAGRAM

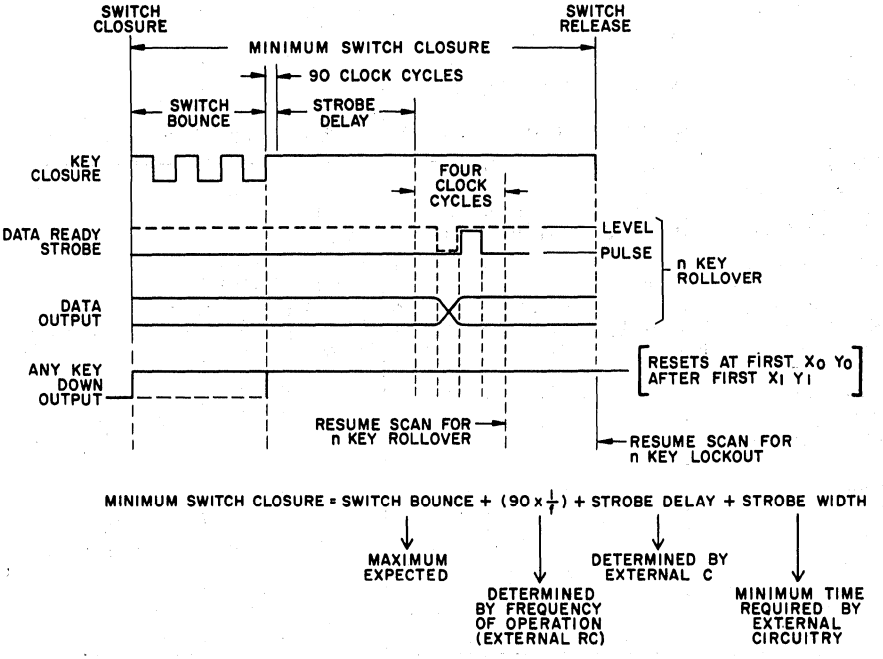


Fig.1

SYMBOL	MODE N	S	C	SC
●		X1 Y0, X0 Y8		
A		X0 Y2		X1 Y2
B		X5 Y3		X2 Y2
C		X2 Y3		X3 Y2
D		X2 Y2		X4 Y2
E		X2 Y1		X5 Y2
F		X3 Y2		X6 Y2
G		X4 Y2		X7 Y2
H	X0 Y5	X0 Y5, X5 Y2	X0 Y5	X0 Y5
I		X7 Y1		X0 Y4
J		X6 Y2		X6 Y6
K		X7 Y2		X3 Y6
L	X2 Y6	X2 Y6, X8 Y2	X2 Y6	X2 Y6
M		X7 Y3		X3 Y5
N		X6 Y3		X4 Y5
O		X8 Y1		
P		X6 Y6		X0 Y2, X0 Y3
Q		X0 Y1		X1 Y3
R		X3 Y1		X2 Y3
S		X1 Y2		X4 Y3
T		X4 Y1		X5 Y3
U		X0 Y1		X6 Y3
V		X4 Y3		X7 Y3
W		X1 Y1		X6 Y5
X		X1 Y3		X8 Y2
Y		X5 Y1		X5 Y6
Z		X0 Y3		X5 Y5
a	X0 Y2		X0 Y2	
b	X5 Y3		X5 Y3	
c	X2 Y3		X2 Y3	
d	X2 Y2		X2 Y2	
e	X2 Y1		X2 Y1	
f	X3 Y2		X3 Y2	
g	X4 Y2		X4 Y2	
h	X5 Y2		X5 Y2	
i	X7 Y1		X7 Y1	
j	X6 Y2		X6 Y2	
k	X7 Y2, X2 Y9		X7 Y2	
l	X8 Y2		X8 Y2	
m	X7 Y3, X1 Y6		X7 Y3	
n	X6 Y3, X1 Y8		X6 Y3	
o	X8 Y1		X8 Y1	
p	X6 Y6, X0 Y8		X6 Y6	
q	X0 Y1		X0 Y1	
r	X3 Y1		X3 Y1	
s	X1 Y2		X1 Y2	
t	X4 Y1		X4 Y1	
u	X6 Y1		X6 Y1	
v	X4 Y3		X4 Y3	
w	X1 Y1		X1 Y1	
x	X1 Y3		X1 Y3	
y	X5 Y1		X5 Y1	
z	X0 Y3		X0 Y3	
[		X8 Y6, X2 Y9		X4 Y6, X8 Y6
\				X1 Y1
]	X8 Y6	X1 Y6	X8 Y6	X8 Y1
^		X1 Y8		X2 Y4
_	X4 Y7, X8 Y7		X4 Y7, X8 Y7	X4 Y7
(	X3 Y6	X3 Y6	X3 Y6	
{	X4 Y5	X4 Y5	X4 Y5	
~				X6 Y4
DEL			X2 Y9	X2 Y9
NULL	X5 Y7	X5 Y7	X5 Y7, X0 Y8	X5 Y7, X0 Y8

SYMBOL	MODE N	S	C	SC
SOH			X0 Y9	X5 Y0, X0 Y9
STX			X1 Y9	X4 Y0, X1 Y9
ETX	X4 Y4	X4 Y4	X4 Y4	X4 Y4, X6 Y0
EOT				X4 Y1
ENQ				X3 Y1
ACK			X2 Y8	X7 Y1, X2 Y8
BEL			X3 Y8	X6 Y1, X3 Y8
BS				X3 Y4
HT	X0 Y4	X0 Y4	X0 Y4, X8 Y9	X8 Y9
LF	X7 Y6	X7 Y6	X7 Y6	
VT	X3 Y7	X3 Y7	X3 Y7	X3 Y7
FF	X7 Y8		X7 Y8	X7 Y8
CR	X3 Y5	X3 Y5	X3 Y5, X1 Y6	X1 Y6
SO	X0 Y7		X0 Y7, X1 Y8	X0 Y7, X1 Y8
SI	X1 Y7	X1 Y7	X1 Y7	X1 Y7
DLE				X0 Y1
DC1				X5 Y1
DC2				X6 Y7
DC3				X2 Y1
DC4				X3 Y0
NAK				X2 Y0
SYN				X5 Y4
ETB				X1 Y0
CAN	X3 Y4		X3 Y4	
EM				X8 Y0
SUB				X0 Y0
ESC				X7 Y0
FS				X1 Y4
GS				X7 Y6
RS	X1 Y4	X1 Y4	X1 Y4	
US	X2 Y7	X2 Y7	X2 Y7	X2 Y7
SP	X3 Y3, X4 Y9	X4 Y9, X3 Y3	X4 Y9, X3 Y3	X4 Y9, X3 Y3
!	X5 Y9	X5 Y9, X0 Y9	X5 Y9	X5 Y9
"	X3 Y9	X3 Y9, X7 Y5, X1 Y9	X3 Y9	X3 Y9, X7 Y5
#	X6 Y9	X6 Y9, X2 Y0	X6 Y9	X6 Y9
$	X2 Y5	X2 Y5, X3 Y0	X2 Y5	X2 Y5
%	X1 Y5	X1 Y5, X4 Y0	X1 Y5	X1 Y5
&	X6 Y8	X6 Y0, X6 Y8, X2 Y8	X6 Y8	X6 Y8
'	X7 Y5	X3 Y8	X7 Y5	X7 Y4
(	X7 Y9	X7 Y4, X3 Y4, X8 Y0	X7 Y9	X7 Y9
)	X4 Y8	X4 Y8, X6 Y7, X8 Y9	X4 Y8	X4 Y8
*	X5 Y8	X5 Y8, X7 Y0, X5 Y4	X5 Y8	X5 Y8
+	X0 Y6	X0 Y6, X5 Y6, X7 Y7	X0 Y6	X0 Y6, X7 Y7
,	X8 Y3	X8 Y3	X8 Y3	X8 Y3
—	X2 Y4	X2 Y4, X8 Y7	X2 Y4	X8 Y7
.	X8 Y4	X8 Y4	X8 Y4	X8 Y4
/	X7 Y4		X7 Y4	
0	X6 Y7, X8 Y8	X8 Y8	X6 Y7, X8 Y8	X8 Y8
1	X0 Y0, X0 Y9		X0 Y0	
2	X1 Y0, X1 Y9		X1 Y0	
3	X2 Y6		X2 Y0	
4	X3 Y0		X3 Y0	
5	X4 Y0		X4 Y0	
6	X5 Y0, X2 Y8		X5 Y0	
7	X6 Y0, X3 Y8		X0 Y0	
8	X7 Y0		X7 Y0	
9	X8 Y0, X8 Y9		X8 Y0	
:	X5 Y4	X8 Y5	X5 Y4	X8 Y5
;	X8 Y5, X5 Y6		X8 Y5, X5 Y6	
<	X6 Y5	X7 Y8, X6 Y5, X0 Y0	X6 Y5	
=	X6 Y4, X7 Y7	X7 Y7, X6 Y4, X4 Y7	X6 Y4	
>	X5 Y5	X5 Y5, X5 Y0, X0 Y7	X5 Y5	
?	X4 Y6	X4 Y6, X7 Y4	X4 Y6	

Note 1. Bits 1 to 6 and bit 8 of the AY-5-3600 correspond to bits 1 to 7 of ASC II.

Note 2. Codes 0000011 and 0011111 are not present in the standard AY-5-3600 pattern.

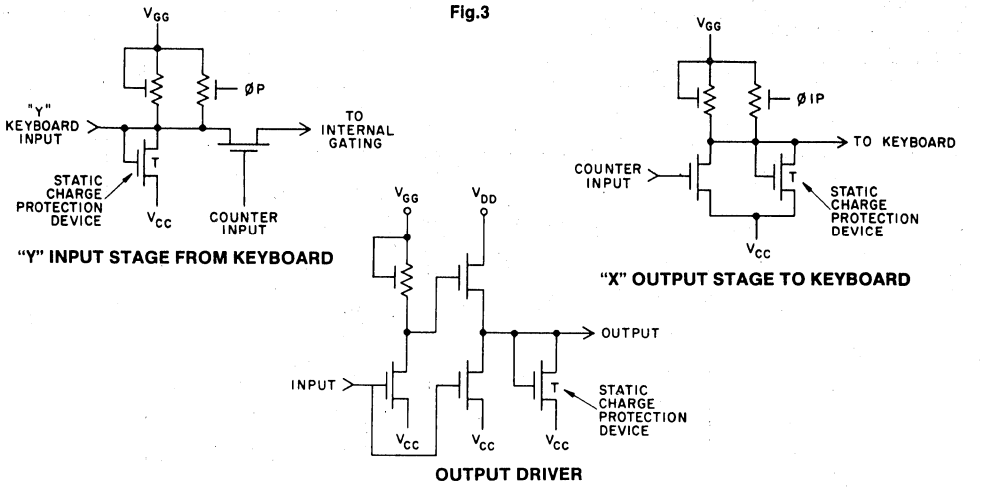
Fig.2 STANDARD AY-5-3600 CODE ASSIGNMENTS ASCII CODE

OPTIONS PROVIDED WITH STANDARD ENCODER

- Device Marking: AY-5-3600
- Internal Oscillator on Pin Nos. 1, 2, 3
- Any Key Output on Pin No. 4
- Any Key Output True (Logic 1) During Key Depression
- Output Data Bit B10 on Pin No. 5
- N-Key Rollover Only
- True Outputs Only
- Pulse Data Ready Signal
- Internal Resistor to V_{DD} on Shift/Control Pin
- Plastic Package

ROM

Fig.3



NOTE: Output driver capable of driving one TTL load with no external resistor.
Capable of driving two TTL loads using an external 6.8KΩ resistor to V_{GG}.

TYPICAL CHARACTERISTIC CURVES

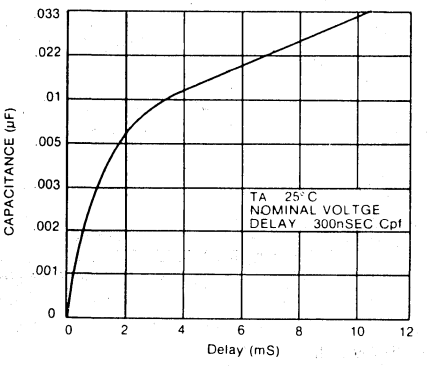


Fig.4 STROBE DELAY vs. C_1

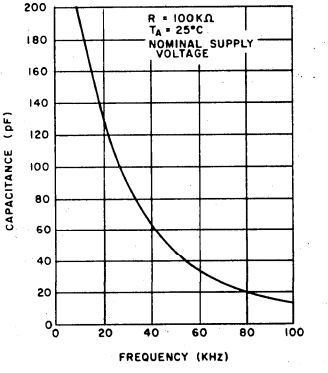


Fig.5 OSCILLATOR FREQUENCY vs. C_2

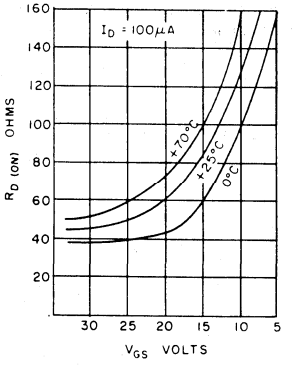


Fig.6 TYPICAL OUTPUT ON RESISTANCE (R_{DON}) vs. GATE BIAS VOLTAGE (V_{GS})

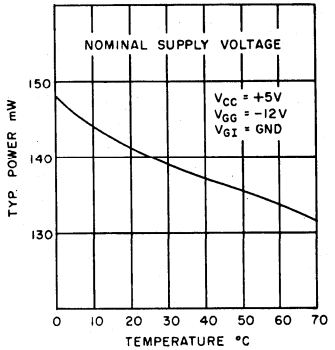
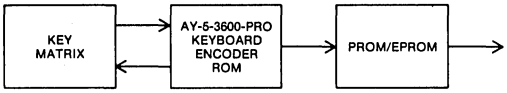


Fig.7 TYPICAL POWER CONSUMPTION (mW)

Keyboard Encoder and PROM/EPROM Application

The AY-5-3600-PRO is pre-programmed during manufacture to provide specific yet simple binary coded outputs thus allowing the purchase of off-the-shelf devices (distributors, etc.). To enhance the device flexibility, the binary outputs have been organized to provide direct interface with a PROM/EPROM.



The PROM (Programmable Read Only Memory) permits the programming of the required output code in the factory or the field within minutes, thus making it extremely suitable for small quantity, fast turnaround keyboard requirements. The EPROM (Erasable Programmable Read Only Memory) is ideally suited for prototyping, where patterns are quite variable, allowing the EPROM to be erased and reprogrammed repeatedly. Similar advantages are realized in the field where pattern changes are necessary in order to respond to redefined requirements or to subtle system peculiarities not previously encountered.

Technical Description

The AY-5-3600-PRO is a binary coded MOS-LSI device programmed to furnish 360 unique 9-bit codes (90 keys × 4 modes × 9 bits). Option selections include such popular functions as Internal Oscillator, Lockout/Rollover and an Any Key Down output. For further, more explicit device characteristics refer to the preceding pages. The internal oscillator is a self contained (on-chip) circuit option which eliminates the need for any external clock source. For applications necessitating an external clock source the internal oscillator input pins may be utilized to function in the slave mode of operation. Lockout or Rollover is selectable via an input pin, thus allowing the versatility required on various keyboard applications. The Any Key Down output performs the function of a gating signal by acknowledging both a key depression and release, making it a convenient signal for use in a repeat application.

For ease of translation, each key is assigned an X-Y coordinate and, in turn, each X-Y coordinate has been identified with a specific yet simple binary coded output. Two formats are described: the first for application with a 64 key 4 mode keyboard and the second for a 90 key 4 mode keyboard.

The 64 key 4 mode application as illustrated in Fig. 8 utilized keyboard encoder addresses X0 Y0 thru X6 Y3. A unique combination of one input (Y) and one output (X) is assigned to each key, for a total coverage of 64 keys. Binary coded outputs B2-B9 have been arranged to provide the necessary 8-bit address inputs to the PROM/EPROM, with B2 and B3 representing the variable mode identification and B4-B9 each specific key closure.

When a key is depressed a path is completed between one X line and one Y line thus addressing that specific X-Y ROM coordinate in the AY-5-3600-PRO. The 8-bit binary code for that X-Y location (ref. Truth Table page 14-15) is transferred into a one character 8-bit output latch (B2-B9) thus providing the appropriate 8-bit address to the 256 x 8 PROM/EPROM.

Expansion to a 90 key 4 mode operation (see Fig. 9) is identical to the 64 key 4 mode except: the 90 key 4 mode version utilizes the full complement of addresses X0 Y0 thru X8 Y9 (90 keys). The 8-bit binary code (B2-B9) previously produced to address the 256 x 8 PROM/EPROM is now expanded to a 9-bit binary code (B1-B9) for addressing to a 512 x 8 PROM/EPROM. With expansion to a 90 key 4 mode application outputs B1-B3 now serve as the variable mode identification.

The interface to a PROM/EPROM enables the custom programming of the required output data in the PROM/EPROM to directly coincide to the specific address inputs from the AY-5-3600-PRO. Any PROM whether it be bipolar, ultraviolet erasable or electrically alterable, may be employed to provide a wide variety of "off-the-shelf" keyboards. Once the keyboard assembly has gone beyond the prototyping stage, and assuming the quantity/cost permit, the PROM/EPROM data can be converted to the standard AY-5-3600 data format (ref. AY-5-3600 Custom Coding Information sheet) and produced in production quantities. This eliminates the PROM/EPROM expense while assuring the absence of undefined coding changes.

Summary of Important Features

- Ability to deliver complete keyboard assemblies within days without sacrificing the features offered in the AY-5-3600 Keyboard Encoder
- Ability to buy off-the-shelf devices (distributor, etc.)
- Ability to verify the specific pattern format using a PROM/EPROM prior to a 'custom' encoder commitment

NORMAL

X	Y	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9
0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	2	0	0	0	0	0	0	0	1	0
0	3	0	0	0	0	0	0	0	1	1
0	4	0	0	0	0	0	0	1	0	0
6	3	0	0	0	1	1	1	1	1	1

6 OF 8 Bit ADDRESS

MODE IDENT. ILLUSTRATED USING NORMAL MODE ONLY, FOR REMAINING MODES REFER TO TRUTH TABLE

64 x 4 BLOCK DIAGRAM

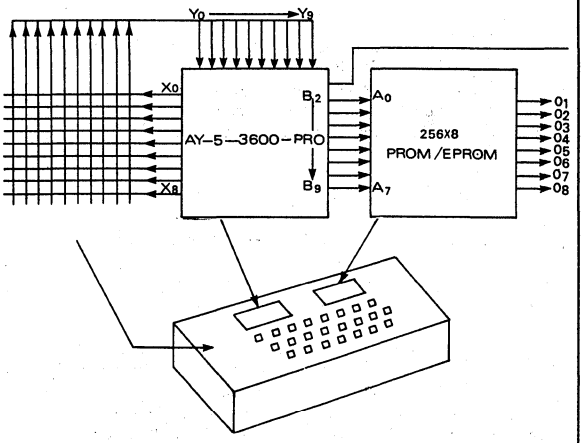


Fig.8 64 KEY 4 MODE KEYBOARD APPLICATION

NORMAL

X	Y	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	B_9
0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	2	0	0	0	0	0	0	0	1	0
0	3	0	0	0	0	0	0	0	1	1
0	4	0	0	0	0	0	0	1	0	0
8	9	1	0	0	0	1	1	0	0	1

6 OF 9 Bit ADDRESS

MODE IDENT. ILLUSTRATED USING NORMAL MODE ONLY, FOR REMAINING MODES REFER TO TRUTH TABLE

90 x 4 BLOCK DIAGRAM

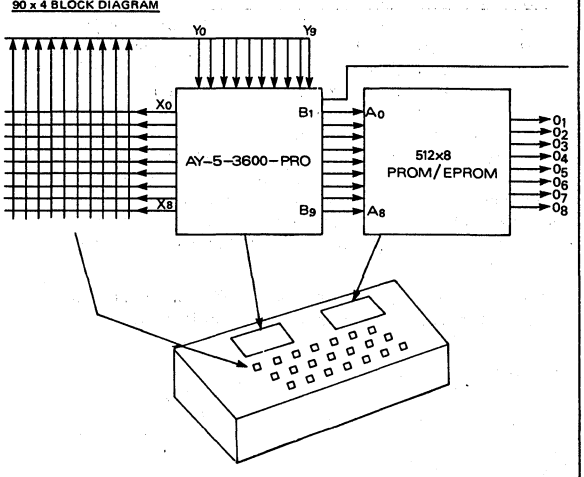


Fig.9 90 KEY 4 MODE KEYBOARD APPLICATION

OPTIONS

- Device Marking: AY-5-3600-PRO
- Internal Oscillator on Pin Nos. 1, 2, 3
- Lockout/Rollover on Pin No. 4
  Internal Resistor to V_{DD} on Lockout/Rollover Pin
- True Outputs Only
- Any Key Output on Pin No. 5.
  Any Key Output True (Logic 1) During Key Depression
- Pulse Data Ready Signal
- Plastic Package
- Internal Resistor to V_{DD} on Shift/Control Pin

XY	NORMAL	SHIFT	CONTROL	SHFT/CTR	XY	NORMAL	SHIFT	CONTROL	SHFT/CTR
0	000000000	001000000	010000000	011000000	45	000101101	001101101	010101101	011101101
1	000000001	001000001	010000001	011000001	46	000101110	001101110	010101110	011101110
2	000000010	001000010	010000010	011000010	47	000101111	001101111	010101111	011101111
3	000000011	001000011	010000011	011000011	48	000110000	001110000	010110000	011110000
4	000000100	001000100	010000100	011000100	49	000110001	001110001	010110001	011110001
5	000000101	001000101	010000101	011000101	50	000110010	001110010	010110010	011110010
6	000000110	001000110	010000110	011000110	51	000110011	001110011	010110011	011110011
7	000000111	001000111	010000111	011000111	52	000110100	001110100	010110100	011110100
8	000001000	001001000	010001000	011001000	53	000110101	001110101	010110101	011110101
9	000001001	001001001	010001001	011001001	54	000110110	001110110	010110110	011110110
10	000001010	001001010	010001010	011001010	55	000110111	001110111	010110111	011110111
11	000001011	001001011	010001011	011001011	56	000111000	001111000	010111000	011111000
12	000001100	001001100	010001100	011001100	57	000111001	001111001	010111001	011111001
13	000001101	001001101	010001101	011001101	58	000111010	001111010	010111010	011111010
14	000001110	001001110	010001110	011001110	59	000111011	001111011	010111011	011111011
15	000001111	001001111	010001111	011001111	60	000111100	001111100	010111100	011111100
16	000010000	001010000	010010000	011010000	61	000111101	001111101	010111101	011111101
17	000010001	001010001	010010001	011010001	62	000111110	001111110	010111110	011111110
18	000010010	001010010	010010010	011010010	63	000111111	001111111	010111111	011111111
19	000010011	001010011	010010011	011010011	64	100000000	101000000	110000000	111000000
20	000010100	001010100	010010100	011010100	65	100000001	101000001	110000001	111000001
21	000010101	001010101	010010101	011010101	66	100000010	101000010	110000010	111000010
22	000010110	001010110	010010110	011010110	67	100000011	101000011	110000011	111000011
23	000010111	001010111	010010111	011010111	68	100000100	101000100	110000100	111000100
24	000011000	001011000	010011000	011011000	69	100000101	101000101	110000101	111000101
25	000011001	001011001	010011001	011011001	70	100000110	101000110	110000110	111000110
26	000011010	001011010	010011010	011011010	71	100000111	101000111	110000111	111000111
27	000011011	001011011	010011011	011011011	72	100001000	101001000	110001000	111001000
28	000011100	001011100	010011100	011011100	73	100001001	101001001	110001001	111001001
29	000011101	001011101	010011101	011011101	74	100001010	101001010	110001010	111001010
30	000011110	001011110	010011110	011011110	75	100001011	101001011	110001011	111001011
31	000011111	001011111	010011111	011011111	76	100001100	101001100	110001100	111001100
32	000100000	001100000	010100000	011100000	77	100001101	101001101	110001101	111001101
33	000100001	001100001	010100001	011100001	78	100001110	101001110	110001110	111001110
34	000100010	001100010	010100010	011100010	79	100001111	101001111	110001111	111001111
35	000100011	001100011	010100011	011100011	80	100010000	101010000	110010000	111010000
36	000100100	001100100	010100100	011100100	81	100010001	101010001	110010001	111010001
37	000100101	001100101	010100101	011100101	82	100010010	101010010	110010010	111010010
38	000100110	001100110	010100110	011100110	83	100010011	101010011	110010011	111010011
39	000100111	001100111	010100111	011100111	84	100010100	101010100	110010100	111010100
40	000101000	001101000	010101000	011101000	85	100010101	101010101	110010101	111010101
41	000101001	001101001	010101001	011101001	86	100010110	101010110	110010110	111010110
42	000101010	001101010	010101010	011101010	87	100010111	101010111	110010111	111010111
43	000101011	001101011	010101011	011101011	88	100011000	101011000	110011000	111011000
44	000101100	001101100	010101100	011101100	89	100011001	101011001	110011001	111011001

Capacitive Keyboard Encoder

FEATURES

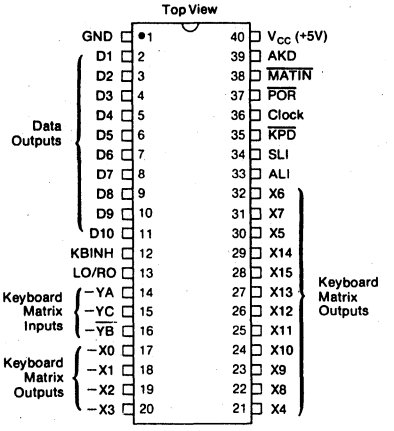
- 128 key keyboard encoder: 112 fully decoded keys, 16 discrete function keys
- 112 keys with 4 modes, 10 bit output
- Key validation logic protects against bounce
- N-key roll over or 2-key roll over
- Internal ROM allows any keys to control SHIFT CTRL, SHIFT LOCK and ALPHA LOCK
- ALPHA LOCK and SHIFT LOCK indicator lines
- Any key down (AKD) strobe
- Single +5 Volt power supply
- Programmable coding of standard and special function keys
- Zener diode protection on all I/O pins
- Low power consumption, less than 2 milliwatts per key
- Usable with capacitive, magnetic, inductive. Hall effect or mechanical keyboard switches
- Inputs and outputs TTL and CMOS compatible
- Internal Oscillator

DESCRIPTION

The G.I. AY-3-4592 is a unique dual pulse scanning encoder and keyboard controller for 112 keys in four modes and 16 programmable discrete function keys. ROM programming permits any keys to control the shift control and lock functions. The AY-3-4592 can be used with capacitive, inductive (magnetic) or switch closure type switches since it works on pulse detection.

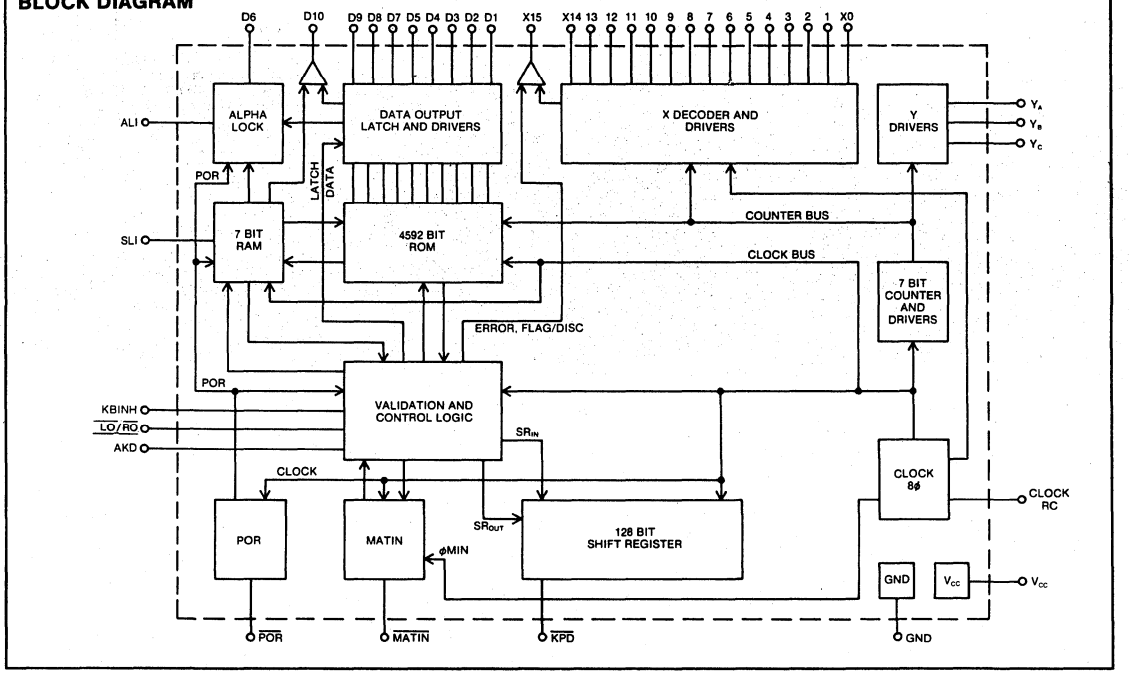
PIN CONFIGURATION

40 LEAD DUAL IN LINE



The AY-3-4592 is fabricated with N-channel MOS technology on a single chip containing a 4592 bit ROM, a 128 bit shift register and an internal oscillator.

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Symbol	Function
1	Ground	GND	Ground Pin
2-10	Data Out	D1-D9	Data Outputs, D1 through D9
11	Data Out	D10	Data Output D10. See "AY-3-4592 options" for complete description
12	Key Inhibit	KBINH	Logic "1" on KBINH will inhibit the processing of Key closures and prevent new output codes. See "AY-3-4592 options" for other custom options
13	Lockout/rollover	LO/RO	High for 2 Key Rollover operation, low for N Key Rollover operation. This input is a high impedance Schmitt trigger with thresholds of approximately ¼ (low) and ¾ (high) of V_{CC}. This allows easy interfacing with very slow RC circuits for such functions as "repeat delay". LO/RO is internally "anded" with AKD/STB; if either is low, N Key rollover is automatically selected.
14-16	Y-Address	YA, YB, YC	Y Address lines select one of eight Y inputs through external multiplexer. Scan sequence is Y7 to Y0
17-27, 30-32	X Outputs	X0-X13, X5-X7	X output drivers for Matrix scanning. Scan sequence is X15 to X0. Each driver generates 8 pairs of pulses each scanning cycle.
28, 29	X15, 14	X15, X14	X15 is programmed as a "discrete output" key in the standard part. Optionally it may be programmed as a error flag or as a Matrix drive line. See "AY-3-4592 options". Unlike X0-X13, neither X14 nor X15 have associated ROM output codes. These lines are used to enable separate discrete keys to be debounced using an addressable latch as illustrated in figure 2.
33	Alpha Lock Indicator	ALI	ALI will indicate if "op code" XX101 is selected. (See operation codes). In the standard device there is no other function. If alpha lock is selected as an option, op code XX101 will result in bit 6 being replaced by bit 9 when a key is depressed.
34	Shift Lock Indicator	SLI	SLI will indicate if "op code" XX011 is selected. (See "operation codes"). In the standard device this op code will also select the shift lock function.
35	Key Pressed	$\overline{KPD}$	$\overline{KPD}$ is used to shift the threshold of the external sense amplifier in order to provide hysteresis to improve noise immunity. In addition $\overline{KPD}$ may be inverted to provide the data input to the 8 bit latches for decoding X14 and X15. When a key closure is detected $\overline{KPD}$ is generated causing the 8 bit latch output to go high. See figure 2.
36	CLOCK	CLK	Resistor/capacitor tie point for the internal oscillator. Nominal frequencies and scan times are shown below:
37	Reset	$\overline{POR}$	Reset clears all internal registers and flip flops. Suggested circuit for power on reset is illustrated in Figure 1.
38	Matrix Input	$\overline{MATIN}$	Input from external multiplexer. Senses signal from X-Y scan of depressed key.
39	Any Key Down Strobe	AKD	AKD is low when no key is depressed. When a key is depresed AKD goes high. If while one key is held, a second key is depressed AKD will go low for 2 clock cycles.
40	Power	V_{CC}	Power supply input; +5 Volts

	C = 150pf		C = 220pf		C = 500pf	
R	Freq	Scan time	Freq	Scan time	Freq	Scan time
5K	1.3 MHz	1.5 msec	1.2 MHz	1.7 msec	.71 MHz	2.8 msec
10K	.8 MHz	2.3 msec	.8 MHz	2.7 msec	.45 MHz	4.3 msec
25K	.4 MHz	4.8 msec	.3 MHz	6.0 msec	.20 MHz	10.0 msec

ROM

OPERATION

Keys are connected in a 16 x 8 matrix. Scanning of the matrix is performed by the encoder in conjunction with an external, multiplexer. The encoder provides a 3 bit binary address (YA, YB, YC) used to scan each of eight possible sense lines (Y-lines). The drive lines (X-lines) are each pulsed low by the encoder. If a key is closed, the pulse is coupled from the drive to the sense lines, amplified and sent to the encoder. When used to encode reactive switches, a detection circuit is necessary between the output of the multiplexer and the $\overline{\text{MATIN}}$ input to the encoder. In this manner, each matrix cross-point is interrogated in turn. Each matrix cross-point is given a unique binary code that is determined by the internal scan counters. This code is used to address a ROM which generates the output codes (such as ASCII or other customer defined codes). The output of the ROM is entered into an output holding register when the key is determined to be a valid key closure. Only the cross-points on X0 through X13 can have output codes: X14 and X15 can be used for scanning discrete keys.

An internal oscillator controls the matrix scanning rate. The minimum scanning time is 1.7 msec, at a 1.2MHz clock. This allows a burst typing speed equivalent to over 250 words/min. When a key is depressed, a matrix address from an X driver and Y input line representing that key is loaded into a 7 bit latch. On the second keyboard scan, the matrix address and the stored address are compared. If the two addresses match, the ROM 10 bit word at that address is loaded into the data holding register. This data remains valid until the next key is depressed. The internal error flag is set, if this option was utilized, whenever there is a mismatch between 7 bit addresses.

Two negative pulses must be detected during the $\overline{\text{MATIN}}$ timing window for the depression to be recognized.

Keyboard Selection

The AY-3-4592 keyboard encoder can be used with a wide variety of available keyboards. An external multiplexing circuit and one external sense amplifier can be tailored to the user's specific requirements. As shown in Figure 1, the sense amplifier detects changes in voltage caused by variations in the switch impedance as a key is depressed and released. Given the key switch impedances for depressed and released states, the values of Rx and Rh can be chosen to guarantee switch closure detection and noise margins. Rx is chosen to match the capacitor or reactor time constants. For example, given a variable capacitance keyboard switch with C1 = 100pf, and C2 = 10pf for depressed and released positions respectively, with a 1.5MHz oscillator and Rx = 10 Kohm, a depressed key would make a 4.7 volt pulse while a raised key would produce a 2.6 volt pulse. The potentiometer would then be set for best noise immunity with minimum pulse width, 90ns for all keys. The hysteresis resistor, Rh, is chosen at roughly ten times the value of Rx to provide increased noise immunity for detected key depressions.

Operation Codes

Depending on the internal programming of the AY-3-4592, keys may have one of three different functions. Keys on matrix lines X0 through X13 have in addition to the output code bits a function flag bit (FFB). If the FFB is programmed as a zero, the key produces a data output when depressed.

When FFB is a one, the key is a "function" key for which bits 1-5 determine the function. These bits are referred to as the "op code" and are used to provide special functions such as shift, shift lock, alpha lock etc. Bits 6-10 are not used.

Op codes may be programmed to provide data outputs as well as change the mode of operation. Data when outputted is not latched as are normal coded outputs.

Bits 1-3 indicate what operation the key will perform; per table 1.

Bit 4 programmed as one indicates a "down-coded" key, for which the 10 data bits programmed in the shift mode level of ROM are outputted when the key is depressed.

Bit 5 programmed as one indicates an "up-coded" key for which the 10 data bits programmed in the control mode level of ROM are outputted when the key is released.

Neither bit 4 nor 5 will have any effect on the operational control of bits 10-3.

Table 1

Op-Code					Function
5	4	3	2	1	
X	X	0	0	0	Function key (with up/down codes)*
X	X	0	0	1	Right Shift Key
X	X	0	1	0	Left Shift Key
X	X	0	1	1	Shift Lock Key or Discrete Key (output SLI)
X	X	1	0	0	Control Key
X	X	1	0	1	Alpha Lock Key or Discrete Key (output ALI)
X	0	1	1	0	Error Reset Key or discrete key (output X15)
X	X	1	1	1	Discrete Key (output D10)

*If the op-code is 00000 the key has no internal function but $\overline{\text{KPD}}$ will go low when it is processed.

OPTIONS

Pin or Function	Option
X15	X15 may be programmed as 1) an X-output to provide a second set of 8 discrete lines 2) a "discrete output" which indicates when a function key with op code XX110 is depressed 3) an Error Flag Indicator (EFI). See "Error Flag" In the AY-3-4592 STD X15 is a discrete output
Error Flag	When this option is selected, the AY-3-4592 has the capability of detecting multiple key depressions during the same scan cycle. When selected, the error flag may be programmed to generate KBINH and or appear at the X15 output. The error flag may be reset by three methods. If the "automatic reset" is selected/the flag will be reset when the error causing Key is released. Op-code XX110 may be programmed on a function key to reset the error flag. If pin 12 is programmed for KBINH error flag will be reset by pulsing pin 12 high. The reset will occur on the negative edge of the KBINH signal; the pulse must be at least 16 clock cycles. In the AY-3-4592 STD, error flag causes KBINH and is automatically reset.
Alpha Lock	When programmed for Alpha lock, the function key with op-code XX101 will cause the bit 6 output to be replaced by bit 9. Bit 9 is not altered. Alpha lock is normally used to force printing of upper case characters irrespective of the shift function. Op Code XX101 will also cause an output on ALI (pin 33). When Alpha lock is not programmed, op code XX101 will simply result in an output on ALI (pin 33). Op code XX101 may be programmed for momentary action, or latched push-on, push-off alternating action. ALI may be programmed for normally low or high output. Op code XX101 is momentary action. ALI is normally low. The AY-3-4592 STD is not programmed for Alpha lock, although there will be an output on ALI.
Shift Lock	When programmed for shift lock, the function key with op-code XX011 will cause normal electronic shift action. Op code XX011 will also cause an output on SLI (pin 34). If shift lock is not programmed, op code XX011 will simply cause an output on SLI. SLI may be programmed for normally low or high output. The AY-3-4592 STD is programmed for shift lock operation with SLI normally low.
KBINH	KBINH, Keyboard Inhibit, may be programmed to be caused by Pin 12 high, by the error flag, or both. In addition, function keys with up or down codes may be programmed, as a group, to be inhibited by KBINH. This is the "KCI Out" option. When pin 12 is programmed to cause KBINH, a "high" input on pin 12 will inhibit processing of common keys. If a key is depressed while the KBINH signal is present, output and output strobe will be generated when KBINH is released. The AY-3-4592 STD has KBINH actuated by pin 12 high, and by the error flag. The "KCI In" option is used, that is, the function key operation is independent of KBINH.
D10	D10, pin 11, may be programmed as the output for the memory bit 10 or as a "discrete" output. As a discrete output pin 10 is switched from its normal state (programmable as high or low) by the function key with op-code XX111. The AY-3-4592 STD is programmed for D10 as a discrete key, normally low.
Key Type	Keys may be either normally open or normally closed. The AY-3-4592 STD is designed for normally open keys.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} ..... -0.3 Volts to +7.0 Volts
Maximum voltage with respect to V_{CC} ..... +0.3 Volts
Storage Temperature ..... 65°C to +150°C
Operating Temperature ..... 0 to 70°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

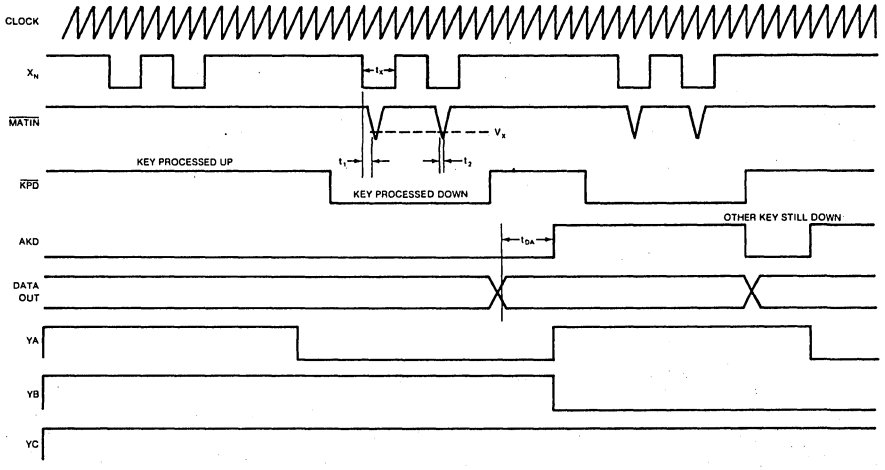
Standard Conditions (unless otherwise noted)

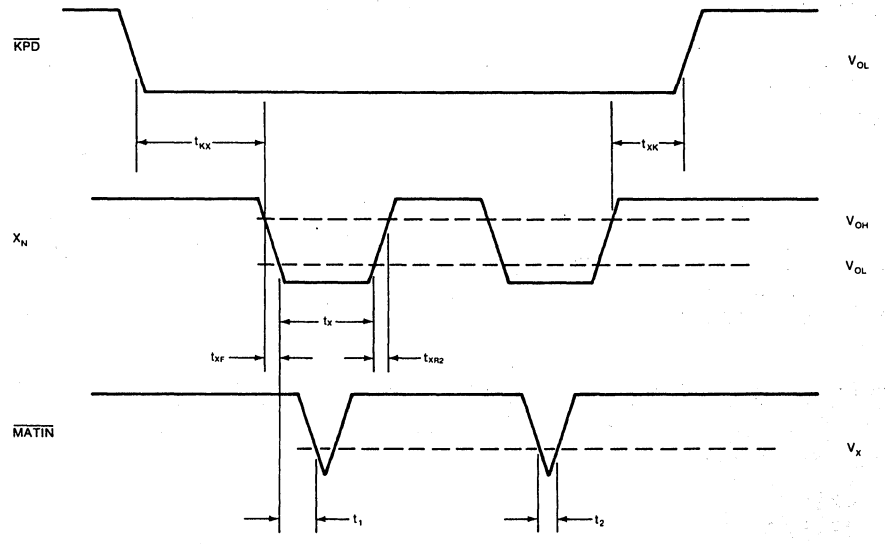
V_{CC} = 5.0V ±5%
T_A = 0° to 70°C

Characteristic	Symbol	Min.	Typ.**	Max.	Unit	Condition
Data Output "1" Voltage	V_{OH}	3.5	-	-	V	I_{OH} = 50μA, 25pF
Data Output "0" Voltage	V_{OL}	-	-	0.5	V	I_{OL} = 1.6mA
All Inputs "1" Voltage	V_{IH}	2.2	-	-	V	except $\overline{POR}$, 2KRO
All Inputs "0" Voltage	V_{IL}	-	-	0.8	V	except $\overline{POR}$, 2KRO
All Inputs Leakage	I_{IH}	-	-	10	μA	V_{in} = 5V
X Output "1" Voltage	X_{OH}	3.5	-	-	V	I_{OH} = 50μA, 100pF
X Output "0" Voltage	X_{OL}	-	-	0.5	V	I_{OL} = 1.6mA
AKd Output Voltage	V_A	-	-	0.6	V	I_{OL} = 3.2mA
$\overline{MATIN}$ Input Voltage	V_X	-	-	0.4	V	
$\overline{POR}$, 2KRO high threshold	V_{SH}	-	1.3	-	V	Schmitt trigger
$\overline{POR}$, 2KRO low threshold	V_{SL}	-	3.7	-	V	Schmitt trigger
Power Supply Current	I_{CC}	-	35	60	mA	Vcc = 5.3V
Clock Frequency	ϕ	200	-	1200	kHz	
Matrix Delay	t_1	-	-	250	ns	
Input pulse width	t_2	90	-	-	ns	
X Output pulse width	t_x	1.7	-	-	μs	
X Output fall time	t_{XF}	-	-	150	ns	V_{OH} = 4.3V, V_{OL} = 0.4V
X Output rise time	t_{XR1}	-	-	150	ns	V_{OH} = 2.4V, V_{OL} = 0.4V
X Output rise time	t_{XR2}	-	-	500	ns	V_{OH} = 3.5V, V_{OL} = 0.4V
X Output rise time	t_{XR3}	-	-	1500	ns	V_{OH} = 4.3V, V_{OL} = 0.4V
$\overline{KPD}$-X Output set time	T_{KX}	500	-	-	ns	
X Output-$\overline{KPD}$ hold time	t_{XK}	100	-	-	ns	
Data out to AKD time	t_{OA}	1.7	-	-	μs	

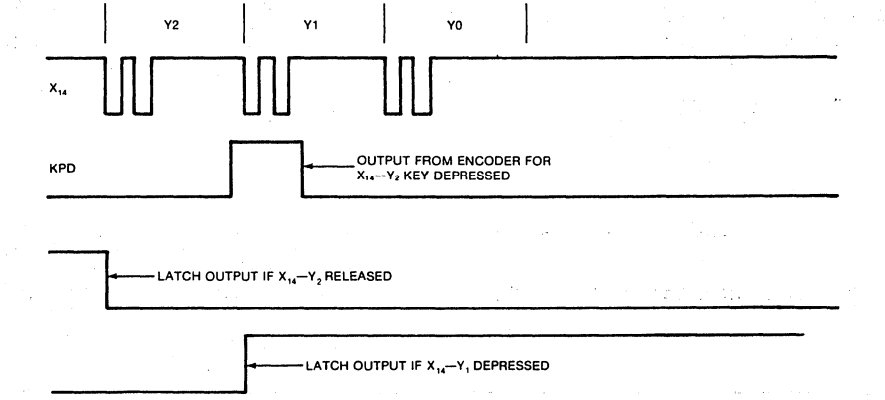
**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS





Discrete Function Key



CODE CHART / AY-3-4592-STD

XXY	F	NORMAL			SHIFT			CONTROL			SHIFT/CONTROL		
	B	HEX	BINARY		HEX	BINARY		HEX	BINARY		HEX	BINARY	
000	1	001	0000000001	Right Shift	3FF	1111111111		3FF	1111111111		3FF	1111111111	
001	1	002	0000000010	Left Shift	3FF	1111111111		3FF	1111111111		3FF	1111111111	
002	1	003	0000000011	Shift Lock	3FF	1111111111		3FF	1111111111		3FF	1111111111	
003	1	004	0000000100	Control	3FF	1111111111		3FF	1111111111		3FF	1111111111	
004	1	005	0000000101	ALI	3FF	1111111111		3FF	1111111111		3FF	1111111111	
005	1	006	0000000110	X15	3FF	1111111111		3FF	1111111111		3FF	1111111111	
006	1	007	0000000111	D10	3FF	1111111111		3FF	1111111111		3FF	1111111111	
007	0	0CE	0011001110	1	0DE	0011011110	!	0CE	0011001110	!	0DE	0011011110	!
010	0	1E4	0111100100	ESC	1E4	0111100100	ESC	1E4	0111100100	ESC	1E4	0111100100	ES
011	0	0CD	0011001101	2	1BF	0110111111	@	0CD	0011001101	2	1FF	0111111111	NUL
012	0	0CD	0011001101	2	0DD	0011011101	"	0CD	0011001101	2	0DD	0011011101	"
013	0	1B8	0110001000	W	1A8	0110101000	W	1E8	0111101000	ETB	1E8	0111101000	ETB
014	0	1BE	0110001110	9	1AE	0110101110	Q	1EE	0111101110	DC1	1EE	0111101110	DC1
015	0	1BC	0110001100	S	1AC	0110101100	S	1EC	0111101100	DC3	1EC	0111101100	DC3
016	0	19E	0110011110	a	18E	0110111110	A	1FE	0111111110	SOH	1FE	0111111110	SOH
017	0	185	0110000101	Z	1A5	0110100101	Z	1E5	0111100101	SUB	1E5	0111100101	SUB
020	0	17F	0101111111	NUL	17F	0101111111	NUL	17F	0101111111	NUL	17F	0101111111	NUL
021	0	0CB	0011001011	4	0DB	0011011011	$	0CB	0011001011	4	0DB	0011011011	$
022	0	0CC	0011001100	3	0DC	0011011100	#	0CC	0011001100	3	0DC	0011011100	#
023	0	1AD	0110001101	r	1AD	0110101101	R	1ED	0111101101	DC2	1ED	0111101101	DC2
024	0	19A	0110011010	e	18A	0110111010	E	1FA	0111111010	ENQ	1FA	0111111010	ENQ
025	0	198	0110011011	d	18B	0110111011	D	1FB	0111111011	EOT	1FB	0111111011	EOT
026	0	187	0110000111	x	1A7	0110100111	X	1E7	0111100111	ETB	1E7	0111100111	ETB
027	0	19C	0110011100	c	18C	0110111100	C	1FC	0111111100	ETX	1FC	0111111100	ETX
030	0	17E	0101111110	SOH	17E	0101111110	SOH	17E	0101111110	SOH	17E	0101111110	SOH
031	0	17D	0101111101	STX	17D	0101111101	STX	17D	0101111101	STX	17D	0101111101	STX
032	0	0CA	0011001010	5	0DA	0011011010	%	0CA	0011001010	5	0DA	0011011010	%
033	0	1AB	0110101011	t	1AB	0110101011	T	1EB	0111101011	DC4	1EB	0111101011	DC4
034	0	199	0110011001	f	1B9	0110111001	F	1F9	0111111001	ACK	1F9	0111111001	ACK
035	0	198	0110011000	g	1B8	0110111000	G	1F8	0111111000	BEL	1F8	0111111000	BEL
036	0	189	0110001001	v	1A9	0110101001	V	1E9	0111101001	SYN	1E9	0111101001	SYN
037	0	19D	0110011101	b	1BD	0110111101	B	1FD	0111111101	STX	1FD	0111111101	STX
040	0	17C	0101111100	ETX	17C	0101111100	ETX	17C	0101111100	ETX	17C	0101111100	ETX
041	0	0C8	0011001000	7	0D9	0011011001	(	0C8	0011001000	7	0D9	0011011001	(
042	0	0C9	0011001001	6	0D9	0011011001	(	0C9	0011001001	6	0D9	0011011001	(
043	0	186	0110000110	y	1A6	0110100110	Y	1E6	0111100110	EM	1E6	0111100110	EM
044	0	197	0110010111	h	1B7	0110110111	H	1F7	0111110111	BS	1F7	0111110111	BS
045	0	191	0110010001	n	1B1	0110110001	N	1F1	0111110001	SO	1F1	0111110001	SO
046	0	0C9	0011001001	6	0C3	0011000011	<	0C9	0011001001	6	0C3	0011000011	<
047	0	0DF	0011011111	SP	0DF	0011011111	SP	0DF	0011011111	SP	0DF	0011011111	SP
050	0	17B	0101111011	EOT	17B	0101111011	EOT	17B	0101111011	EOT	17B	0101111011	EOT
051	0	0C7	0011000111	8	0D5	0011010101	*	0C7	0011000111	8	0D5	0011010101	*
052	0	0C8	0011001000	7	0D8	0011011000	'	0C8	0011001000	7	0D8	0011011000	'
053	0	18A	0110001010	u	1AA	0110101010	U	1EA	0111101010	NAK	1EA	0111101010	NAK
054	0	195	0110010101	J	1B5	0110110101	J	1F5	0111110101	ENQ	1F5	0111110101	ENQ
055	0	194	0110010100	k	1B4	0110110100	K	1F4	0111110100	VT	1F4	0111110100	VT
056	0	192	0110010010	m	1B2	0110110010	M	1F2	0111110010	CR	1F2	0111110010	CR
057	0	0D3	0011010011	,	0C3	0011000011	<	0D3	0011010011		0C3	0011000011	<
060	0	17A	0101111010	ENQ	17A	0101111010	ENQ	17A	0101111010	ENQ	17A	0101111010	ENQ
061	0	0C6	0011000110	9	0D7	0011010111	(	0C6	0011000110	9	0D7	0011010111	(
062	0	0C7	0011000111	8	0D7	0011010111	(	0C7	0011000111	8	0D7	0011010111	(
063	0	196	0110010110	i	1B6	0110110110	I	1F6	0111110110	HT	1F6	0111110110	HT
064	0	190	0110010000	o	1B0	0110110000	O	1F0	0111110000	SI	1F0	0111110000	SI
065	0	194	0110010100	K	1A4	0110100100	[	1F4	0111110100	VT	1E4	0111100100	ESC
066	0	193	0110010011	l	1B3	0110110011	L	1F3	0111110011	FF	1F3	0111110011	FF
067	0	192	0110010010	m	1A2	0110100010	]	1F2	0111110010	CR	1E2	0111100010	GS
070	0	179	0101111001	ACK	179	0101111001	ACK	179	0101111001	ACK	179	0101111001	ACK
071	0	0CF	0011001111	∯	0D6	0011010110	)	0CF	0011001111	∯	0D6	0011010110	)
072	0	0C6	0011000110	9	0D6	0011010110	)	0C6	0011000110	9	0D6	0011010110	)
073	0	178	0101111000	BEL	178	0101111000	BEL	178	0101111000	BEL	178	0101111000	BEL

CODE CHART / AY-3-4592-STD

XXY	F B	NORMAL HEX	NORMAL BINARY		SHIFT HEX	SHIFT BINARY		CONTROL HEX	CONTROL BINARY		SHIFT/CONTROL HEX	SHIFT/CONTROL BINARY	
074	0	18F	01100011111	P	1AF	01101011111	P	1EF	01111011111	DLE	1EF	01111011111	DLE
075	0	0C4	00110001000	;	0C5	00110001101	:	0C4	00110001000	;	0C5	00110001101	:
076	0	193	01100100011	L	1A3	01101001011	\	1F3	01111100011	FF	1E3	01111000011	FS
077	0	0D1	00110100001	.	0C1	00110000001	>	0D1	00110100001	.	0C1	00110000001	>
080	0	0D2	00110100010	–	1A0	01101000000	~	0D2	00110100010	–	1A0	01101000000	~
081	0	191	01100100001	n	1A1	01101000001	^	1F1	01111100001	SI	1E1	01111000001	RS
082	0	18F	01100011111	P	1BF	01101111111	@	1EF	01111011111	DLE	1FF	01111111111	NUL
083	0	1A4	01101001000	[	1A2	01101000010	]	1E4	01111001000	ESC	1E2	01111000010	GS
084	0	0D8	00110110000	'	0DD	00110111101	"	0D8	00110110000	'	0DD	00110111101	"
085	0	0C4	00110001000	;	0D4	00110101000	+	0C4	00110001000	;	0D4	00110101000	+
086	0	0D0	00110100000	/	0C0	00110000000	?	0D0	00110100000	/	0C0	00110000000	?
087	0	177	01011101111	BS	177	01011101111	BS	177	01011101111	BS	177	01011101111	BS
090	0	0C2	00110000010	=	0D4	00110101000	+	0C2	00110000010	=	0D4	00110101000	+
091	0	0C5	00110001101	:	0D5	00110101101	*	0C5	00110001101	:	0D5	00110101101	*
092	0	176	01011101110	HT	176	01011101110	HT	176	01011101110	HT	176	01011101110	HT
093	0	1A3	01101001011	\	0B3	00101100011	!	1E3	01111001011	FS	1E3	01111001011	FS
094	0	175	01011101101	LF	175	01011101101	LF	175	01011101101	LF	175	01011101101	LF
095	0	1A4	01101001000	[	0B4	00101101000	[	1E4	01111001000	ESC	1E4	01111001000	ESC
096	0	1F2	01111110010	CR	1F2	01111110010	CR	1F2	01111110010	CR	1F2	01111110010	CR
097	0	1A2	01101001010	]	0B2	00101100010	}	1E2	01111001010	GS	1E2	01111001010	GS
100	0	080	00100000000	DEL	080	00100000000	DEL	080	00100000000	DEL	080	00100000000	DEL
101	0	174	01011101000	VT	174	01011101000	VT	174	01011101000	VT	174	01011101000	VT
102	0	0D2	00110100010	_	1A0	01101000000	_	1E0	01111000000	US	1E0	01111000000	US
103	0	173	01011100011	FS	173	01011100011	FS	173	01011100011	FS	173	01011100011	FS
104	0	1F5	01111101101	LF	1F5	01111101101	LF	1F5	01111101101	LF	1F5	01111101101	LF
105	0	1BF	01101111111	@	1A3	01101001011	\	1FF	01111111111	NUL	1FF	01111111111	NUL
106	0	1A1	01101000001	^	0B1	00101100001	~	1E1	01111000001	RS	1E1	01111000001	RS
107	0	1A0	01101000000	_	0C2	00110000010	=	1A0	01101000000	_	0C2	00110000010	=
110	0	172	01011100010	CR	172	01011100010	CR	172	01011100010	CR	172	01011100010	CR
111	0	1F6	01111101110	HT	1F6	01111101110	HT	1F6	01111101110	HT	1F6	01111101110	HT
112	0	0D2	00110100010	-	0C2	00110000010	=	0D2	00110100010	–	0C2	00110000010	=
113	0	171	01011100001	SO	171	01011100001	SO	171	01011100001	SO	171	01011100001	SO
114	0	190	01100100000	o	1A0	01101000000	~	1F0	01111100000	SI	1E0	01111000000	US
115	0	1A4	01101001000	[	1A2	01101000010	]	1A4	01101001000	[	1A2	01101000010	]
116	0	1F7	01111101111	BS	1F7	01111101111	BS	1F7	01111101111	BS	1F7	01111101111	BS
117	0	160	01011000000	US	160	01011000000	US	160	01011000000	US	160	01011000000	US
120	0	170	01011100000	SI	170	01011100000	SI	170	01011100000	SI	170	01011100000	SI
121	0	0C8	00110010000	7	0C8	00110010000	7	0C8	00110010000	7	0C8	00110010000	7
122	0	1F4	01111101000	VT	1F4	01111101000	VT	1F4	01111101000	VT	1F4	01111101000	VT
123	0	16F	01011011111	DLE	16F	01011011111	DLE	16F	01011011111	DLE	16F	01011011111	DLE
124	0	0CB	00110010011	4	0CB	00110010011	4	0CB	00110010011	4	0CB	00110010011	4
125	0	0D3	00110100011	,	0D3	00110100011	,	0D8	00110110000	'	0D3	00110100011	,
126	0	0CE	00110011110	I	0CE	00110011110	1	0CE	00110011110	I	0CE	00110011110	I
127	0	0CF	00110011111	ø	0CF	00110011111	ø	0CF	00110011111	ø	0CF	00110011111	0
130	0	16E	01011011110	DC1	16E	01011011110	DC1	16E	01011011110	DC1	16E	01011011110	DC1
131	0	0C6	00110001110	9	0C6	00110001110	9	0C6	00110001110	9	0C6	00110001110	9
132	0	0C7	00110001111	8	0C7	00110001111	8	0C7	00110001111	8	0C7	00110001111	8
133	0	0CA	00110010010	5	0CA	00110010010	5	0CA	00110010010	5	0CA	00110010010	5
134	0	0C9	00110010001	6	0C9	00110010001	6	0C9	00110010001	6	0C9	00110010001	6
135	0	0CD	00110011101	2	0CD	00110011101	2	0CD	00110011101	2	0CD	00110011101	2
136	0	0CC	00110011100	3	0CC	00110011100	3	0CC	00110011100	3	0CC	00110011100	3
137	0	0D1	00110100001		0D1	00110100001		0D1	00110100001	.	0D1	00110100001	

OPTIONS ARE: Error Flag — Programmed
X15 — Discrete output, normally low
KBINH — Set by high on pin 12 or error flag. Function keys not inhibited by KBINH
Error Flag — Reset by releasing error-causing key
Shift Lock — Operational. SLI normally low
Alpha Lock — Inhibited. ALI normally low, set by OP code XX101
D10 — Discrete output, normally low
Key Type — Normally open

NOTE: Bit 9 — Programmed to allow alpha lock implementation using external logic
Bit 8 — Programmed low for "mono mode" keys, for which the output is the same in all modes.
Bits 1-7 — "Inverted" ASCII data bits

ROM

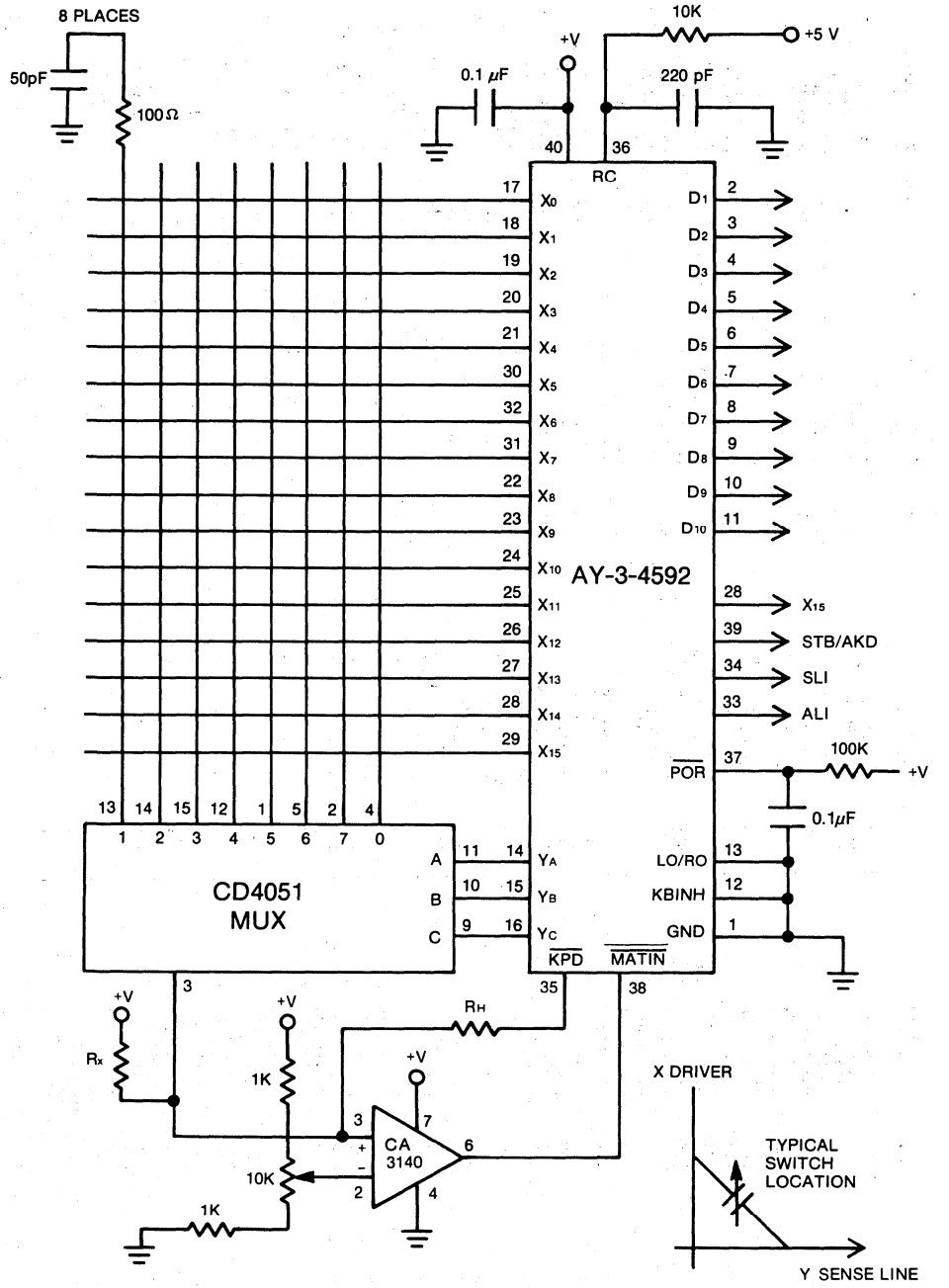


Fig. 1 SAMPLE KEYBOARD DESIGN ROM CODED KEYS

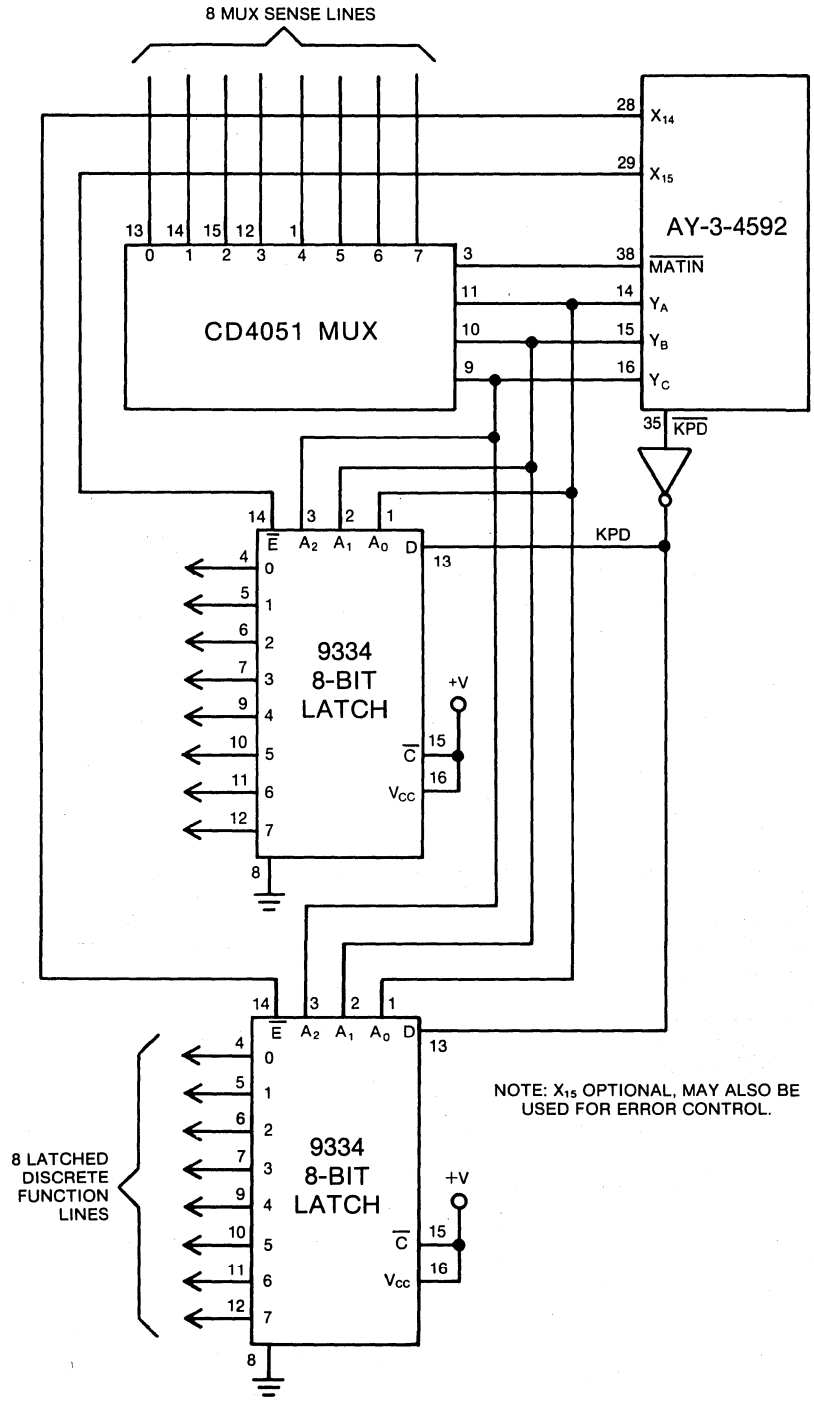


Fig. 2 SAMPLE KEYBOARD DESIGN DISCRETE FUNCTION KEYS

GENERAL INSTRUMENT

Character Generator

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
CHARACTER GENERATOR	2,560 bits organized as 64 - 5 x 8 characters.	RO-3-2513	3-44

Character Generator

FEATURES

- 64 x 8 x 5 Organization—ideal for systems requiring a row scan 5 x 7 dot matrix character generator
- Single +5 Volt Supply
- TTL Compatible — all inputs and outputs
- Static Operation — no clocks required
- 450ns Maximum Access Time
- 175mW Maximum Power
- Three-State Outputs — under the control of an 'Output Inhibit' input to simplify memory expansion
- Standard ASCII (RO-3-2513/CGR-001) or Totally Automated Custom Programming Available
- Zener Protected Inputs
- Glass Passivation Protection

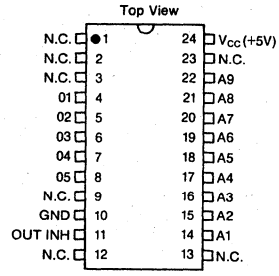
DESCRIPTION

The General Instrument RO-3-2513 is a 2560 bit static Read-Only Memory organized as 512 five bit words and is ideally suited for use as a Character Generator. Fabricated in General Instrument's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-2513 can store, for high speed raster scan CRT displays, a full 64 characters in a standard 5 x 7 dot matrix format.

The RO-3-2513 is available pre-programmed with ASCII encoded 5 x 7 characters (General Instrument's part no. RO-3-2513/CGR-001) a direct replacement in pin connection, operation, and character font for the Signetics 2513/CM2140. The RO-3-2513 is also available preprogrammed with lower case ASCII encoded 5 x 7 characters (General Instrument's part no. RO-3-2513/CGR-005), a direct replacement for the Signetics 2513/CM3021.

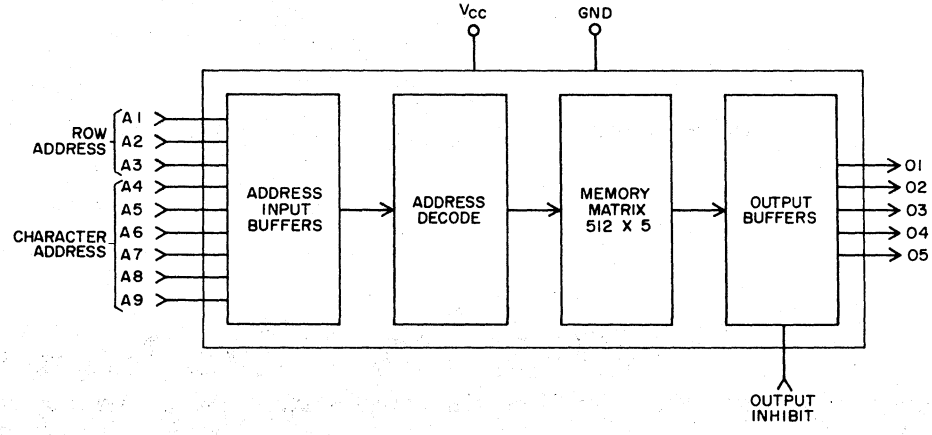
PIN CONFIGURATION

24 LEAD DUAL IN LINE



A separate publication, "RO-3-2513 Custom Coding Information," available from General Instrument's Sales Offices, describes the punched card and truth table format for custom programming of the RO-3-2513 memory.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage to this device. Functional operation at these conditions is not implied—operating conditions are specified below.

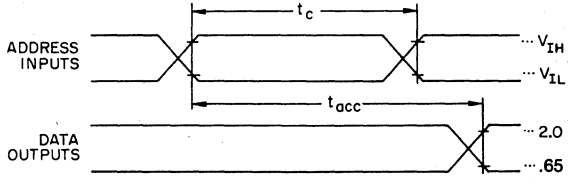
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, $C_{L\ TOTAL}$ = 50pF.

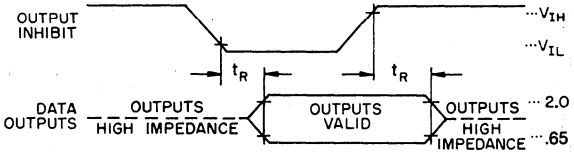
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
I_{CC}	—	—	25	33	mA	Outputs open
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	400	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Data Outputs						
Access Time	t_{ACC}	75	250	450	ns	
Inhibit Response Time	t_R	—	150	200	ns	
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



A. ACCESS TIME (ADDRESS TO OUTPUT-OUTPUT INHIBIT AT LOGIC '0')



B. INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

RO-3-2513-001 STANDARD PATTERN CHARACTER FORMAT (Upper Case ASCII)

The RO-3-2513/CGR-001 is a pre-programmed version of the RO-3-2513 series with ASCII encoding and the character font shown below. A logic "1" represents an input or output voltage nominally equal to Vcc (+5V) and a logic "0" represents a voltage nominally equal to GND (0V).

An example demonstrating the correspondence of device outputs and addressing sequence to the 5 x 7 dot matrix font is shown below:

CHARACTER ADDRESS

RO-3-2513/CGR-001 Address Bit	A9	A8	A7	A6	A5	A4
ASCII Bit	6	5	4	3	2	1
ASCII upper case "S" Character	0	1	0	0	1	1

ROW ADDRESS

A_3	A_2	A_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

OUTPUTS

O_5	O_4	O_3	O_2	O_1
0	0	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	0	0
0	1	1	1	0
0	0	0	0	1
1	0	0	0	1
0	1	1	1	0

RO-3-2513/CGR-001 CHARACTER ADDRESS A_6 A_5 A_4	A_9 A_8 A_7 0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0 0 0								
0 0 1								
0 1 0								
0 1 1								
1 0 0								
1 0 1								
1 1 0								
1 1 1								

RO-3-2513-005 STANDARD PATTERN CHARACTER FORMAT (Lower Case ASCII)

The RO-3-2513/CGR-005 is a pre-programmed version of the RO-3-2513 series with ASCII encoding and the character font shown below. A logic "1" represents an input or output voltage nominally equal to Vcc (+5V) and a logic "0" represents a voltage nominally equal to GND (0V).

An example demonstrating the correspondence of device outputs and addressing sequence to the 5 x 7 dot matrix font is shown below:

CHARACTER ADDRESS

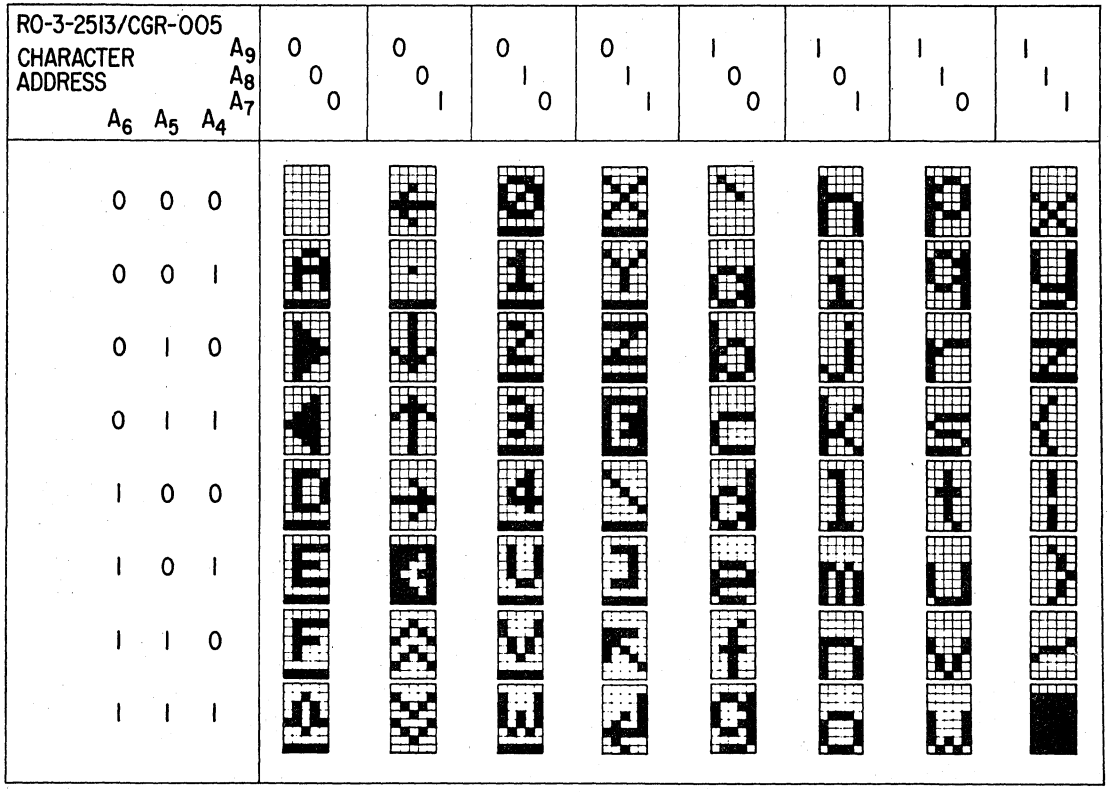
RO-3-2513/CGR-005 Address Bit	A9	A8	A7	A6	A5	A4
ASCII Bit	6	5	4	3	2	1
ASCII lower case 's' Character	1	1	0	0	1	1

ROW ADDRESS

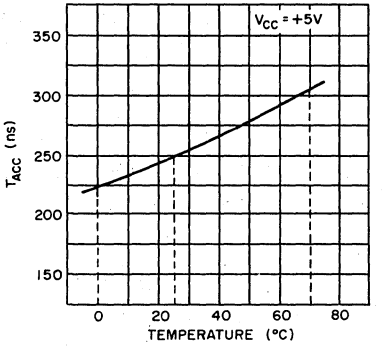
A3	A2	A1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

OUTPUTS

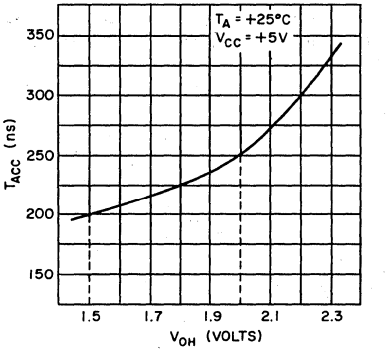
05	04	03	02	01
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	1	1	1	1
1	0	0	0	0
0	1	1	1	0
0	0	0	0	1
1	1	1	1	0



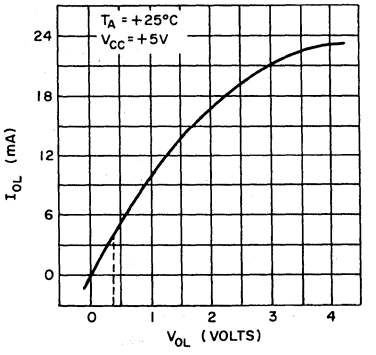
TYPICAL CHARACTERISTIC CURVES



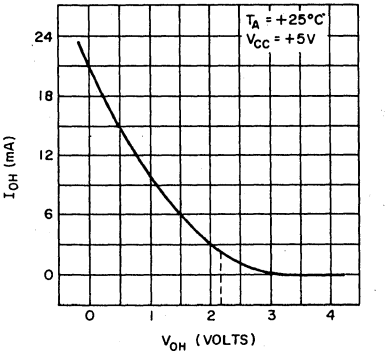
ACCESS TIME vs. TEMPERATURE



ACCESS TIME vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

EAROM 4

Electrically Alterable Read Only Memories including Industrial/Military EAROMs 4-3

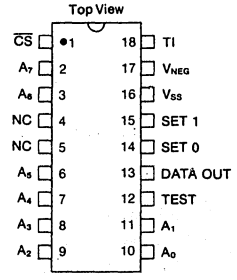
82 Bit Electrically Alterable Read Only Memory

FEATURES

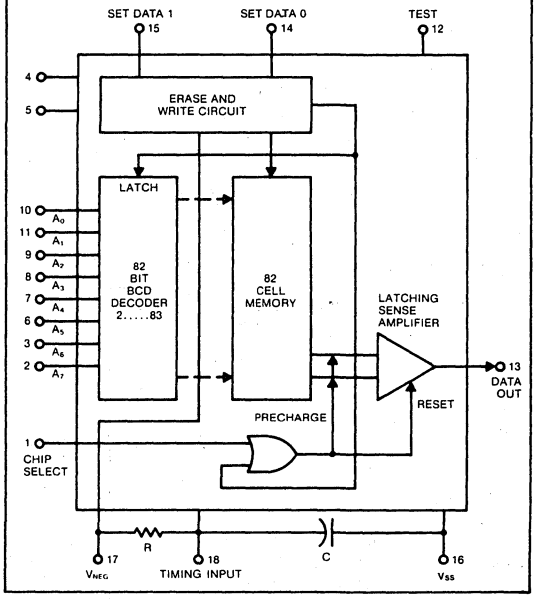
- 82 x 1 bit organization
- Addressing by two 4-bit BCD-digits
- +5, −30V power supplies
- Set inputs have debounce circuits
- Bit erasable
- 100 μsec Read Access Time
- Minimum Data Retention, 7 years unpowered, 2 years powered
- P-Channel output transistor, open drain, pull down resistor
- Control, Address and Data Inputs TTL or CMOS compatible
- Ideally suited for T.V. receiver channel selection

PIN CONFIGURATION

18 LEAD DUAL IN-LINE



BLOCK DIAGRAM



DESCRIPTION

The ER0082 is a 82 x 1 bit electrically alterable read only memory. This device can be used as part of a television receiver tuner control system. The memory is programmed by the user to maintain a record of channels the user wishes to be tuned, and is non-volatile in that the information stored within is not affected by the condition of or the sequencing of power supplied to the chip.

OPERATION

Memory Address

The address is provided by two positive logic binary coded decimal (BCD) digits, LSD (A_0-A_3) and MSD (A_4-A_7) (least and most significant digits); i.e. 8 bits which supply the address of a bit in the memory. There is an address in memory associated with each of the BCD numbers 2 through 83. Addresses outside the range of 2 to 83 at the LSD and MSD inputs do not cause any modification of the stored bits or change in the output data.

Example: Address 83 = 10000011 (A_7...A_0)
Address 2 = 00000010 (A_7...A_0)

Address changes must occur only during $\overline{CS}$ high and must be stable at least 20μs before $\overline{CS}$ goes low.

Memory Read

The negative transition of $\overline{CS}$ (from a "1" level to a "0" level) initiates a memory read cycle, except when the transition occurs during a memory alteration cycle, in which case the transition is ignored. A read cycle will cause the DATA OUT pin to indicate the state of the memory bit read. The DATA OUT pin will retain the state until either $\overline{CS}$ goes to "1" or a memory alteration cycle is initiated. DATA OUT will show the contents of the address 100μs after $\overline{CS}$ starts falling. When $\overline{CS}$ is high the DATA OUT pin is low. The DATA OUT pin is internally pulled up to the positive supply, V_{SS} and for a "0" output the DATA OUT pin floats with an external pull-down (10KΩ) to ground.

Memory Alteration

A memory alteration cycle is initiated only when the SET DATA "0" or the SET DATA "1" input, but not both, has been continuously at "0" for the specified debounce time. This allows an input to be entered via a contact closure to ground using switches. These inputs are connected to V_{SS} via internal pull-ups. During the alteration cycle the address is held latched within the LSI. Changes in the address and SET DATA inputs are ignored, and the DATA OUT pin is held at "0". Only one memory bit may be erased or written during any single memory alteration cycle. The alteration cycle, once initiated, must go to completion. Upon completion of an alteration cycle or the fall of $\overline{CS}$ whichever occurs last, the memory bit corresponding to the current input address will be read and outputted on the DATA OUT terminal. A memory read of a bit altered due to SET DATA "0" input will cause the DATA OUT pin to be "0". Similarly, a read of a bit altered due to a SET DATA "1" input will cause the DATA OUT pin to be "1". The SET DATA inputs have internal circuits to provide delays for interfacing to mechanical switches or relays. Each successful debounce of a SET DATA input will initiate only one memory alteration cycle. Another alteration cycle will not occur until both

EAROM

SET DATA inputs have remained continuously at a "1" level for the specified release time and only one of the SET DATA inputs has again been successfully debounced. After an alteration cycle is complete, a read cycle may not be initiated by CS until 3 cycles of the clock on the "Timing" input pin have occurred (about 12.5ms for a nominal 200Hz frequency).

Timing

This is an input provided for external components used for a timing reference. A resistor (680K) and a capacitor (.01μF) may be connected to this input to provide a 200Hz nominal clock frequency. A lower capacitor or resistor value will provide a higher frequency. The timer will run only during a read cycle, alteration cycles, or while timing a debounce or release. Increasing the clock frequency will shorten these times. The frequency can vary from 50Hz min to 500Hz max. and may be measured on the timing pin.

PIN FUNCTIONS

NAME	FUNCTIONS
A_0-A_7	Address bus used to select 1 of 82 addresses.
$\overline{CS}$	Chip select. An active low signal which enables or disables the data out pin.
Data Out	DATA OUT is a single bit indicating the state of the addressed memory cell.
Set Data 0 Set Data 1	These are inputs by which the user can modify the memory contents.
TI	Provides a timing reference for internal timing cycles.
TEST	A TEST pin which provides a connection to V_m, an internal voltage used for evaluating chip memory performance. In normal operation this pin should be left unconnected.
V_{SS}	Substrate Supply. Nominally +5V.
V_{NEG}	Power supply input. Nominally −30V.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
(except V_{NEG}) with respect to V_{SS} ..... −20V to +0.3V
V_{NEG} with respect to V_{SS} ..... −40V
Storage temperature (No Data Retention) ..... −65°C to +150°C
Storage temperature (with Data Retention)
Operating ..... 0°C to +70°C
Unpowered ..... −40°C to +85°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

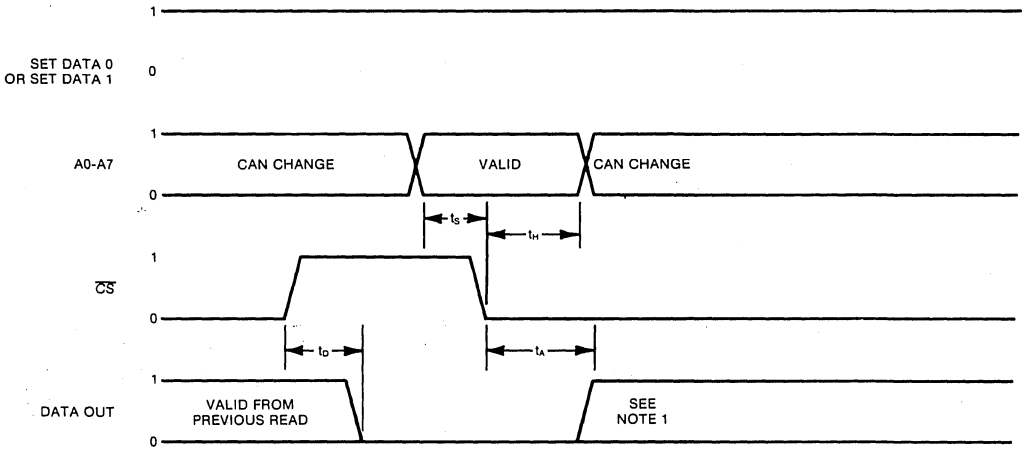
Standard Conditions (unless otherwise noted)

V_{SS} = +4.5V to +8.0V
$V_{SS} - V_{NEG}$ = −32V to −38V
Operating Temperature T_A = 0°C to 70°C

Characteristic	Sym	Min	Max	Units	Conditions
DC CHARACTERISTICS					
Input Logic "1"	V_{IH}	V_{SS} −2.0	V_{SS} +.3	V	
Input Logic "0"	V_{IL}	V_{SS} −10	V_{SS} −4.1	V	
Input Leakage	I_L	—	10	μA	
Output Logic "1"	V_{OH}	—	V_{SS} −.5	V	@ 0.5mA
Power Supply	I_{SS}	4	20	mA	
Power Dissipation	P_{SS}	130	700	mW	
AC CHARACTERISTICS					
Read Cycle Time	—	130	—	μs	
Read Access Time	t_A	—	100	μs	from fall of $\overline{CS}$
Memory Alteration Time	—	200	—	ms	
Time between Memory Alteration Cycles	t_C	12.5	—	ms	
Debounce Time for Changing Memory	t_B	12.5	37.5	ms	
Address Setup Time	t_S	20	—	μs	
Address Hold Time	t_H	100	—	μs	
Reset Time	t_D	2	30	μs	from rise of $\overline{CS}$
Input Rise & Fall Times	—	.03	30	ms	on all inputs
EAROM CHARACTERISTICS					
Data Retention, Power Off (Storage)	—	10	—	Years	−40°C to +85°C
Data Retention, Power On	—	10	—	Years	0°C to +70°C
Read Cycles Per Cell	—	10^7	—	—	no loss of data
Erase/Write Cycles per Cell	—	10^9	—	cycles	10 year retention
Erase/Write Cycles per Cell	—	10^4	—	cycles	1 year retention

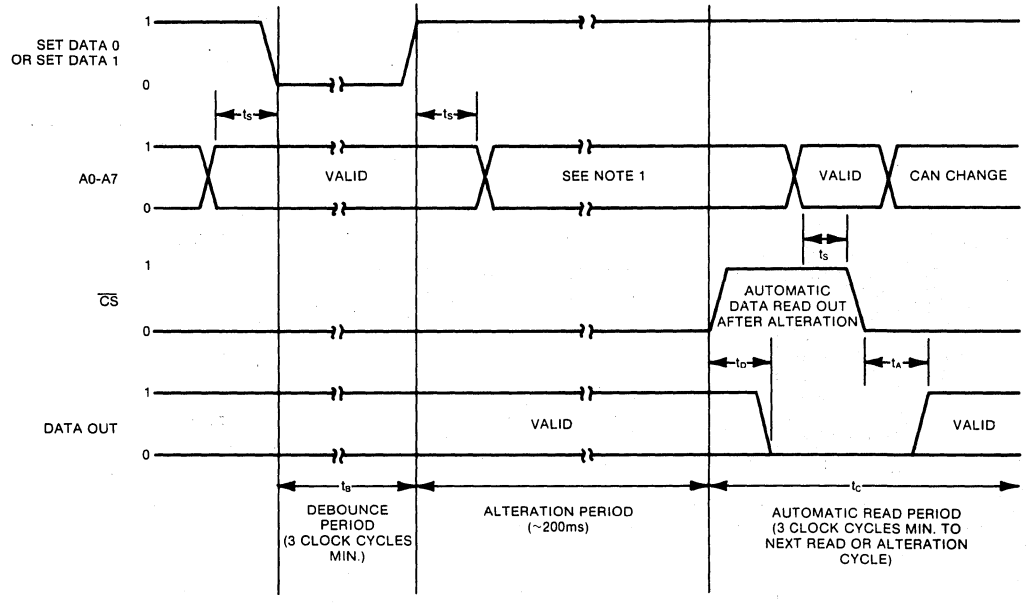
TIMING DIAGRAMS

READ OPERATION



NOTE 1: Data will be valid until the next positive $\overline{CS}$ transition or until initiation of an alteration cycle.

DATA ALTERATION



NOTE 1: Address may change here, but should not change if verification of correct alteration is required.

1400 Bit Serial Electrically Alterable Read Only Memory

FEATURES

- 100 word x 14 bit organization
- Addressing by two consecutive one-of-ten codes
- Single −35 Volt supply
- Word alterable
- 10 year data storage
- MOS compatible signal levels
- Write/erase time: 10ms

DESCRIPTION

The ER1400 is a serial input/output 1400 bit electrically erasable and reprogrammable ROM, organized as 100 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus.

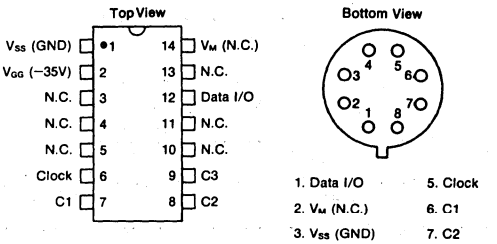
Mode selection is by a 3 bit code applied to C1, C2 and C3.

Before writing, a selected location must be preconditioned by an Erase operation. Data is then stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 1400 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

PIN CONFIGURATIONS

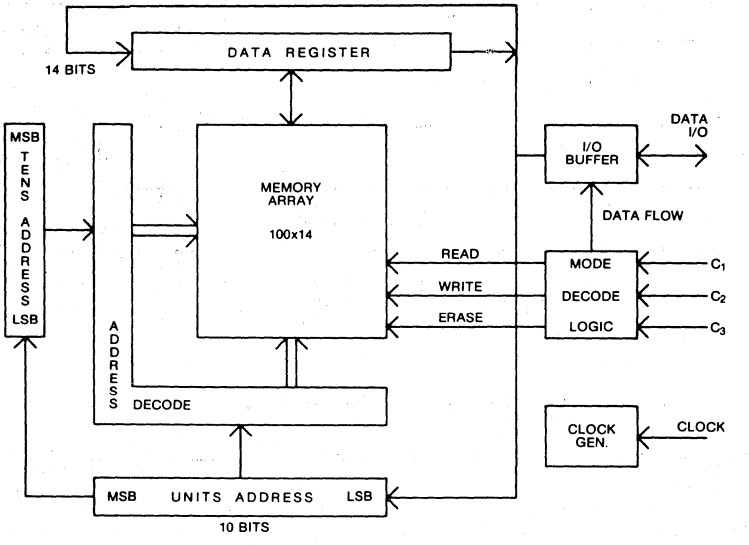
Standard package
14 LEAD DUAL IN LINE

Special Order Package
8 LEAD TO-8 (ER1400T)



N.C.= No external connection
for normal usage

BLOCK DIAGRAM



PIN FUNCTIONS

Name	Function
Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respecitvely. When outputting data is has MOS drive capability, while in all other modes it is left floating.
V_M	Used for testing purposes only. Must be left unconnected for normal operation.
V_{SS}	Chip substrate. Normally connected to ground.
V_{GG}	DC supply. Normally connected to V_{SS} −35 Volt supply.
Clock	Timing reference. Required for all operations. May be left at logic zero when device is in standby.
C1,C2,C3	Mode control pins. Their operation is as follows:

C1	C2	C3	Function
0	0	0	Standby—the output buffer is left floating. If the clock is maintained, the contents of the Address and Data Registers will remain unchanged.
0	1	1	Accept Address—Data presented at the I/O pin is shifted into the Address Register with each clock pulse. Addressing is by two consecutive one-of-ten codes.
1	0	0	Read—The address word is read from memory into the data register.
1	0	1	Shift Data Out—The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.
0	1	0	Erase—The word stored at the addessed location is erased to all ones.
1	1	1	Accept Data—The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.
1	1	0	Write—The word contained in the Data Register is written into the location designated by the Address Register.
0	0	1	Not Used

EAROM

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
(except V_{GG}) with respect to V_{SS} ..... −20V to +0.3V
V_{GG} with respect to V_{SS} ..... −40V
Storage temperature (No Data Retention) ..... −65°C to +150°C
Storage temperature (with Data Retention)
Operating ..... −25°C to +75°C
Unpowered ..... −65°C to +80°C

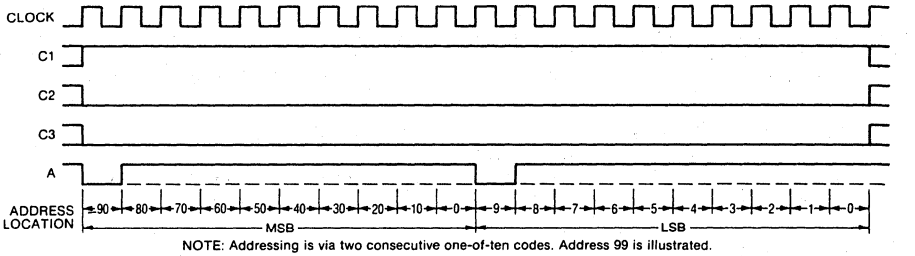
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)
V_{SS} = GND
V_{GG} = −35V ± 8%
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input logic "1"	V_{IL}	V_{SS}−15.0	—	V_{SS}−8.0	Volts	
Input logic "0"	V_{IH}	V_{SS}−1.0	—	V_{SS}+0.3	Volts	
Input leakage	I_L	—	—	10	μA	V_{IN} = −15V
Output logic "1"	V_{OL}	—	—	V_{SS}−12.0	Volts	Load = 1.5 Meg, 100pF
Output logic "0"	V_{OH}	V_{SS}−1.0	—	V_{SS}+0.3	Volts	I_{SOURCE} = 200μA
Power consumption	P_{GG}	—	—	300	mW	
Power supply current	I_{GG}	—	—	8.0	mA	
AC CHARACTERISTICS						
Clock Frequency	fϕ	10.0	14.0	17.0	kHz	
Clock duty cycle	Dϕ	35	50	65	%	
Write time	tw	10.0	15.0	24.0	ms	
Erase time	te	10.0	15.0	24.0	ms	
Rise, fall time	tr, tf	—	—	1.0	μs	
Control, Data set up time	t_{CS}	1	—	—	μs	
Control, Data hold time	t_{CH}	0	—	—	μs	
Propagation delay	tpw	—	—	20.0	μs	Load − 1 Meg. 100pF
Non-volatile data storage	T_S	10	—	—	Years	See Note 1.
Number of erase/write cycles	N_W	—	—	10^4	—	Per word. See Note 2.
Number of read accesses between writes	N_{RA}	10^9	—	—	—	Per word

** Typical values are at +25°C and nominal voltages.
NOTE 1: T_S is for powered or unpowered storage.
NOTE 2: N_W (=10^4) is a maximum for data retention times greater than 10 years. Beyond 10^4 reprograming cycles, there is a gradual, logarithmic reduction in retention time with 1 year being a typical value after 10^5 cycles.

TIMING DIAGRAMS



NOTE: Addressing is via two consecutive one-of-ten codes. Address 99 is illustrated.

Fig.1 ACCEPT ADDRESS

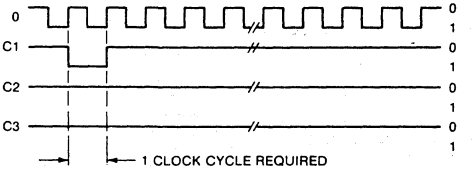
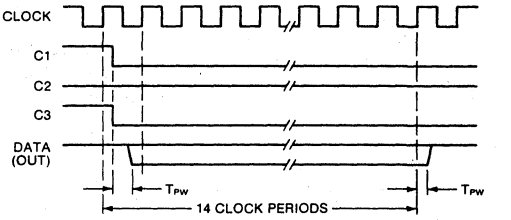


Fig.2 READ



TPW measured initially from control line transition to data out, then measured from the positive clock edges to data changes. Timing measurements are made at VSS −2 and −10 volt points.

Fig.3 SHIFT DATA OUT

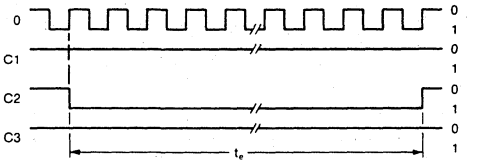


Fig.4 ERASE

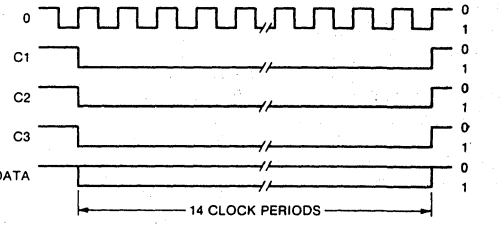


Fig.5 ACCEPT DATA

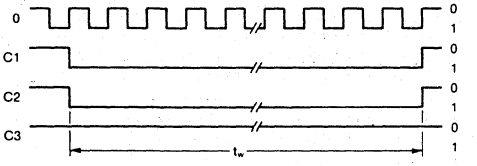


Fig.6 WRITE

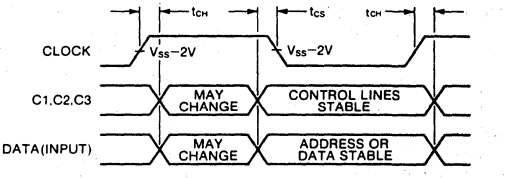


Fig.7 INPUT TIMING

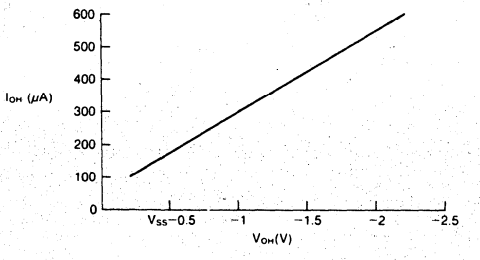


Fig.8 TYPICAL OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

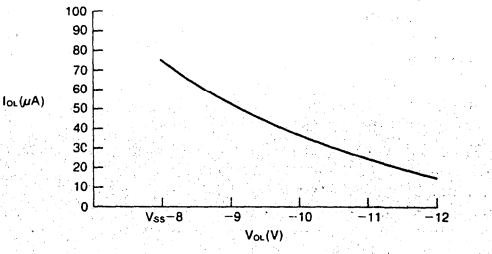


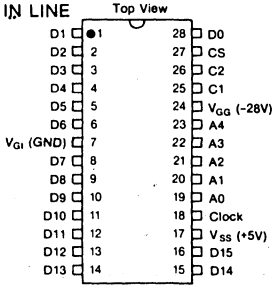
Fig.9 TYPICAL OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

512 Bit Electrically Alterable Read Only Memory

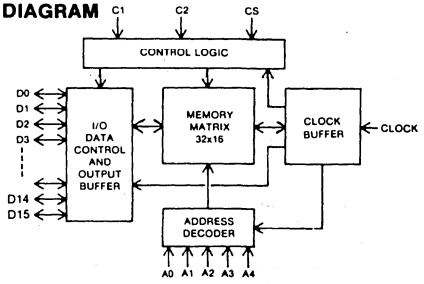
- 32 word x 16 bit organization
- 5 bit binary addressing
- +5, −28 V power supplies
- Word Alterable
- 10 year data storage for ER2051 (at +70°C)
- 1 year data storage for ER2051 IR (at +85°C) and ER2051 HR (at +125°C)
- TTL compatibility with pull-up resistors on inputs
- Tri-state outputs
- Read Time: 1μs (ER2051), 2μs (ER2051 IR and ER2051 HR)
- Write/Erase Time: 50ms (ER2051), 100ms (ER2051 HR)
- No Voltage switching required
- Chip select
- Two extended temperature ranges:
  −40°C to +85°C (Industrial) Part # ER2051 IR
  −55°C to +125°C (Hi-Rel) Part # ER2051 HR

PIN CONFIGURATION

28 LEAD DUAL IN LINE — Top View



BLOCK DIAGRAM



DESCRIPTION

The ER2051, ER2051 IR and ER2051 HR are fully decoded 32 x 16 electrically erasable and reprogrammable ROMs. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

The EAROM may be operated with the V_{SS} power supply between +5V and +10Volts, as long as the V_{SS}—V_{GG} always equals 33 Volts. Thus, V_{SS} can be +5Volts for TTL compatibility or up to +10Volts for CMOS compatibility, if V_{GG} is appropriately adjusted.

The ER2051 IR and ER2051 HR are screened to Mil Std. 883B/ method 5004.1/level B, pre-cap visual inspection, environmental testing, burn-in and external visual. They are available in 28 lead ceramic dual in line packages.

OPERATION

Data is stored in a two transistor memory cell. After the cell is preconditioned by an erase signal (which causes a positive shift in the threshold of both transistors), data is written into one of the transistors making its threshold more negative. A sensing flip flop is used to read the memory cell and presents a logic high or low to the output depending on which transistor is "written."

It is important to note two things: first, that an erase is required before a wire to precondition the cell, and second, that after an erase, both transistors will have the same threshold voltage and valid data will not be present at the output.

The ER2051, ER2051 IR and ER2051 HR EAROMs use dynamic, edge triggered circuits internally. This requires either a mode change, a clock or a transition of the chip select between successive operations. Thus successive operations in the same mode must be separated by transitions of one of these four lines. Clock pulses are not normally required during erase or write operations, but are needed for successive operations if the chip select is held high, i.e., applications where one EAROM is used.

In using the read clock to refresh the outputs during a read operation, a minimal frequency is recommended to insure that the read cycle lifetime between writes (NR_A) is kept to a maximum.

PIN FUNCTIONS

A_0-A_4	5-Bit Word Address
D_0-D_{15}	Data input and output pins
CS	Chip Select. Chip selected at logic "1". When chip select is at logic "0", outputs are open circuit, read, write and erase are disabled. Power is reduced.
C1, C2	Mode Control Inputs C1 C2 0 1 Erase Mode: stored data is erased at addressed location. 1 0 Read Mode: addressed data read after clock pulse. Output data retained at output pins until next read operation. 0 0 Write Mode: input data written at addressed location. Clock not required.
CLK	Clock Input. Pulse to logic "1" for read operation. Data will remain valid for 20 to 60 seconds; the outputs will then become open circuit until another clock pulse is received.
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input.
V_{GG}	Power Supply Input. Normally at -28 volts.

EAROM

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to V_{SS}) ..... -35V to +0.3V
Storage temperature ..... -65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—ranges are specified below.

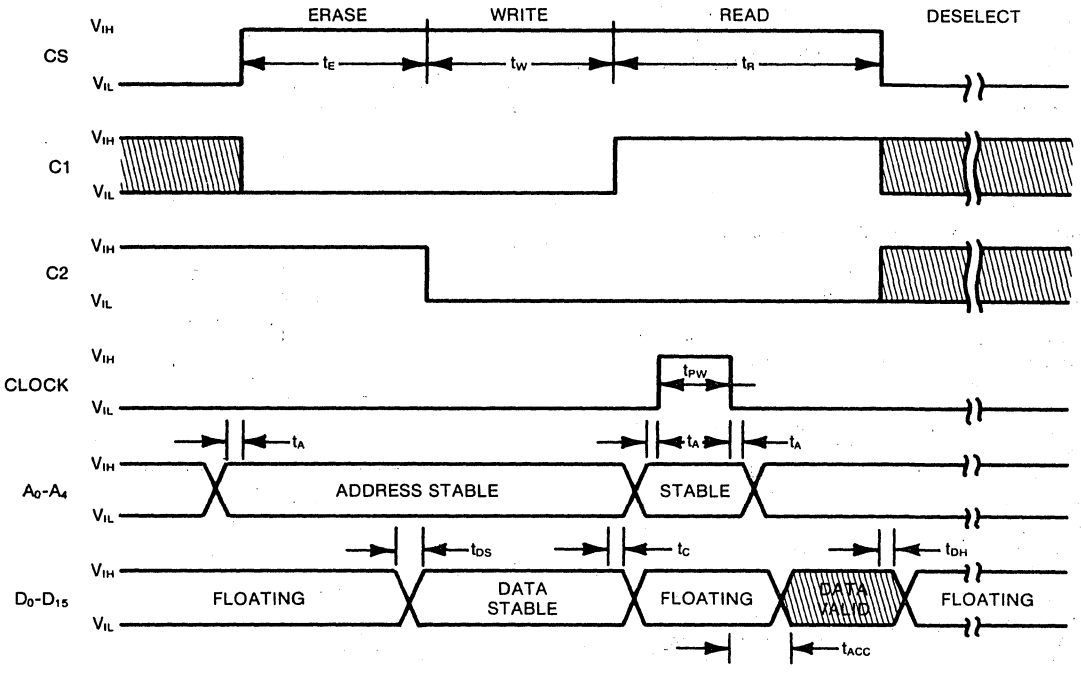
Standard Conditions (for TTL compatibility)

V_{SS} = +5V ±5%
V_{GG} = -28V ±5%
V_{GI} = GND
Operating Temperature T_A = 0°C to +70°C for ER2051
T_A = −40°C to +85°C for ER2051 IR
T_A = −55°C to +125°C for ER2051 HR
Output Load = 100pF, 1 TTL load

		ER2051			ER2051 IR/ER2051 HR				
Characteristics	**Sym**	**Min.**	**Typ.****	**Max.**	**Min.**	**Typ.****	**Max.**	**Units**	**Conditions**
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	V_{SS} −1.5	—	V_{SS} +0.3	V_{SS} −1.5	—	V_{SS} +0.3	V	
Input Logic "0"	V_{IL}	V_{SS} −15	—	0.8	V_{SS} −10	—	0.6	V	
Output Logic "1"	V_{OH}	V_{SS} −1.5	—	—	V_{SS} −1.5	—	—	V	I_{OH} = 100μA
Output Logic "0"	V_{OL}	—	—	0.6	—	—	0.6	V	I_{OL} = 1.6mA for V_{SS} = 5V
Input Leakage	I_L	—	2	10	—	2	10	μA	V_{IN} = V_{SS} −15
Output Leakage	I_O	—	2	10	—	2	10	μA	Chip deselected
Power Supply Current									
Read	I_{GG}	—	—	14	—	—	18	mA	I_{GG} returned through V_{SS}
Write	I_{GG}	—	—	11	—	—	15	mA	
Erase	I_{GG}	—	—	11	—	—	15	mA	
Deselected	I_{GG}	—	—	9	—	—	12	mA	
AC CHARACTERISTICS									
Access Time	t_{ACC}	—	—	1.0	—	—	2.0	μs	
Clock Pulse width	t_{PW}	2.0	—	20.0	2.0	—	20.0	μs	
Erase Cycle Time	t_E	50	—	200.0	100	—	200.0	ms	
Write Cycle Time	t_W	50	—	200.0	100	—	200.0	ms	
Read Cycle Time	t_R	3.5	—	24.0	4.5	—	25	μs	
Address to Clock Time	t_A	50	—	—	50	—	—	ns	
Data Set Up Time	t_{DS}	50	—	—	50	—	—	ns	
Data Hold Time	t_{DH}	50	—	—	50	—	—	ns	
Control to Address & Data Change	t_C	0	—	—	0	—	—	ns	
Number of Reads/Word Refresh	N_{RA}	10^{11}	—	—	10^{11}	—	—		
Number of Erase/Write Cycles	N_W	10^6	—	—	10^5	—	—	—	
Input Capacitance, all pins	C_{IO}	—	8	15	—	8	15	pF	
Unpowered Data Storage Time	t_S	10	—	—	1	—	—	Years	at max. temperature
Power Dissipation Read Cycle	P_D	—	450	500	—	450	500	mW	at 25°C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	500	mW	at 125°C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	600	mW	at −55°C V_{SS} = +5, V_{GG} = −29
Pulse Rise, fall time	t_r, t_f	10	—	100	10	—	100	ns	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



512 Bit Electrically Alterable Read Only Memory

FEATURES

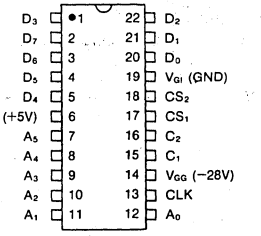
- 64 word x 8 bit organization
- 6 bit binary addressing
- +5, −28V power supplies
- Word Alterable
- 10 year data storage for ER2055 (at +70°C)
- 1 year data storage for ER2055 IR (at +85°C) and ER2055 HR (at +125°C)
- TTL compatible with pull-up resistors on inputs
- Tri-state outputs
- Read Time: 2μs (ER2055), 4μs (ER2055 IR and ER2055 HR)
- Write/Erase Time: 50ms (ER2055), 100ms (ER2055 HR)
- No voltage switching required
- 2 chip selects
- Two extended temperature ranges:
  −40°C to +85°C (Industrial) Part # ER2055 IR
  −55°C to +125°C (Hi-Rel) Part # ER2055 HR

EAROM

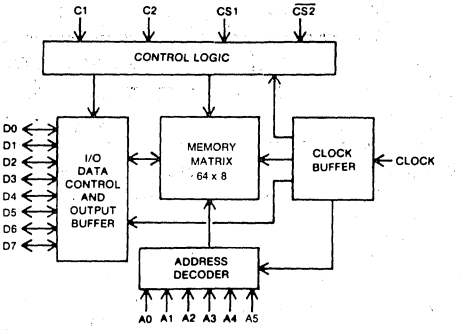
PIN CONFIGURATION

22 LEAD DUAL IN LINE

Top View



BLOCK DIAGRAM



DESCRIPTION

The ER2055 is a fully decoded 64 x 8 electrically erasable and reprogrammable ROM. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

OPERATION

Data is stored in a two transistor memory cell. After the cell is preconditioned by an erase signal (which causes a positive shift in the threshold of both transistors), data is written into one of the transistors making its threshold more negative. A sensing flip flop is used to read the memory cell and presents a logic high or low to the output depending on which transistor is "written".

The ER2055 EAROM may be operated with V_{SS} between +5 and +10 volts for either TTL or CMOS compatibility. The negative power supply, V_{GG}, should be adjusted so that the difference between V_{SS} and V_{GG} is always 33 volts.

It is important to note two things: first, that an erase is required before a write to precondition the cell, and second, that after an erase, both transistors will have the same threshold voltage and valid data will not be present at the output.

The ER2055 EAROM uses dynamic edge triggered circuits internally. This requires either a mode change, a clock or a transition of the chip selects between successive operations. Thus successive operations in the same mode must be separated by transition of one of these four lines. Clock pulses are not normally required during erase or write operations, but are needed for successive operations if the chip select is held high, i.e., applications where one EAROM is used.

In using the read clock to refresh the outputs during a read operation a minimal frequency is recommended to insure that the read cycle lifetime between writes (N_{RA}) is kept to a maximum.

The ER2055 IR and ER2055 HR are screened to Mil Std. 883B/method 5004.1/level B, pre-cap visual inspection, environmental testing, burn-in and external visual. They are available in 28 lead ceramic dual in line packages.

PIN FUNCTIONS

A_0-A_5	6-Bit Word Address
D_0-D_7	Data input and output pins
CS1, $\overline{CS2}$	Chip Selects Chip selected at logic "1" on CS1 and logic "0" on $\overline{CS2}$. When chip is not selected, outputs are open circuit, read, write and erase are disabled. Power is reduced.
C1, C2	Mode Control Inputs C1 C2 0 1 Erase Mode: stored data is erased at addressed location. 1 0 Read Mode: addressed data read after clock pulse. Output data retained at output pins until next read operation. 0 0 Write Mode: input data written at addressed location. Clock not required.
CLK	Clock Input. Pulse to logic "1" for read operation. Data will remain valid for 20 to 60 seconds; the outputs will then become open circuit until another clock pulse is received.
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input.
V_{GG}	Power Supply Input. Normally at -28 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to Vss) ..... -35V to +0.3V
Storage temperature ..... -65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (for TTL Compatibility)

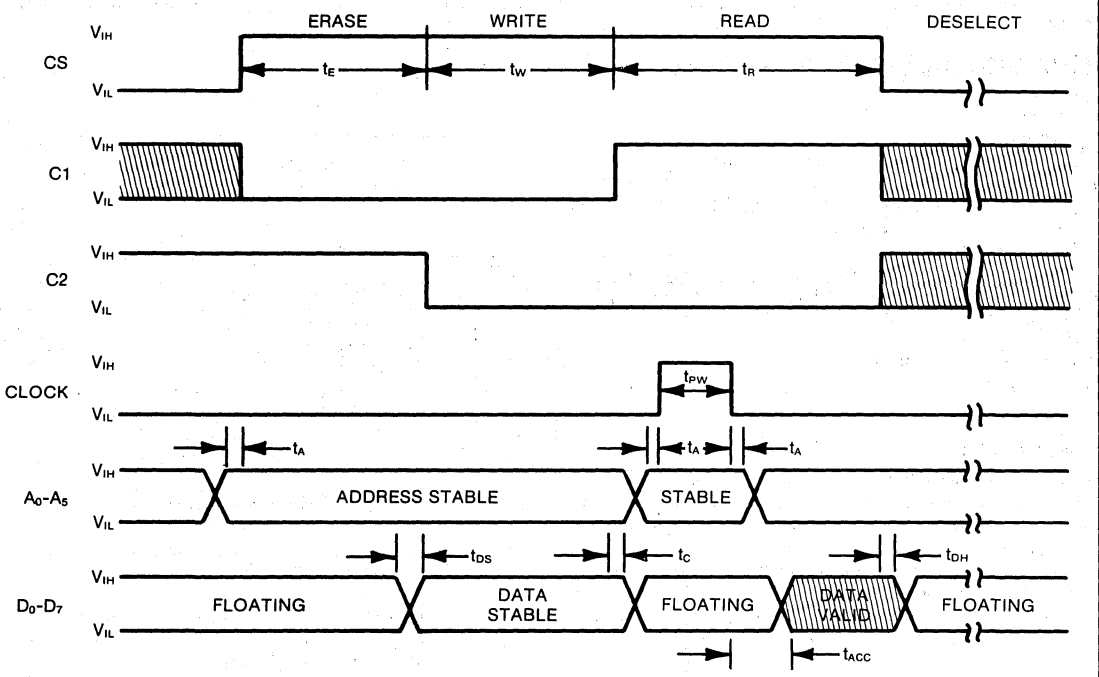
V_{SS} = +5V±5%
V_{GG} = -28V±5%
V_{GI} = GND
Operating Temperature T_A = 0°C to +70°C for ER2055
T_A = −40°C to +85°C for ER2055 IR
T_A = −55°C to +125°C for ER2055 HR
Output Load = 100pF, 1 TTL load

		ER2055			ER2055 IR/ER2055 HR				
Characteristics	**Sym**	**Min.**	**Typ.****	**Max.**	**Min.**	**Typ.****	**Max.**	**Units**	**Conditions**
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	V_{SS} −1.5	—	V_{SS} +0.3	V_{SS} −1.5	—	V_{SS} +0.3	V	
Input Logic "0"	V_{IL}	V_{SS} −15	—	0.8	V_{SS} −10	—	0.6	V	
Output Logic "1"	V_{OH}	V_{SS} −1.5	—	—	V_{SS} −1.5	—	—	V	I_{OH} = 100μA
Output Logic "0"	V_{OL}	—	—	0.6	—	—	0.6	V	I_{OL} = 1.6mA for V_{SS} = 5V
Input Leakage	I_L	—	2	10	—	2	10	μA	V_{IN} = V_{SS} −15
Output Leakage	I_O	—	2	10	—	2	10	μA	Chip deselected
Power Supply Current									
Read	I_{GG}	—	8	10	—	8	13	mA	I_{SS} approx. I_{GG}
Write	I_{GG}	—	6	7	—	6	9	mA	I_{SS} approx. I_{GG}
Erase	I_{GG}	—	4	6	—	4	8	mA	I_{SS} approx. I_{GG}
Deselected	I_{GG}	—	3	4	—	3	6	mA	I_{SS} approx. I_{GG}
AC CHARACTERISTICS									
Access Time	t_{ACC}	—	—	2.0	—	—	4.0	μs	
Clock Pulse width	t_{PW}	2.0	—	20.0	2.0	—	20.0	μs	
Erase Cycle Time	t_E	50	—	200.0	100	—	200.0	ms	
Write Cycle Time	t_W	50	—	200.0	100	—	200.0	ms	
Read Cycle Time	t_R	5.0	—	24.0	6.0	—	25.0	μs	
Address to Clock Time	t_A	50	—	—	50	—	—	ns	
Data Set Up Time	t_{DS}	50	—	—	50	—	—	ns	
Data Hold Time	t_{DH}	50	—	—	50	—	—	ns	
Control to Address & Data Change	t_C	0	—	—	0	—	—	ns	
Number of Reads/Word Refresh	N_{RA}	10^{11}	—	—	10^{11}	—	—		
Number of Erase/Write Cycles	N_W	10^6	—	—	10^5	—	—	—	
Input Capacitance, all pins	C_{IO}	—	6	10	—	6	10	pF	
Unpowered Data Storage Time	t_S	10	—	—	1	—	—	Years	at max. temperature
Power Dissipation Read Cycle	P_D	—	450	500	—	450	500	mW	at 25°C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	500	mW	at 125°C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	600	mW	at −55°C V_{SS} = +5, V_{GG} = −29
Pulse Rise, fall time	t_{R1} t_F	10	—	100	10	—	100	ns	

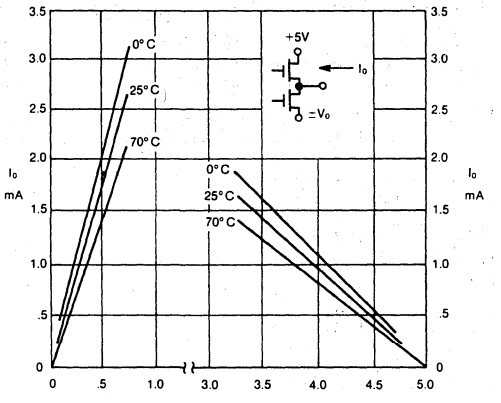
**Typical values are at +25°C and nominal voltages.

EAROM

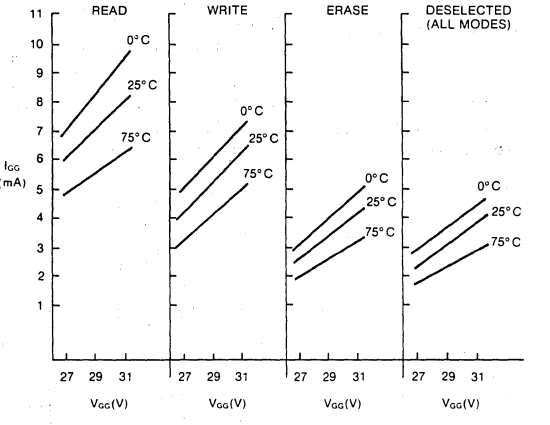
TIMING DIAGRAM



TYPICAL OUTPUT CHARACTERISTICS



TYPICAL SUPPLY CURRENT VS POWER SUPPLY VOLTAGE



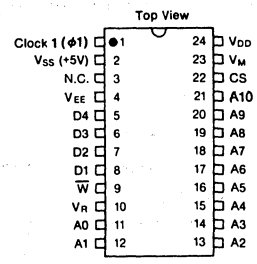
8192 Bit Electrically Alterable Read Only Memory

FEATURES

- 2048 word x 4 bit organization
- 11 bit binary addressing
- ±5, −14, −24V power supplies
- Block erasable
- 1 year unpowered data storage
- TTL compatible with pull up resistors on inputs
- Tri-state outputs
- Read time: 1.6μs
- Write time: 10ms, erase time: 100ms
- Chip select

PIN CONFIGURATION

24 LEAD DUAL IN LINE



DESCRIPTION

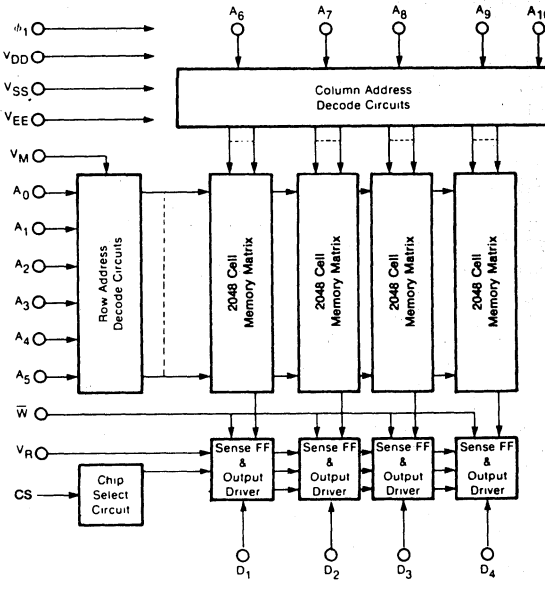
The ER2810 IR and ER2810 HR are fully decoded 2048 x 4-bit electrically erasable and reprogrammable ROMs utilizing second-generation MNOS epitaxial processing technology.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 8192 MNOS memory transistors. When the writing voltage is removed, the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

The ER2810 IR and ER2810 HR are screened to Mil Std. 883B/ method 5004.1/level B, pre-cap visual inspection, environmental testing, burn-in and external visual. They are available in 24 lead ceramic dual in line packages.

Stored data may be accessed a minimum of 2×10^{10} times without refresh and is non-volatile in the unpowered state in excess of one year. Data is erased by applying a V_{SS} −28V pulse to the erase substrate of the device. Data may be reprogrammed, without degradation of the retention time, up to 10^5 times, beyond which a gradual, logarithmic fall off is seen. All outputs are at logic high when the device is in the erased state.

BLOCK DIAGRAM



EAROM

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs or outputs relative to V_{SS} . . . . . +0.3V to -30V
Storage temperature . . . . . -65°C to +150°C
Soldering temperature of leads (10 seconds) . . . . . +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

RECOMMENDED OPERATING CONDITIONS

T_A = −40°C to +85°C for ER2810 IR
T_A = −55°C to +125°C for ER2810 HR

Symbol	Parameter	Erase Mode			Write Mode			Read Mode			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{DD}	Supply Voltage	4.75	V_{SS}	V_{SS}+0.3	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{SS}	Substrate supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_M	Memory voltage	—	V_{SS}	—	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-10.5	V_{SS}-10	V_{SS}-9.5	V
V_R	Reference voltage	—	V_{SS}	—	—	V_{SS}	—	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{EEH}	Erase substrate input high	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V
V_{EEL}	Erase substrate input low	V_{SS}-29	V_{SS}-28	V_{SS}-27	Not Applicable			Not Applicable			V
V_{WH}	Write control input high	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{WL}	Write control input low	V_{SS}-29	—	V_{SS}-4.4	V_{SS}-29	—	V_{SS}-4.4	Not Applicable			V
$V\phi_H$	ϕ_1 input high voltage	—	V_{SS}	—	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V
$V\phi_L$	ϕ_1 input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{IH}	Address and CS input high	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{IL}	Address and CS input low	Don't Care			V_{DD}	—	V_{SS}-4.4	V_{DD}	—	V_{SS}-4.4	V
V_{DH}	Data input high voltage	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	Not Applicable			V
V_{DL}	Data input low voltage	Don't Care			V_{DD}	—	V_{SS}-4.4	Not Applicable			V

STATIC ELECTRICAL CHARACTERISTICS

T_A = −40°C to +85°C for ER2810 IR
T_A = −55°C to +125°C for ER2810 HR
(NO EXTERNAL LOADS EXCEPT AS NOTED)

Symbol	Parameter	Conditions All Pins at V_{SS} Unless Noted	Min	Typ	Max	Unit
I_{IN}	Input leakage current (except pins 1, 2, 4, 5, 6, 7, 8, and 24) at V_{SS}-15V	$\phi1$=V_{DD}=V_{SS}-20	—	—	-2.0	μA
$I\phi_1$	ϕ_1 leakage current at V_{SS}-29V	V_{DD}=V_{SS}-29, $\overline{W}$=V_{SS}-25	—	—	-200	μA
I_O	Output leakage current at V_{SS}-15V	Chip deselected	—	—	-10.0	μA
I_{EEL}	Erase leakage current at V_{SS}-28V	$\overline{W}$=V_{SS}-25	—	—	-200	μA
I_{DD1}	V_{DD} supply current - read mode at V_{SS}-19V	Outputs open (See Figure 6)	—	16	20	mA
I_{DD2}	V_{DD} supply current - Write mode at V_{SS}-28V	Outputs open (See Figure 5)	—	30	40	mA
V_{OH}	Data output high voltage - TTL load	One Series 7400 TTL load with R_S = 1K, V_{CC} = V_{SS}	V_{SS} −1.5	—	—	V
V_{OL}	Data output low voltage - TTL load	(See TTL Notes)	—	—	V_{SS} −10	V
V_{OH}	Data Output high voltage - MOS		V_{SS}-1.5	—	—	V
V_{OL}	Data Output low voltage — MOS	C_L = 100pF	—	—	V_{SS} −14	V
T_S	Unpowered nonvolatile data storage	Typical write conditions	1	—	—	Years

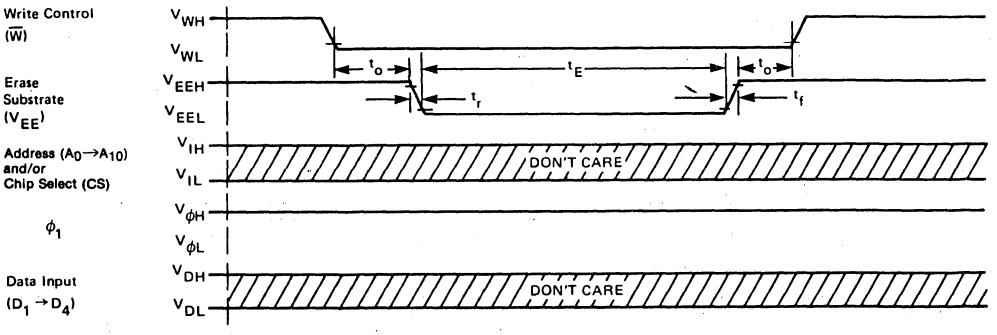
CAPACITANCE AT V_{IN} = V_{SS}, ALL OTHER PINS GROUNDED (V_{SS}), f = 1MHz

Symbol	Parameter	Min	Typ	Max	Unit
C_I	Address and chip select input capacitance	—	5	7	pF
C_W	Write control input capacitance	—	10	20	pF
C_{ST}	Strobe input capacitance	—	10	15	pF
$C\phi_1$	ϕ_1 Input Capacitance	—	40	50	pF
C_{EE}	Erase substrate capacitance	—	600	700	pF
C_D	Data input/output capacitance	—	6	10	pF

ERASE CYCLE CHARACTERISTICS

$T_A = -40°C$ to $+85°C$ for ER2810 IR
$T_A = -55°C$ to $+125°C$ for ER2810 HR

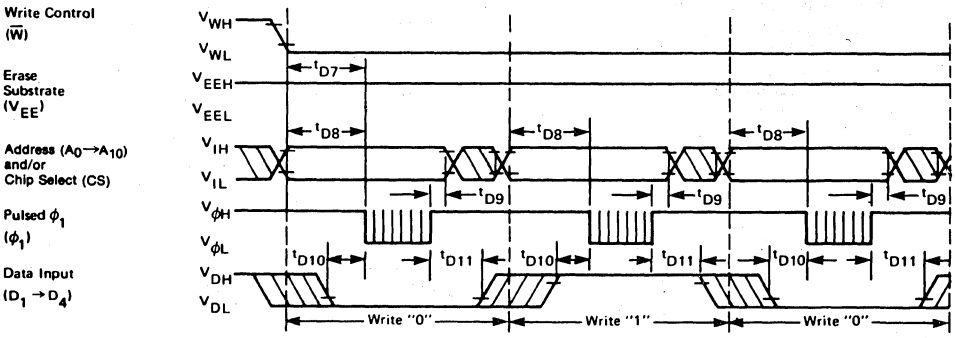
Symbol	Parameter	Min	Typ	Max	Units
t_E	V_{EE} erase pulse width	100	—	1000	ms
t_R, t_F	V_{EE} rise time, V_{EE} fall time	0.01	—	1.0	ms
t_O	Write-erase overlap	10	—	—	μs



WRITE CYCLE CHARACTERISTICS

$T_A = -40°C$ to $+85°C$ for ER2810 IR
$T_A = -55°C$ to $+125°C$ for ER2810 HR (See Note 3)

Symbol	Parameter	Min	Typ	Max	Units
$N\phi_W$	Number of ϕ_1 write pulses at 100 μs ±10%, 5 μs min. dead time between pulses)	100	200	300	Pulses
t_{D7}	Write control rise to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D8}	Address change and chip select fall to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D9}	Pulsed ϕ_1 fall to address and chip select change delay	0.0	—	—	μs
t_{D10}	Data input change to pulsed ϕ_1 rise delay	0.0	—	—	μs
t_{D11}	Pulsed ϕ_1 fall to data input change delay	0.0	—	—	μs
N_W	Number of times word may be rewritten	—	—	10^5	—

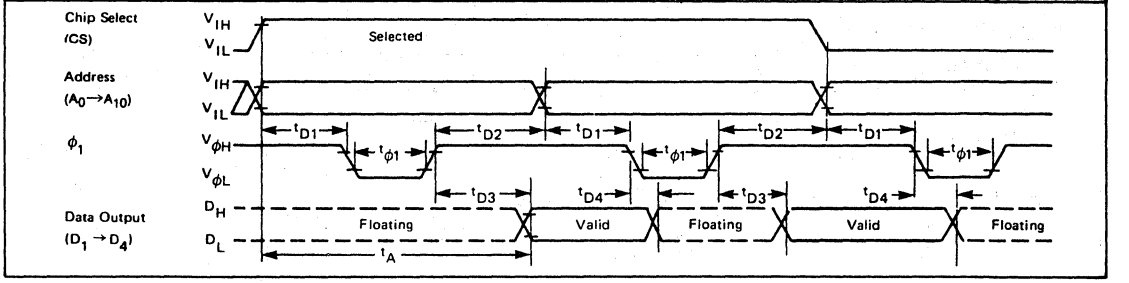


NOTES:

1. Due to the dynamic nature of the circuit a "ϕ_1 NOT" time in excess of 40 μsec may result in a floated output condition. Consequently data must be resampled with a 40 μsec time period following the fall of ϕ_1 to ensure its validity.
2. Several seconds may be required following a programming operation for the circuit to become operable in the read mode. If data is to be verified immediately following programming, a forward current of +1mA ± 10% may be forced into the erase substrate junction (Pin 4, V_{EE}), for a period not to exceed 10 milliseconds, to quickly dissipate charge trapped at internal circuit nodes.
3. Maximum power dissipation occurs during programming. When programming multichip systems where the application of programming voltages is required for several minutes, forced air cooling is recommended to reduce package temperature. Power is not reduced when chip is deselected.
4. All typical values are at +25°C and nominal voltages.
5. ϕ pulses are required after the fall of the chip select line to force the data outputs into a high impedance state.

READ CYCLE CHARACTERISTICS $T_A = -40°C$ to $+85°C$ for ER2810 IR
$T_A = -55°C$ to $+125°C$ for ER2810 HR

Symbol	Parameter (See Figures 1 through 4)	Min	Typ	Max	Units	
T_A	Access time	—	1.6	2.0	μs	
$t_{\phi 1}$	Pulse width (rise and fall times ⩽50ns) (See Note 1)	800	—	5000	ns	
t_{D1}	Address and chip select change to ϕ_1 fall delay	400	—	—	ns	
t_{D2}	ϕ_1 Rise to address and chip select change delay	50	—	—	ns	See Note 1
t_{D3}	ϕ_1 Rise to data output valid delay (See Notes 1 and 2)	—	—	750	ns	See Note 1
t_{D4}	ϕ_1 Fall to floated output delay	—	—	300	ns	
N_{RA}	Number of read accesses/word between refresh	2×10^{10}	—	—	—	



EAROM

PIN FUNCTIONS

Chip Select (CS)
Must be in the high state to enable the data output terminals or to write data into the device.

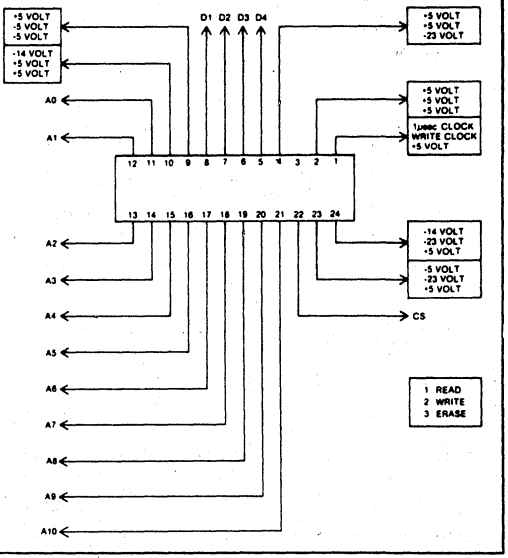
Data Input/Output (D1-D4)
D1 through D4 are bidirectional data terminals. Data are entered on these terminals during the write cycle and read out during the read cycle. When deselected, these terminals are in a floating condition.

Write Control ($\overline{W}$)
The write control terminal must be in the low state in order to write data into the device.

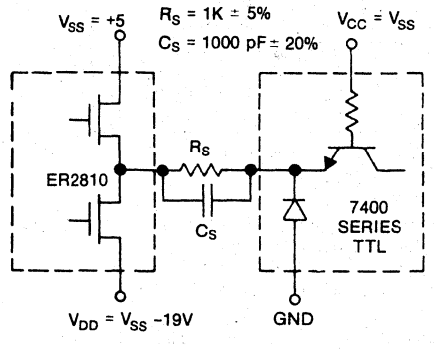
Phase One ($\phi 1$)
During the write and read operations, pulses must be applied to the $\phi 1$ terminal to fully shift the memory transistor threshold voltage to its most negative state. This is required for voltage bootstrapping in the row-selection circuitry. The $\phi 1$ input is high level and not TTL-compatible.

NOTE: All control, address and data inputs are TTL-compatible with pull-up resistors.

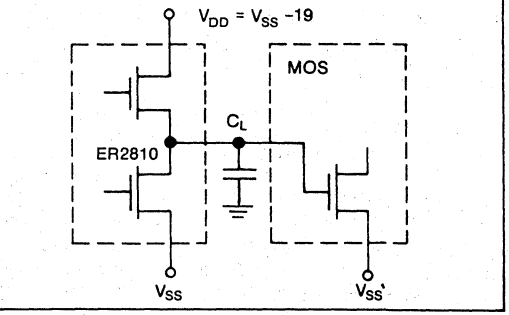
ER2810 OPERATION



TTL INTERFACE



MOS INTERFACE



4096 Bit High Speed Electrically Alterable Read Only Memory

FEATURES

- 1024 word x 4 bit organization
- 10 bit binary addressing
- +5, −12, −30V power supplies
- Word or block alterable
- 10 year data storage for ER3400
- 1 year data storage for ER3400 IR at +85°C and ER3400 HR at +125°C
- TTL compatible with pull-up resistors on inputs
- Tri-state outputs
- Read access time: 900ns max.
- Write time: 1ms, Erase time: 10ms
- 10^9 Read cycles/word between refreshes
- 10^7 Read cycles/word for ER3400 IR and ER3400 HR
- Two extended temperature ranges

DESCRIPTION

The ER3400, ER3400 IR and ER3400 HR are 1024 x 4 bit fully decoded, Electrically Alterable Read Only Memories intended for use as read mostly memories. Word or block alterability of data may be selected by application of the appropriate binary code to the control lines, C0 and C1. These devices operate with one clock, CHIP ENABLE ($\overline{CE}$), which also serves for chip selection.

OPERATION

Selection of one of four possible operating modes is made by setting the correct code on the C0 and C1 lines as defined under "Pin Functions." On-chip latching of the control, address and data imputs occurs on the falling edge of $\overline{CE}$, thus releasing these lines for system use during a Write or Erase operation.

Two points should be noted:

First, an Erase is required before a Write to precondition the memory cells to be written.

Second, both an Erase and a Write operation is terminated by a "Dummy Read" operation, during which data out is not valid. This is necessary to discharge internal, precharged nodes of the circuit and is similar to a normal read except for t_{DS} which must be a minimum of 1500ns. The "Dummy Read" need not occur on the same addressed location as the preceding Write or Erase.

The rising edge of a $\overline{CE}$ pulse in the Erase or Write mode signals the start of the charge trapping mechanism which produces respectively a positive or a negative shift in the threshold voltage of the selected MNOS transistor. An erased location is manifested as a logic '1' on the data output lines.

In the Write mode, a WRITE ENABLE ($\overline{WE}$) pulse in conjunction with a $\overline{CE}$ pulse indicates to the ER3400 that the data on the D0-D3 data bus is valid input data.

$\overline{WE}$ may be tied to $\overline{CE}$ for all operations.

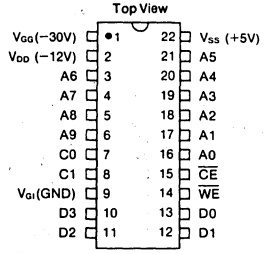
Due to the non-volatile properties of the memory and the unpredictable nature of power up and power down sequences in some systems, power sequencing protection circuitry is provided on the ER3400. Added protection against accidental erasure, should this be necessary, may be afforded by implementing one or more of the following suggestions.

Since V_{GG} is essential for erasing or writing, the most effective precaution is to apply and remove V_{GG} while V_{DD} and V_{SS} are within the specification limits.

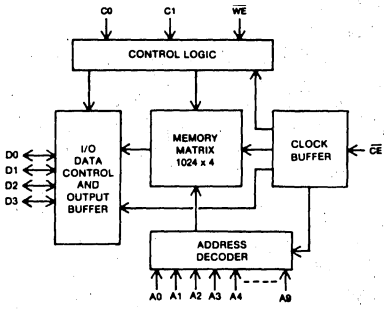
PIN CONFIGURATION

22 LEAD DUAL IN LINE

Top View



BLOCK DIAGRAM



Keeping C0 and C1 low (chip in Read mode) and/or maintaining $\overline{CE}$ high during power-up and power-down will also aid in safeguarding against accidental erasure.

In Read mode, V_{GG} may be tied to V_{SS} resulting in a reduction of power consumption of approximately 30%. Application Note 1203A describes a DC-DC converter circuit capable of producing the −30V, V_{GG} from the +5 and −12V supplies.

The ER3400 IR and ER3400 HR are screened to Mil. Std. 883B/ method 5004.1/ level B, pre-cap visual inspection, environmental testing, burn-in and external visual.

MEMORY CHARACTERISTICS

At some point in time after writing a particular memory location, the stored charge will have decayed beyond the point at which the internal sensing circuitry is capable of distinguishing a logic '1' from a '0'. This time is known as the data retention time. Reprogramming will restore the location to its original, zero-time condition.

Endurance is the number of reprogramming cycles a location may experience before the retention time is reduced beyond that specified.

Both parameters are functions of supply voltage, write and erase time and temperature.

A description of the means by which retention time may be determined appears in Application Note 1210.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs except V_{GG}
(with respect to V_{SS}) ..... −20V to +0.3V
Storage temperature (without data retention) .... −65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = +5V ±5%
V_{DD} = −12V ±5%
V_{GG} = −30V ±5%
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C (ER3400)
−40°C to +85°C (ER3400IR)
−55°C to +125°C (ER3400HR)

		ER3400			ER3400IR/ER3400HR				
Characteristic	Sym	Min	Typ**	Max	Min	Typ**	Max	Unit	Conditions
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	V_{SS} −1.5	—	V_{SS} +0.15	V_{SS} −1.0	—	V_{SS} +0.15	V	
Input Logic "0"	V_{IL}	−10	—	0.8	−10	—	0.6	V	
Output Logic "1"	V_{OH}	V_{SS} −1.5	—	—	V_{SS} −1.5	—	—	V	I_{OH} = 2mA
Output Logic "0"	V_{OL}	—	—	0.4	—	—	0.5	V	I_{OL} = 2mA
Control Input Leakage	I_{LC}	—	—	−2.0	—	—	−2.0	μA	V_{ON} = V_{SS} −15 Volts
Data Input Leakage	I_{LD}	—	—	−10.0	—	—	−10.0	μA	V_{IN} = V_{SS} −15 Volts
Power Supply Current									
V_{DD} Supply Current: Chip selected	I_{DD}	—	—	−25.0	—	—	−27.0	mA	V_{DD} = V_{SS} −17 Volts
Chip de-selected	I_{DD}	—	—	−12.0	—	—	−14.0	mA	V_{DD} = V_{SS} −17 Volts
V_{GG} Supply Current: Write mode	I_{GG}	—	—	−4.0	—	—	−5.0	mA	V_{GG} = V_{SS} −35 Volts
V_{SS} Supply Current: Chip selected	I_{SS}	—	—	−31.0	—	—	−32.0	mA	V_{GG} = V_{SS} −17V, V_{GG} = V_{SS} −35V
Chip de-selected	I_{SS}	—	—	−14.5	—	—	−16.0	mA	V_{GG} = V_{SS} −17V, V_{GG} = V_{SS} −35V
AC CHARACTERISTICS									
Input capacitance—control inputs	C_I	—	6	8	—	6	8	pF	
Input capacitance—data inputs	C_D	—	8	10	—	8	10	pF	
Read Mode Characteristics									
Address and control to $\overline{CE}$	t_{D1}	100	—	—	200	—	—	ns	
Address and control hold time	t_{D2}	250	—	—	300	—	—	ns	
$\overline{CE}$ to Data I/O Off	t_{D3}	50	—	300	50	—	350	ns	
$\overline{CE}$ high	t_{D4}	700	—	—	700	—	—	ns	
$\overline{CE}$ high (Dummy Read)	t_{D5}	1500	—	—	1500	—	—	ns	
Access time	t_A	—	—	900	—	—	1000	ns	RL = 2K to V_{SS}, CL = 100pF
$\overline{CE}$ pulse width	$t_{\overline{CE}}$	1	—	50	1	—	25	μs	
Read cycle time	t_{CY}	1700	—	—	1700	—	—	ns	
$\overline{CE}$ rise, fall time	t_r, t_f	10	—	100	10	—	100	ns	
Write/Erase Mode Characteristics									
Address and control to $\overline{CE}$	t_{D11}	100	—	—	200	—	—	ns	
Address and control hold time	t_{D12}	250	—	—	350	—	—	ns	
$\overline{CE}$ fall to $\overline{WE}$ fall delay	t_{D13}	0	—	—	0	—	—	ns	
$\overline{WE}$ rise to $\overline{CE}$ rise delay	t_{D14}	−50	—	—	−50	—	—	ns	$\overline{WE}$ rise may overlap $\overline{CE}$ rise by a maximum of 50ns.
Data stable to $\overline{WE}$	t_{D15}	0	—	—	0	—	—	ns	
$\overline{WE}$ rise to End of Data Stable	t_{D16}	100	—	—	200	—	—	ns	Data is latched on the chip on the positive edge of WE
$\overline{CE}$ pulse width	$t_{\overline{CE}}$	1	—	50	1	—	25	μs	
$\overline{WE}$ pulse width	$t_{\overline{WE}}$	500	—	—	500	—	—	ns	
Write time	t_W	1	—	2	1	—	2	ms	
Erase time	t_E	10	—	20	10	—	20	ms	
Unpowered Data Storage Time	t_S	10	—	—	1	—	—	yrs.	See Note 2
Number of Reprogramming Cycles	N_W	10^3	—	—	10^3	—	—	—	See Note 2
Number of Read Accesses/Location between refresh	N_{RA}	10^9	—	—	10^7	—	—	—	

**Typical values are at +25°C and nominal voltages.

NOTES: 1. Data read during "dummy read" is not valid data.
2. The minimum t_S is guaranteed for a minimum of 10^3 reprogramming cycles beyond which a logarithmic fall off in retention time is seen with 1 year being a typical value after 10^4 cycles (ER3400 only)
3. Data for ER3400IR and ER3400HR is PRELIMINARY.

TIMING DIAGRAMS

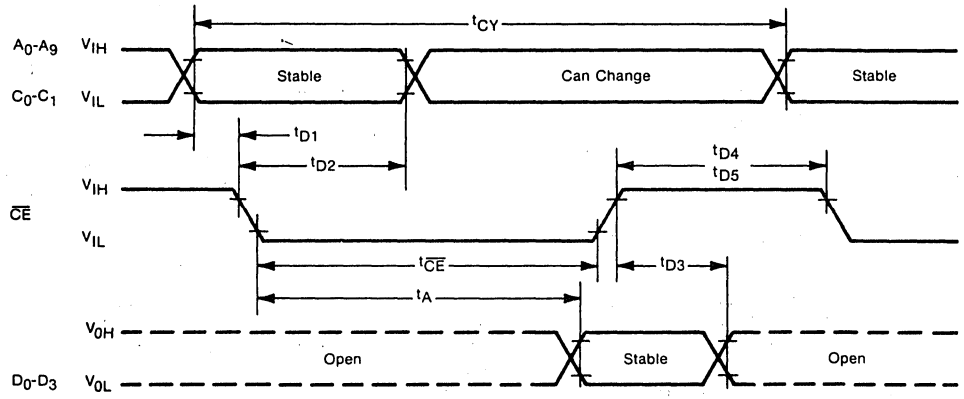


Fig. 1: READ AND DUMMY READ MODE TIMING

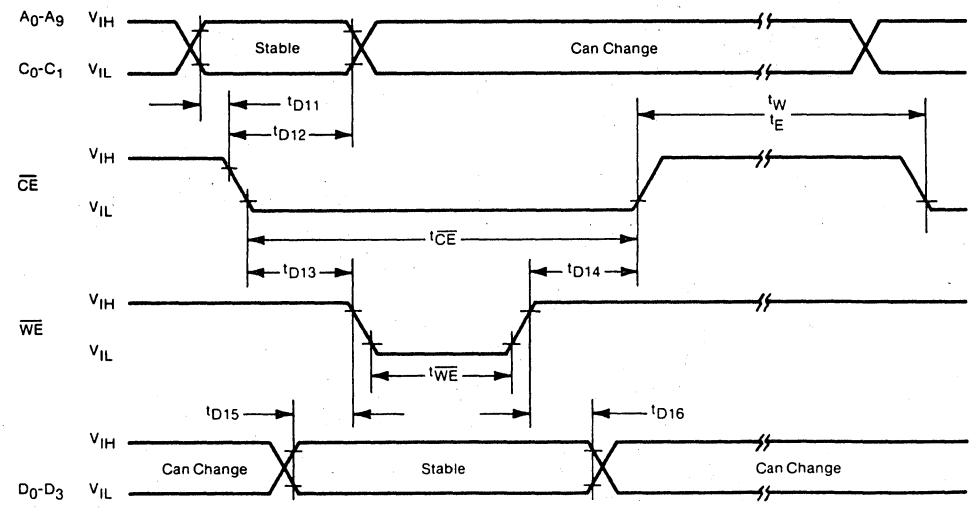


Fig.2: WRITE AND ERASE MODE TIMING

PIN FUNCTIONS

A_0-A_9	10-Bit Word Address
D_0-D_3	Data input and output pins
$\overline{CE}$	Chip Enable. Chip selected when $\overline{CE}$ is pulsed to logic "0".
C_0, C_1	Mode Control Inputs
	C0 C1 0 1 Block Erase Mode: erase operation performed on all words. 1 1 Word Erase Mode: stored data is erased at addressed location. 0 0 Read Mode: addressed data read after leading edge of $\overline{CE}$ pulse. 1 0 Write Mode: input data written at addressed location.
$\overline{WE}$	Write Enable. Input data read when $\overline{WE}$ is pulsed to logic "0".
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input
V_{DD}	Power Supply Input. Normally at -12 volts.
V_{GG}	Power Supply Input. Normally at -30 volts.

TYPICAL CHARACTERISTIC CURVES

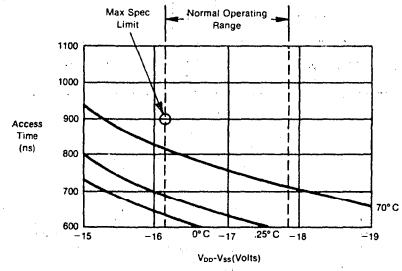


Fig.3: TYPICAL ACCESS TIME vs. POWER SUPPLY VOLTAGE

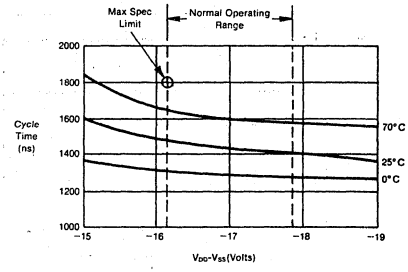


Fig.4: TYPICAL CYCLE TIME vs. POWER SUPPLY VOLTAGE

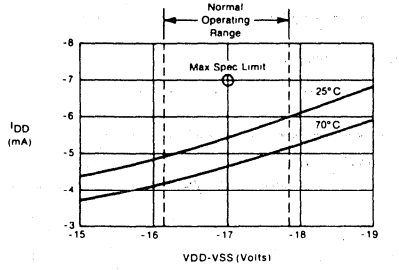


Fig.5: I_{DD} vs. V_{DD}-V_{SS} POWER SUPPLY VOLTAGE IN READ MODE AND NOT SELECTED

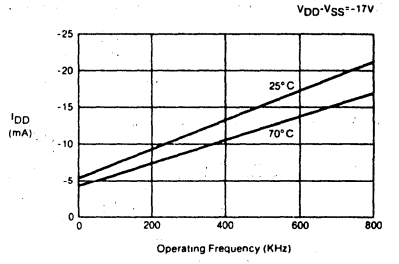


Fig.6: I_{DD} vs. OPERATING FREQUENCY IN READ MODE AND SELECTED

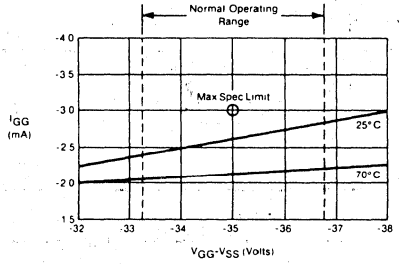


Fig.7: I_{GG} vs. V_{GG}-V_{SS} POWER SUPPLY VOLTAGE IN READ MODE AND NOT SELECTED

Personal Terminal 5

Personal Terminals 5-1

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
"8900" HOME INFORMATION SYSTEM	The "8900" Home Information System is a powerful system for video display of game, educational, financial, research and related "home computer" service information with detailed graphics definition and manipulation.	CP1610	5-3
		GIMINI "8900"	5-9
		AY-3-8900	5-10
		AY-3-8900-1	5-10
		RO-3-9502	5-13
		RO-3-9503	5-16
		RA-3-9600	5-18
	The basic Home Information System can easily be expanded to include additional functions through the use of cartridge ROMs and increased memory, and further enhanced with full color operation, complex sound effects generation, and interface to audio cassette decks and other peripherals.	RO-3-9504	5-21
		AY-3-8910	5-23
		AY-3-8915	5-30
TELEVIEW SYSTEM	The Teleview System is a powerful system to display information on a TV receiver. It can store data from either telephone line or TV RF signals information.	TELEVIEW System	5-32
		PIC 1650A	5-37
		AY-3-9710	5-38
		AY-3-9725	5-45

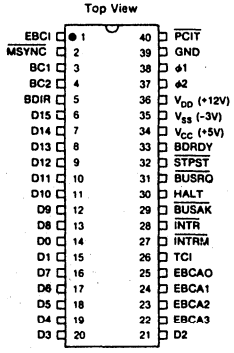
16-Bit Microprocessor

FEATURES

- 8 program accessible 16-bit general purpose registers
- 86 basic instructions
- 4 addressing modes: immediate, direct, indirect, relative
- Conditional branching on status word and 16 external conditions
- Unlimited interrupt nesting and priority resolution
- 16-bit logic and 2's complement arithmetic
- Status logic and word: carry, overflow, sign, zero
- Direct memory access (DMA) for high speed data transfer
- 64K memory using single address
- TTL compatible/simple bus structure
- CP1610: 1μs cycle time, 2MHz 2-phase clock

PIN CONFIGURATION

40 LEAD DUAL IN LINE



DESCRIPTION

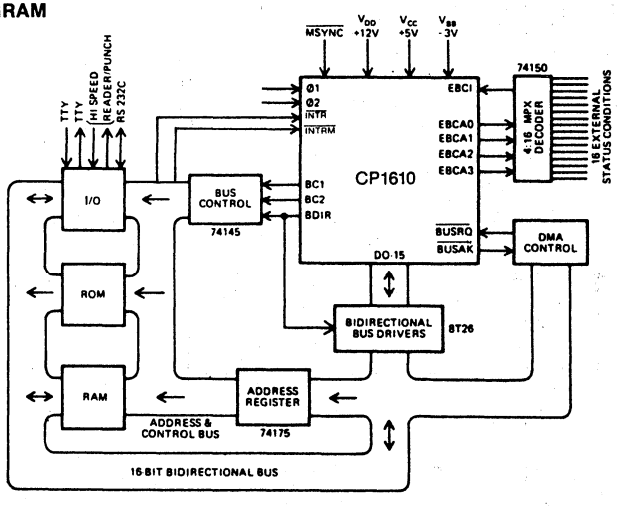
The CP1610 is a compatible member of the Series 1600 Microprocessor products family. It is a complete, 16-bit, single chip, high speed MOS-LSI Microprocessor. The Series 1600 family is fabricated with General Instrument's N-Channel Ion-Implant process, insuring high performance with proven reliability and production history. All members of the Series 1600 family are fully compatible with the CP1610.

The Microprocessor has been designed for high speed data processing and real time applications. Typical applications include programmable TV games, home computer systems/ home information centers, programmable calculator systems, peripheral controllers, process controllers, intelligent terminals and instruments, data acquisition and digital communications processors, numerical control systems and many general purpose mini-computer applications.The Microprocessor can readily support a variety of peripheral equipment such as TTY, CRT display, tape reader/punch, A/D & D/A converter, keyboard, cassette tape, floppy disk, and RS-232C data communication lines.

The CP1610 utilizes third generation minicomputer architecture with eight general purpose registers to achieve a versatile, sophisticated microcomputer system. The 16-bit word enables fast and efficient processing of alphanumeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of program memory, data memory, or peripheral devices. This single address space concept, combined with a powerful instruction set, provides an efficient solution to microcomputer and many minicomputer-based product requirements.

PERSONAL TERMINAL

CP1610 SYSTEM DIAGRAM



PROCESSOR SIGNALS

DATA BUS

D0-D15
Input/Output/High Impedance

Data 0-15: 16-bit bidirectional bus used to transfer data, addresses, and instructions between the microprocessor, memory, and peripheral devices.

PROCESSOR CONTROL

$\overline{\text{STPST}}$
Input
SToP-STart: Edge-triggered by negative transition; used to control the running condition of the microprocessor.

HALT
Output
HALT: indicates that the microprocessor is in a stopped mode.

$\overline{\text{MSYNC}}$
Input
Master SYNC: Active low input synchronizes the microprocessor to the $\phi 1$, $\phi 2$ clocks during power-up initialization.

EBCA 0-3
Outputs
External Branch Condition Addresses 0-3: Address for one-of-16 external digital state tests via the BEXT (Branch on EXTernal) instruction.

EBCI
Input
External Branch Condition Input: Return signal from the one-of-16 selection made by EBCA 0-3.

BUS CONTROL

BDIR, BC1, BC2
Outputs
Bus DIRection, Bus Controls 1, 2: Bus control signals externally decoded to define the state of bus operations (see State Flow Diagram).

$\overline{\text{BUSRQ}}$
Input

$\overline{\text{BUSAK}}$
Output
BUS ReQuest, BUS AcKnowledge: BUSRQ* requests the microprocessor to relinquish control of the bus indefinitely. BUSAK* informs devices that the bus has been released.

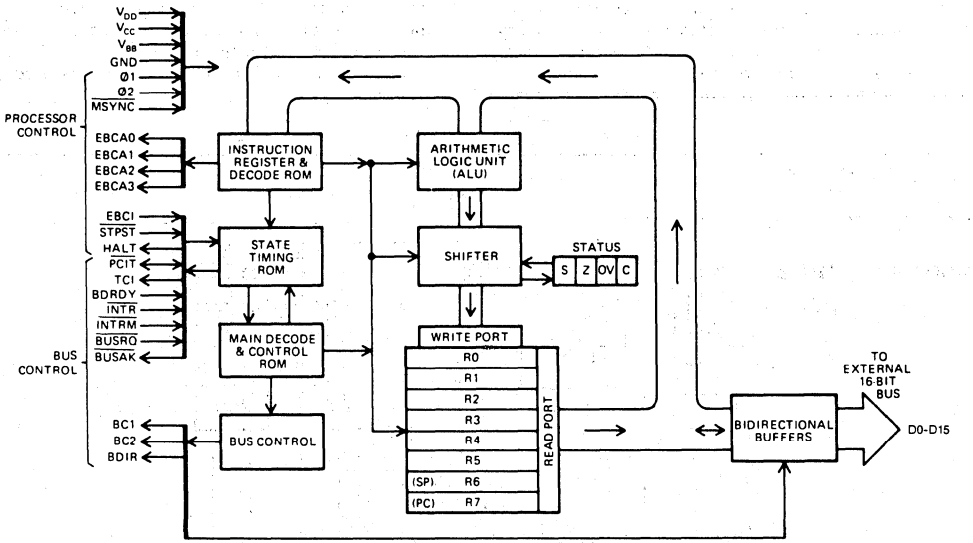
BDRDY
Input
Bus Data ReaDY: causes the microprocessor to "wait" and resynchronize to slow memory and peripheral devices.

$\overline{\text{INTR}}$, $\overline{\text{INTRM}}$
INTeRupt, INTeRupt Masked: request the microprocessor to service an interrupt upon completion of current instruction.

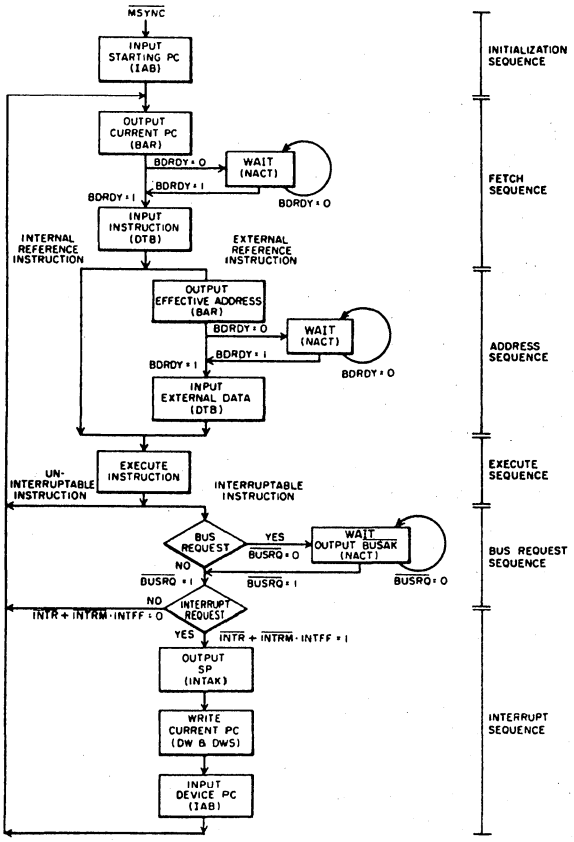
TCI
Output
Terminate Current Interrupt: pulse outputted by the microprocessor in response to the TCI instruction.

$\overline{\text{PCIT}}$
Input/output
Program Counter Inhibit/Trap: As an input, inhibits incrementation of the Program Counter during the instruction fetch sequence. As an output, generates a pulse during execution of a Software INterrupt (SIN) instruction.

CP1610 INTERNAL BLOCK DIAGRAM



SIMPLIFIED STATE FLOW DIAGRAM



BUS CONTROL SIGNALS

BDIR	BC2	BC1	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = high impedance
0	0	1	ADAR	Address Data to Address Register, D0-D15 = high impedance
0	1	0	IAB	Interrupt Address to Bus, D0-D15 = Input
0	1	1	DTB	Data To Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DW	Data Write
1	1	0	DWS	Data Write Strobe
1	1	1	INTAK	INTerrupt AcKnowledge

INSTRUCTION SET (SUMMARY LISTING)

		Mnemonics	Operation	Microcycles				Comments
INTERNAL REFERENCE INSTRUCTIONS	Register to Register	MOVR	MOVe Register	6/7				
		TSTR	TeST Register	6/7				MOVR to itself
		JR	Jump to address in Register	7				MOVR to PC
		ADDR	ADD contents of Registers	6				
		SUBR	SUBtract contents of Registers	6				
		CMPR	CoMPare Registers by subtr.	6				Results not stored
		ANDR	logical AND Registers	6				
		XORR	eXclusive OR Registers	6				
		CLRR	CLeaR Register	6				XORR with itself
	Single Register	INCR	INCrement Register	6				
		DECR	DECrement Register	6				
		COMR	COMplement Register	6				One's Complement
		NEGR	NEGate Register	6				Two's Complement
		ADCR	ADd Carry Bit to Register	6				
		GSWD	Get Status WorD	6				
		NOP	No OPeration	6				
		SIN	Software INterrupt	6				Pulse to $\overline{PCIT}$ pin
		RSWD	Return Status WorD	6				
	Register Shift	SWAP	SWAP 8-bit bytes	6				Not interruptable. One or two position shift capability. Two position SWAP not supported.
		SLL	Shift Logical Left	6				
		RLC	Rotate Left thru Carry	6				
		SLLC	Shift Logical Left thru Carry	6				
		SLR	Shift Logical Right	6				
		SAR	Shift Arithmetic Right	6				
		RRC	Rotate Right thru Carry	6				
		SARC	Shift Arithmetic Right thru Carry	6				
				Add two cycles for 2-position shift.				
	Control Instructions	HLT	HaLT	4				
		SDBD	Set Double Byte Data	4				Must precede external reference to double byte data
		EIS	Enable Interrupt System	4				Not interruptable
		DIS	Disable Interrupt System	4				
		TCI	Terminate Current Interrupt	4				
		CLRC	CLeaR Carry to zero	4				
		SETC	SET Carry to one	4				
	Jump Instructions	J	Jump	12				
		JE	Jump, Enable, interrupt	12				
		JD	Jump, Disable interrupt	12				
		JSR	Jump, Save Return	12				Return Address saved in R4, 5 or 6.
		JSRE	Jump, Save Return & Enable	12				
		JSRD	Jump, Save Return & Disable interrupt	12				
EXTERNAL REFERENCE INSTRUCTIONS	Conditional Branch Instructions	B	unconditional Branch	9*				Two words
		NOPP	No OPeration	7*				Two words
		BC (BLGE)	Branch on Carry	7				C=1
		BNC (BLLT)	Branch on No Carry	7				C=0
		BOV	Branch on OVerflow	7				OV=1
		BNOV	Branch on No OVerflow	7				OV=0
		BPL	Branch on PLus	7				S=0
		BMI	Branch on Minus	7				S=1
		BZE (BEQ)	Branch on ZEro or EQual	7				Z=1
		BNZE (BNEQ)	Branch if Not ZEro or Not EQual	7				Z=0
		BLT	Branch if Less Than	7				S∀OV=1
		BGE	Branch if Greater than or Equal	7				S∀OV=0
		BLE	Branch if Less than or Equal	7				ZV(S∀OV)=1
		BGT	Branch if Greater Than	7				ZV(S∀OV)=0
		BUSC	Branch if Sign≠Carry	7				C∀S=1
		BESC	Branch if Sign=Carry	7				C∀S=0
		BEXT	Branch if External condition is True	7				4 LSB of instruction are decoded select 1 of 16 external conditions.
				Add 2 cycles if test condition is true, except *				Displacement in PC+1 PC←PC±Displacement
	I/O			Dir.	Imm.	Indir.	Stack	
		MVO	MoVe Out	11	9	9	9	Not interruptable
		PSHR	PuSH Register to stack	—	—	—	9	PSHR=MVO@R6. Not interruptable
		MVI	MoVe In	10	8	8	11	
		PULR	PULl from stack to Register	—	—	—	11	PULR=MVI@R6.
	Arithmetic & Logic	ADD	ADD	10	8	8	11	
		SUB	SUBtract	10	8	8	11	
		CMP	CoMPare	10	8	8	11	Result not saved
		AND	logical AND	10	8	8	11	
		XOR	eXclusive OR	10	8	8	11	

1 MICROCYCLE=2 CLOCK CYCLES

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD}, V_{CC}, GND and all other input/output voltages with respect to V_{BB} . . . . . −0.3V to +18.0V
Storage Temperature . . . . . −55°C to +150°C
Operating Temperature . . . . . .0°C to +70°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

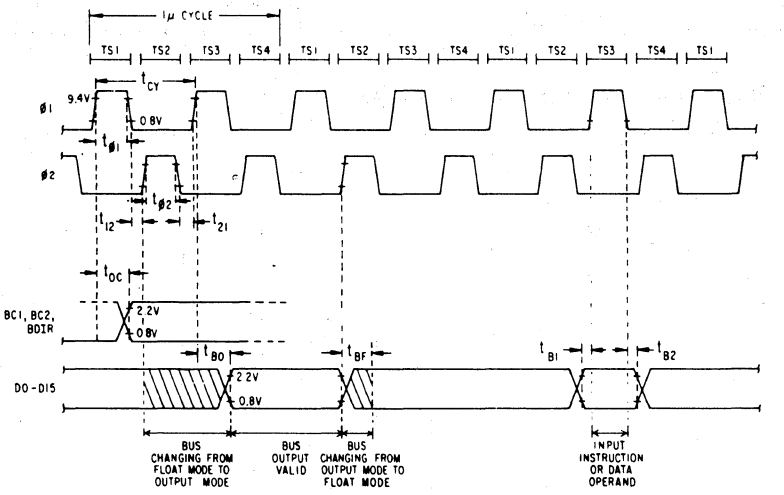
Standard Conditions: (unless otherwise noted)
V_{DD}=+11V±5%, 70mA(typ), 110mA(max.) V_{BB} = −2.2V ± 5%, 0.2mA(typ), 2mA(max.)
V_{CC}=+5V±5%, 12mA(typ), 25mA(max.) Operating Temperature (T_A)=0°C to +70°C

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
High	V_{IHC}	10.0	—	V_{DD}	V	
Low	V_{ILC}	0	—	0.6	V	
Input current	I_C	—	—	15	mA	$V_{IHC} = (V_{DD} - 1)V$
Logic Inputs						
Low	V_{IL}	0	—	0.65	V	
High (All Lines except BDRDY)	V_{IH}	2.4	—	V_{CC}	V	
High (Bus Data Ready Line See Note)	V_{IHB}	3.0	—	V_{CC}	V	
Logic Outputs						
High	V_{OH}	2.4	V_{CC}	—	V	$I_{OH} = 100\mu A$
Low (Data Bus Lines D0-D15)	V_{OL}	—	—	0.5	V	$I_{OL} = 1.6mA$
Low (Bus Control Lines, BC1,BC2,BDIR)	V_{OL}	—	—	0.45	V	$I_{OL} = 2.0mA$
Low (All Others)	V_{OL}	—	—	0.45	V	$I_{OL} = 1.6mA$
AC CHARACTERISTICS						
Clock Pulse Inputs, $\phi1$ or $\phi2$						
Pulse Width	$t\phi2$, $t\phi2$	250		—	ns	
Skew ($\phi1$, $\phi2$ delay)	t_{12}, t_{21}	0	—	—	ns	
Clock Period	t_{cy}	0.5	—	2.0	μs	
Rise & Fall Times	tr, tf	—	—	15	ns	
Master SYNC:						
Delay from ϕ	tms	—	—	30	ns	
D0-D15 Bus Signals						
Output delay from $\phi1$ (float to output)	t_{BO}	—	—	100	ns	1 TTL Load & 100pF
Output delay from $\phi2$ (output to float)	t_{BF}	—	50	—	ns	
Input setup time before $\phi1$	t_{B1}	0	—	—	ns	
Input hold time after $\phi1$	t_{B2}	10	—	—	ns	
Bus Control Signals BC1,BC2,BDIR						
Output delay from $\phi1$	t_{DC}	—	—	100	ns	
Skew	—	—	—	30	ns	
BUSAK Output delay from $\phi1$	t_{BU}	—	150	—	ns	
TCI Output delay from $\phi1$	t_{TO}	—	200	—	ns	
TCI Pulse Width	t_{TW}	—	300	—	ns	
EBCA output delay from BEXT input	t_{DE}	—	—	150	ns	
EBCA wait time for EBCI input	t_{AI}	—	—	400	ns	
CAPACITANCE						TA = +25°C; V_{DD} = +12V; V_{CC} = +5V; V_{BB} = −3V; $t\phi1 = t\phi2 = 120ns$
$\phi1$, $\phi2$ Clock Input capacitance	$C\phi1$, $C\phi2$	—	20	30	pF	
D0-D15	—	—	8	15	pF	
All Other	—	—	5	10	pF	

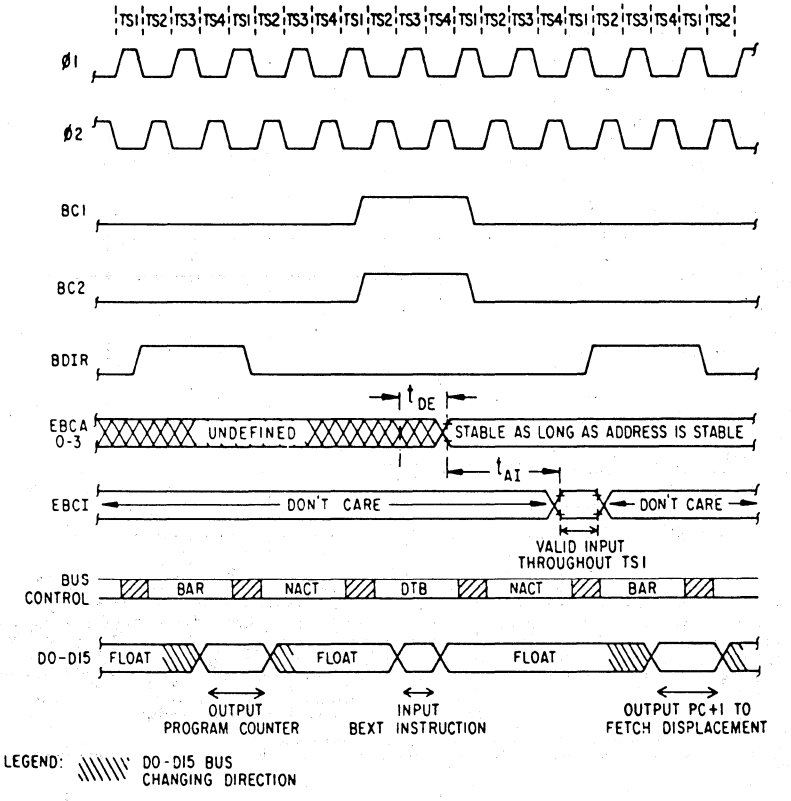
**Typical values are at +25°C and nominal voltages.

NOTE: The Bus Data ReaDY(BDRDY) line is sampled during time period TSI after a BAR or ADAR bus control signal. BDRDY must go low requesting a wait state 50 ns before the end of TS1 and remain low for 50 ns minimum. BDRDY may go high asynchronously. In response to BDRDY, the CPU will extend bus cycles by adding additional microcycles up to a maximum of 40 μsec duration.

CLOCK AND BUS TIMING



TYPICAL INSTRUCTION SEQUENCE (EXTERNAL BRANCH TIMING)



PERSONAL TERMINAL

GIMINI Deluxe "8900" Programmable Game System

FEATURES

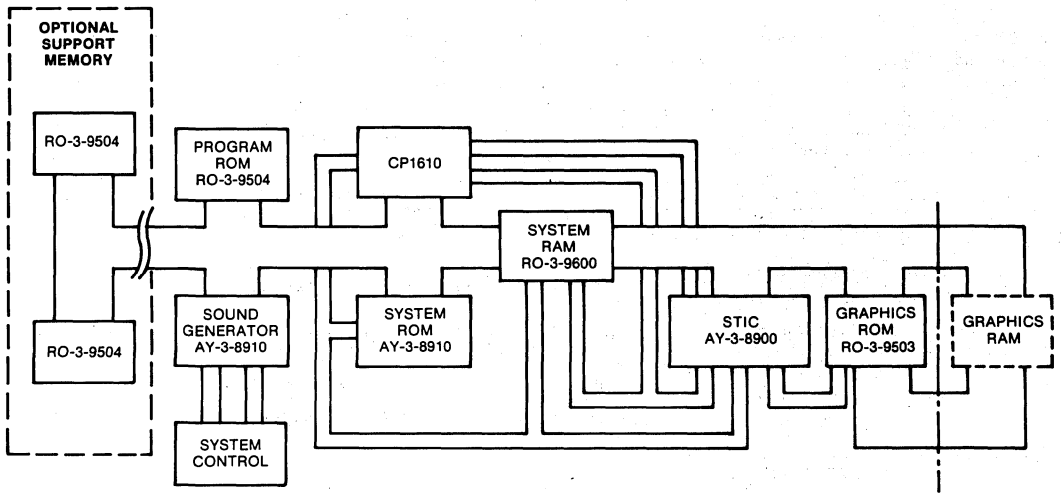
- Infinite game selection
- Lowest cost expandable system
- Uses programmable Read Only Memories with 16K and 20K Storage (RO-3-9502, RO-3-9503, and RO-3-9504)
- Eight color selectable, coordinate addressable game objects
- Resident library of 256 complex game objects, including full 64 character alpha numerics
- Shape library extenable by a further 256 objects using graphics RAM.
- Full multicolor background capability
- Sixteen selectable color tones
- Program controllable moving background
- Two hundred and forty independently programmable background locations

DESCRIPTION

The GIMINI 8900 system is based on two processors; one computes the game action against the stored program rules; and the second interprets a condensed memory area and uses this to generate the T.V. raster display. The second processor fetches moving and background pictures from the graphic picture storage and presents the data as a video output.

The set consists of five General Instrument supplied N-Channel circuits. The AY-3-8900 Standard Television Interface Circuit (STIC); the CP1610 GIMINI Microprocessor; an RO-3-9502 20K program ROM; a similar RO-3-9503 graphics picture ROM and an RA-3-9600 RAM. To complete the system the user supplies clocking and modulation circuitry plus any other peripheral control requirements. Other circuits may be optionally added to expand the system capabilities. They are the AY-3-8910 Sound Generator, the RO-3-9504 ROMs, and Standard RAM devices.

8900 SYSTEM DIAGRAM



Standard Television Interface Chip

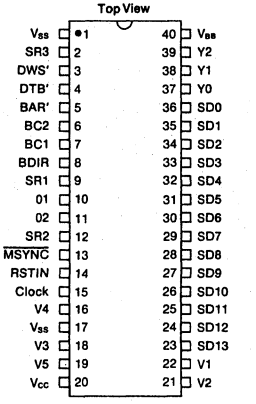
FEATURES

- Outputs include coded signal timings for CCIR or NTSC compatible video signal generation. AY-3-8900 for CCIR, AY-3-8900-1 for NTSC
- Operation from a 4.000MHz clock for AY-3-8900 and from a 3.579545MHz clock for AY-3-8900-1
- 8 coordinate addressable foreground objects on a grid of 168H by 104V for AY-3-8900 or 167H by 105V for AY-3-8900-1 of which 159 x 96 are visible positions
- Foreground objects independently programmable for half height, y zoom, x zoom and 8 or 16 character lines high
- Selectable background display on a matrix of 20H x 12V using 8 x 8 picture elements
- Capable of accepting data, address and graphics information on common multiplexed bus
- 16 digitally selectable colors

PIN CONFIGURATIONS

40 LEAD DUAL IN LINE

AY-3-8900/AY-3-8900-1



PERSONAL TERMINAL

DESCRIPTION

The AY-3-8900/8900-1 STIC is designed for use within a computer system having an external CPU and an area of ROM and RAM memory. Some of the memory must be dedicated to the support of the graphic character descriptors and patterns.

The display facilities of the circuit are separated into two simultaneously operating modes. The main chip function provides eight coordinate positioned "foreground" objects, which have a number of display options including selection from a choice of sixteen colors. The second mode provides a background display facility, which is composed of a matrix of twelve rows by twenty columns of which 19 are composed of 8 x 8 picture elements and the 20th 7 x 8 picture elements. The "background" mode utilizes a dedicated area of external memory (240 by 14 bit words) to store the character control codes for each display position and both modes require some external memory assigned to the storage of the character patterns. The graphic pattern memory is eight bits wide.

The AY-3-8900/8900-1 operates within the computer system by time sharing a bidirectional 14 bit bus. The demultiplexing and the system synchronization are defined by three sets of control signals.

The main synchronization which operates at the T.V. frame rate uses SR1, SR2 and SR3. The SR1 signal occurs once per frame and it is used to synchronize the CPU algorithms to the intended display sequences. SR1 indicates that STIC time is complete and that the AY-3-8900-1 has switched to the CPU controlled mode. SR2 is issued thirteen or fourteen times per picture frame depending on picture offset. The AY-3-8900/8900-1 takes this signal low to request the first line access for a new row of twenty characters.

The SR3 signal operates in conjunction with SR2 to read the "background" character descriptors out of external memory. The AY-3-8900/8900-1 pulses SR3 positive for each character position. Once the first line has been accessed by the SR2, SR3 combination, the following fifteen lines to complete the 8 x 8 array are fetched by SR3 alone.

The SR3 signal is also issued during the CPU controlled mode in response to BAR, ADAR or DW to enable an external device onto the 14 bit BUS.

The second control bus is used to specify address, read and write sequences for the area of external memory used to store the graphic character "dot" patterns. The three signals on this BUS are BAR', DTB' and DWS'. The BAR" is output by the AY-3-8900/8900-1 when a valid graphics character address is on the 14 bit BUS. The external memory must latch this address for future read or write operations. The DTB' signal indicates that a "read" is requested and the external memory must place the eight bits of character pattern onto the 14 bit BUS. The DWS' signal indicates that a "write" is requested.

The graphics control BUS is used during "STIC" time in the fetch of "foreground" object patterns and "background" object patterns. During the non "STIC" time when in the CPU controlled mode, the graphics control BUS can be used to link the memory area containing the graphics patterns to the main memory area of the external microprocessor.

The third control BUS communicates with the external CPU. This BUS comprises signals BC1, BC2 and BDIR. They are coded to signify address, read and write sequences. The CPU control BUS is only validated if the AY-3-8900/8900-1 is in the CPU controlled mode, otherwise it is ignored.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +40°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{BB} ..... −0.2V to +9.0V
V_{CC}, V_{DD} & V_{SS} with Respect to V_{BB} ..... −0.2V to +9.0V

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

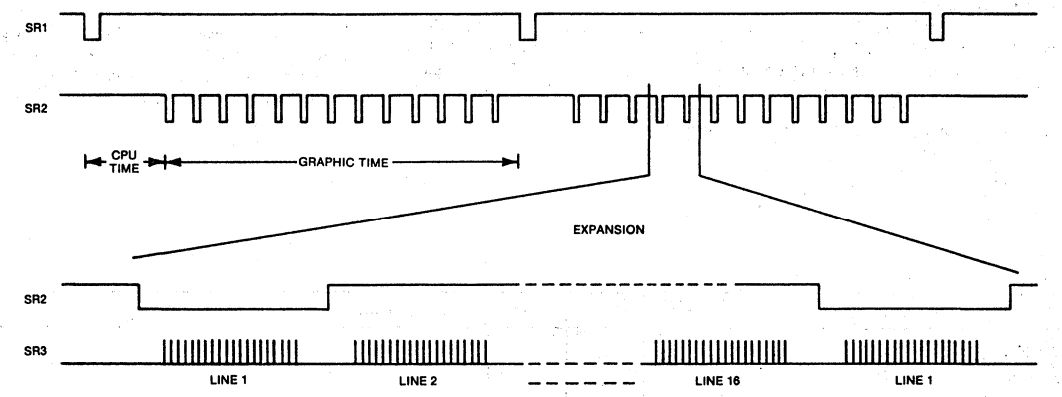
Standard Conditions (unless otherwise stated)

T_A = 0°C to +40°C, V_{BB} = −3.3V,
V_{CC} = ±4.85V—±5.15V, V_{SS} = 0.0V

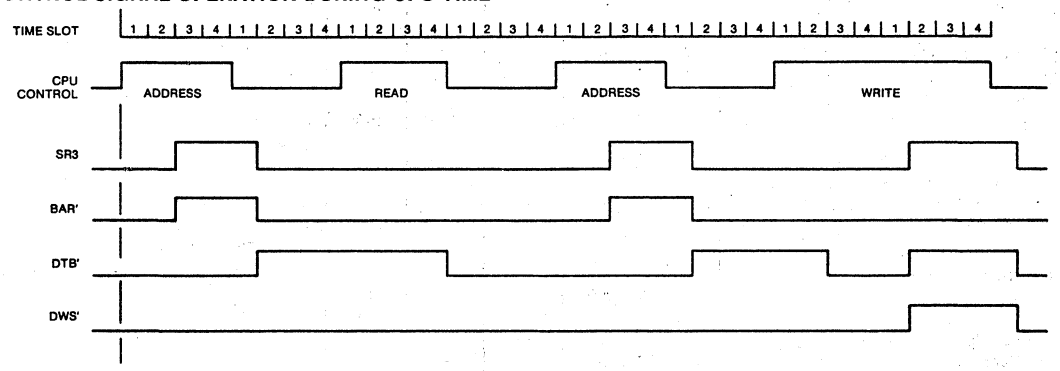
Characteristic	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Bus Inputs						
Input Logic Low	V_{IL}	0	—	0.7	V	
Input Logic High	V_{IH}	2.4	—	—	V	
Input Current	I_{IL}	—	—	10	μA	$V_{in} = V_{CC}$
Bus Outputs						
Output Logic Low	V_{OL}	0	—	0.5	V	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	V	+100pF
Supply Current						
V_{CC} Supply	I_{CC}	—	—	200	mA	V_{CC} = +5.25V @40°C
AC CHARACTERISTICS						
Clock Input Freq.	f_{CI}	—	—	—	MHz	4.000 for AY-3-8900 3.579545 for AY-3-8900-1 both externally adjusted
Bus Inputs						
Address Set Up	t_{AS}	200	—	—	ns	
Address Overlap	t_{AO}	30	—	—	ns	
Write Set Up	t_{WS}	100	—	—	ns	
Write Overlap	t_{WO}	30	—	—	ns	
Bus Outputs						
Turn ON Delay	t_{DA}	—	—	140	ns	1 TTL Load
Turn OFF Delay	t_{DO}	0	—	—	ns	+100pF

PERSONAL TERMINAL

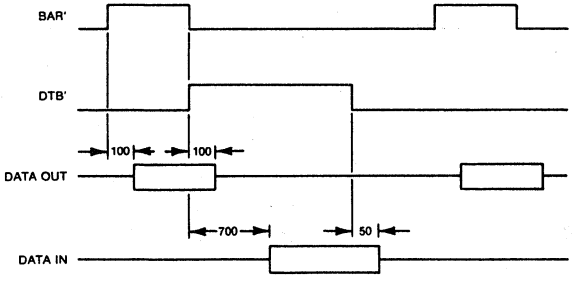
SYSTEM SYNCHRONIZATION TIMING



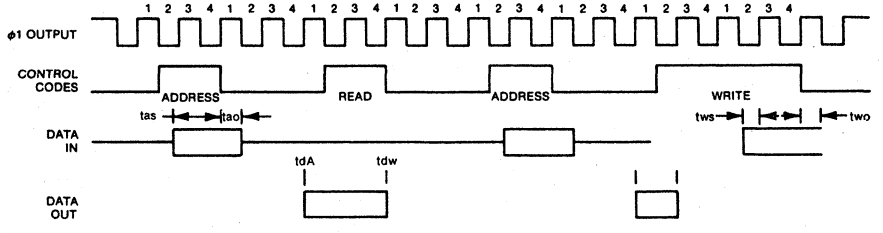
CONTROL SIGNAL OPERATION DURING CPU TIME



OBJECT FETCH TIMING



AY-3-8900-1 CPU CONTROL TIMING



Program ROM

FEATURES

- Mask programmable storage providing 2048 x 10 bit words
- 16 bit on-chip address latch
- Control decoder
- Programmable memory map circuitry to place 2K ROM page within 65K word memory space located on 2K page boundaries
- Master logic with programmable 16 bit vectored start address
- Interrupt logic with programmable 16 bit vectored interrupt address
- 16 bit static address outputs for external memory
- Control signals for external memory:
  ENABLE = (DTB + DWS) Address External = R/$\overline{E}$
  WRITE = DWS. Address External = R/$\overline{W}$
- Programmable memory map selection for external memory area
- Bus drive capability, 1 TTL load and 100pF plus tri-state

CIRCUIT REQUIREMENTS

The RO-3-9502 operates as the program memory for systems using a CP1610 series microprocessor.

It is configured as 2048 x 10 bit words and contains several features which reduce the device count in a practical microprocessor application.

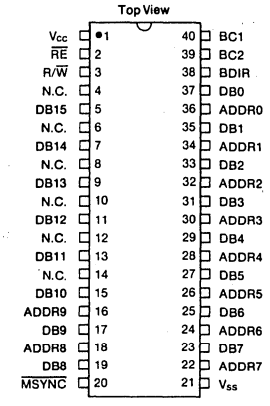
OPERATING DESCRIPTION

The RO-3-9502 is initialized by the MSYNC Input and from the positive edge of this signal, it remains in a tri-state output condition, awaiting the IAB response. During the IAB, the 9502 transmits a 16 bit code onto the external bus thus providing the system start address vector. The completion of the MCLR sequence is recorded on chip such that any further IAB Codes output the second interrupt vector. From initialization, the 9502 waits for the first address code. For this address code and all subsequent address sequences, the 9502 reads the 16 bit external bus and latches the value into its address register. The contents of this address register are made available for connection to external memory and are supplied on 16 latched outputs with a drive capability of 1 TTL load and 100pF.

The 9502 contains a programmable memory map location for its own 2K page and if a valid address is detected, the particular addressed location will transfer its contents to the chip output buffers. If the control code following the address cycle was a Read, the 9502 will output the 10 bits of addressed data and also drive a logic zero on the top six bits of the bus.

PIN CONFIGURATIONS

40 LEAD DUAL IN LINE



INPUT CONTROL SIGNALS

BDIR	BC1	BC2	EQUIVALENT SIGNAL	RESPONSE
0	0	0	NACT	NACT
0	0	1	IAB	IAB
0	1	0	ADAR	ADAR
0	1	1	DTB	DTB
1	0	0	BAR	BAR
1	0	1	DWS	—
1	1	0	DW	—
1	1	1	INTAK	—

OPERATION WITH EXTERNAL MEMORY

The 16 bits from the address register are provided as static outputs for connection to external ROM or RAM devices. Two other signals are provided to control the external memory area. An enable signal is provided for any read or write operation, and a write signal, for any move out operation. The two external memory control signals are gated by a min-max memory map comparator. The minimum and maximum values are programmable on boundaries within the 65K word memory area. The memory map comparator for external memory is a simple single compare and the operation is such that when a 2K area is chosen, a five bit compare is used and for a 4K area a four bit compare, etc. The effect of this is that 2K pages may start on 2K boundaries, i.e., 0, 2, 4, 6, 8 etc., but 4K pages must be on 4K boundaries, i.e., 0, 4, 8, 12, etc. The same is true for 8K and 16K pages.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +40°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +9.0V
V_{CC} with Respect to V_{SS} ..... −0.2V to +9.0V

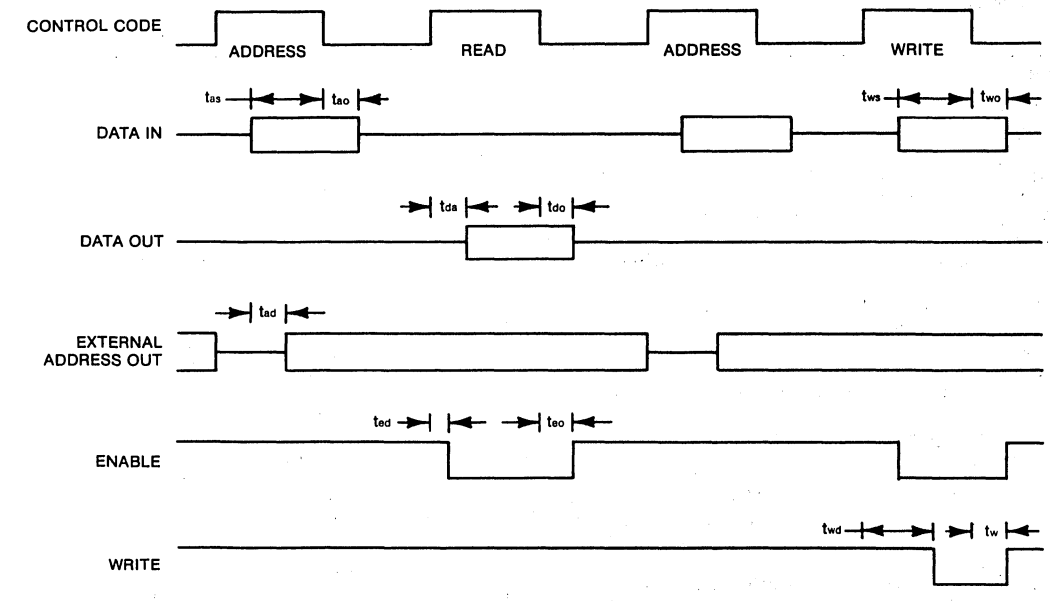
* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

T_A = 0°C to +40°C V_{SS} = 0.0V
V_{CC} = +4.85V − +5.15V

Characteristic	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Inputs						
Input Logic Low	V_{IL}	0	—	0.7	volts	
Input Logic High	V_{IH}	2.4	—	V_{CC}	volts	
Input Leakage	V_{IL}	—	—	10	μA	$V_{IN} = V_{CC}$
CPU BUS Outputs						
Output Logic Low	V_{OL}	0	—	0.5	volts	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	volts	+100pF
Address and Enable Outputs						
Output Logic Low	V_{OL}	0	—	0.5	volts	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	volts	+100pF
Supply Current						
V_{CC} Supply	I_{CC}	—	—	120	mA	V_{CC} = 5.25V @ 40°C
AC CHARACTERISTICS						
Inputs						
Address Set Up	t_{as}	300	—	—	nsec	
Address Overlap	t_{ao}	—	50	—	nsec	
Write Set Up	t_{ws}	300	—	—	nsec	
Write Overlap	t_{wo}	—	50	—	nsec	
CPU BUS Outputs						
Turn ON Delay	t_{da}	—	—	300	nsec	1 TTL Load
Turn OFF Delay	t_{do}	—	—	200	nsec	+100pF
Address and Enable Outputs						
Turn ON Delay	t_{ad},t_{ed}	—	—	200	nsec	
Turn OFF Delay	t_{eo}	—	—	150	nsec	
Turn ON Delay	t_{wd}	—	—	300	nsec	
Turn OFF Delay	t_{wo}	—	—	150	nsec	

MEMORY TIMING RO-3-9502



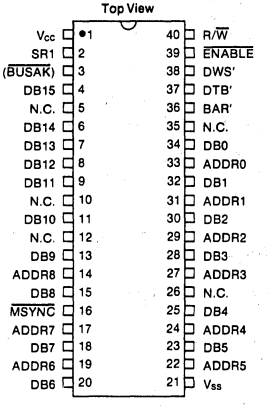
Graphics ROM

FEATURES

- Mask programmable storage providing 2048 x 8 bit words
- 16 bit on-chip address latch
- Memory map circuitry to place the 2K ROM page within a 65K memory area
- 8 bit tri-state bus with higher 8 bits driven to zero during read operations
- 11 bit, static address outputs for external memory
- Control signals for external memory:
  $\overline{\text{ENABLE}}$
  R/$\overline{\text{W}}$
- Bus drive capability, 1 TTL load and 100pF plus tri-state

PIN CONFIGURATIONS

40 LEAD DUAL IN LINE



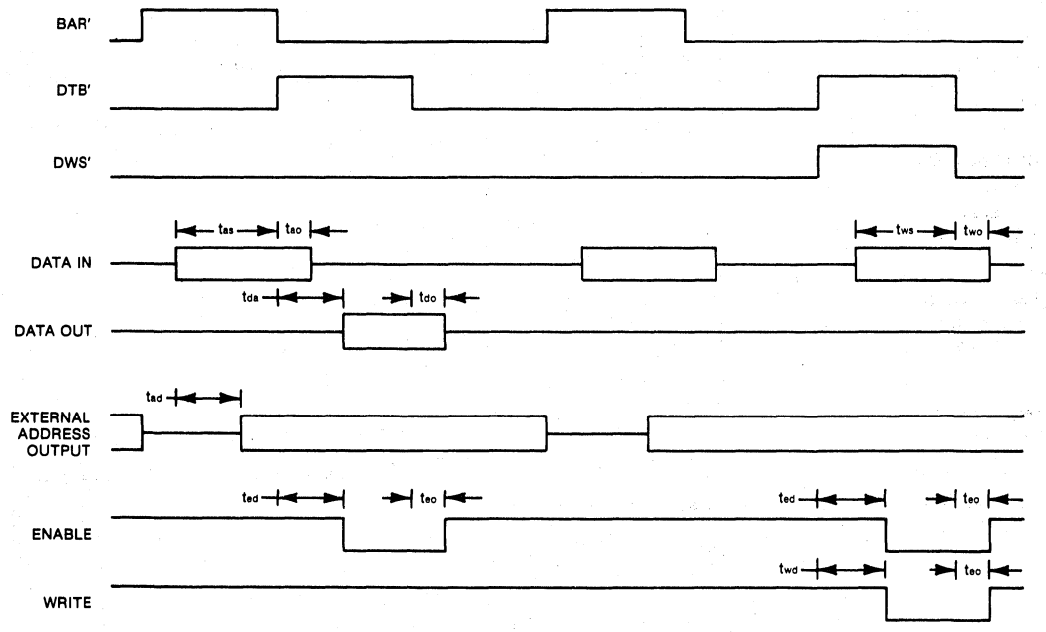
OPERATING DESCRIPTION

The device operates in three memory configurations. These configurations are selected via the input control signals.

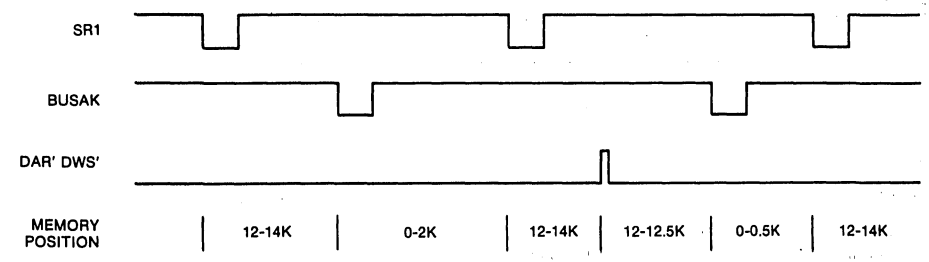
1. When SR1 has been pulsed negative, the memory is located at 12288 to 14335. The external memory is addressed at 14336 to 16383.
2. When $\overline{\text{BUSAK}}$ has been pulsed negative, the memory is located at 0 to 2047. The external memory is addressed at 2048 to 4095.
3. When BAR' and DWS' are pulsed positive, the memory will not respond to address bit 9 and address bit 10, which restricts the memory to 512 locations. The memory is now located from 0 to 511 relative to the current memory origin. The external memory is also addressable from 0 to 511 relative to its current origin. Configuration three may be released by applying a negative pulse on the SR1 input.

PERSONAL TERMINAL

MEMORY TIMING



MEMORY POSITION RELATIVE TO CONTROL OPERATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +40°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +9.0V
V_{CC} with respect to V_{SS} ..... −0.2V to +9.0V

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

T_A = 0°C to +40°C
V_{CC} = +4.85V − + 5.15V
V_{SS} = 0.0V

Characteristic	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Bus Inputs						
Input Logic Low	V_{IL}	0	—	0.7	Volts	
Input Logic High	V_{IH}	2.4	—	V_{CC}	Volts	
Input Leakage	I_{IL}	—	—	10	μA	$V_{IN} = V_{CC}$
CPU BUS Outputs						
Output Logic Low	V_{OL}	0	—	0.5	Volts	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	Volts	+100pF
Address and Enable Outputs						
Output Logic Low	V_{OL}	0	—	0.5	Volts	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	Volts	+100pF
Supply Current						
V_{CC} Current	I_{CC}	—	—	150	mA	V_{CC} = +5.25V @ 40°C
AC CHARACTERISTICS						
Bus Inputs						
Address Set Up	t_{as}	300	—	—	nsec	
Address Overlap	t_{ao}	—	50	—	nsec	
Write Set Up	t_{ws}	300	—	—	nsec	
Write Overlap	t_{wo}	—	50	—	nsec	
CPU BUS Outputs						
Turn ON Delay	t_{da}	—	—	300	nsec	1 TTL Load
Turn OFF Delay	t_{do}	—	—	200	nsec	+100pF
Address and Enable Outputs						
Turn ON Delay	t_{ad},t_{ed},t_{wd}	—	—	200	nsec	1TTL Load
Turn OFF Delay	t_{eo}	—	—	100	nsec	+100pF

All delays measured between 2.2 Volts and 0.7 Volts test points

PERSONAL TERMINAL

System RAM

FEATURES

- Memory area 352 words of 16 bits
- Address counter and control logic for D.M.A. operation
- Control decoder for CPU data control signals
- Memory map comparator and control logic for additional memory on 14 bit bus
- Current line buffer — 20 words of 14 bits
- Drive capability on 16 bit and 14 bit bus for 1 TTL load and 100pF

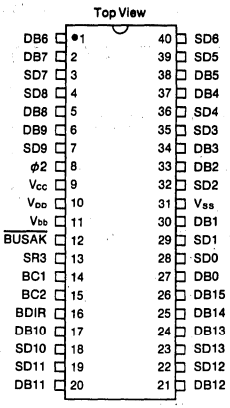
FUNCTIONAL DESCRIPTION

The RA-3-9600 is a 'dual port' interface and 16 bit wide RAM storage area. The RA-3-9600 contains twenty 14 bit serial data buffer registers with separate bus control signals.

The RA-3-9600 memory is 352 x 16 bit contiguous words from address 512-863 with the graphics descriptors using the first 240 words. The graphics use only the lower 14 bits of each word leaving the two most significant bits available for user storage.

PIN CONFIGURATIONS

40 LEAD DUAL IN LINE



OPERATION DESCRIPTION

The RA-3-9600 RAM accepts data from the CPU via a 16 bit bi-directional bus which is time multiplexed with address and data. A 3 bit control bus from the CPU is used to provide strobe signals for the on-chip address latch and main memory area.

The RAM has two operating modes:

Mode 1 — On decoding an interrupt the RAM is enabled into a bus copy mode. In this mode the RAM copies the lower fourteen bits of the CPU bus onto the graphics bus. The direction of copy is always from the CPU and towards the graphics except during a bus reversal condition. The reversal condition is indicated when the CPU requests a read from an external graphics address on the 14 bit bus. Under this condition the 9600 will turn its 14 bit bus outputs into tri-state and gate the 14 bit bus through to the 16 bit CPU bus.

Mode 2—Is selected when the CPU issues $\overline{\text{BUSAK}}$ command (DMA request). The effect of $\overline{\text{BUSAK}}$ inside the 9600 is to reset the interrupt synchronizing logic and to switch the address decoder from the CPU address register to the graphics address counter. This counter, which sequences through the 240 words of graphics data, will have been previously set to zero when the interrupt signal was decoded. When the CPU is in the DMA state, the graphics system will prepare to display a new row of twenty characters and to load the 20 buffer registers within the 9600. For the first cycle of DMA after interrupt the graphics address counter will be at zero and the data at that address is passed to the 14 bit output. The action of SR3 will enable the output buffers and drive the 14 bit bus. The twenty shift registers are also loaded at this time. The negative edge of SR3 tri-states the 14 bit output and increments the graphics address counter. The shift registers are also clocked at this time. The SR3 input provides twenty positive pulses to the 9600 and loads the shift register buffers while giving the graphics the first row of characters. At the end of the first DMA cycle, after the CPU interrupt, the graphics address counter will be at value 20. The 9600 operation for the next fifteen lines will be to clock the 20 shift registers and gate the contents onto the 14 bit bus under control of the SR3 input. When the CPU is running and $\overline{\text{BUSAK}}$ is a logic 1, the graphics address counter is not incremented and it stays at the value 20. At the end of the first row of characters, the complete DMA operation is repeated and the address counter will be left at 40. This sequence occurs for the 12 rows of characters until all 240 have been successfully accessed.

The operation of SR3, INCREMENT/TRI-STATE signal, is to step the shift register sequentially through each of the twenty characters. If the $\overline{\text{BUSAK}}$ signal is low, i.e., in DMA, it also increments the graphics ADDRESS COUNTER. SR3 disables the 14 bit graphics bus during the low period.

At the end of active picture the STIC issues an interrupt request to the CPU. The RA-3-9600 tests for the INTAK* response from the CPU and uses this signal as an entry control for a copy mode between the two buses. The end of the copy mode is controlled by the first $\overline{\text{BUSAK}}$ negative edge.

*INTAK, equivalent BC1, BC2, BDIR = '1'

PERSONAL TERMINAL

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +40°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltage With Respect to V_{BB} ..... −0.2V to +18.0V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB} ..... −0.2V to +18.0V

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

T_A = 0°C to +40°C
V_{CC} = +4.85V—+5.15V
V_{DD} = +11.6V—+12.4V
V_{BB} = −3.3V

Characteristic	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
Clock Input Freq. $\phi 2$	—	—	—	—	MHz	1.79545MHz
Input Logic Low	V_{ILC}	0	—	0.7	Volts	
Input Logic High	V_{IHC}	2.4	—	V_{DD}	Volts	
Input Current	I_{ILC}	—	—	10	μA	$V_{in} = V_{CC}$
Bus Inputs and Control Inputs						
Input Logic Low	V_{IL}	0	—	0.7	Volts	
Input Logic High	V_{IH}	2.4	—	V_{CC}	Volts	
Input Currents	I_{IL}	—	—	10	μA	$V_{in} = V_{CC}$
Bus Outputs						
Output Logic Low	V_{IL}	0	—	0.5	Volts	1 TTL Load
Output Logic High	V_{OL}	2.4	—	V_{CC}	Volts	+100pF
AC CHARACTERISTICS						
Clock Input						
Rise & Fall Time	tr, tf	—	—	50	nsec	
CPU Bus Timing						
Address Set Up Time	tas	300	—	—	nsec	
Address Hold Time	tao	—	—	50	nsec	
Data Access Time	tda	—	—	500	nsec	1 TTL Load
Data Hold Time	tdo	—	100	—	nsec	+100pF
Write Data Setup	tws	100	—	—	nsec	
Write Data Hold	tas	0	—	—	nsec	
Graphics Bus Timing						
Data Access Time	tga	—	—	150	nsec	1 TTL Load
Data Hold Time	tgo	—	100	—	nsec	+100pF

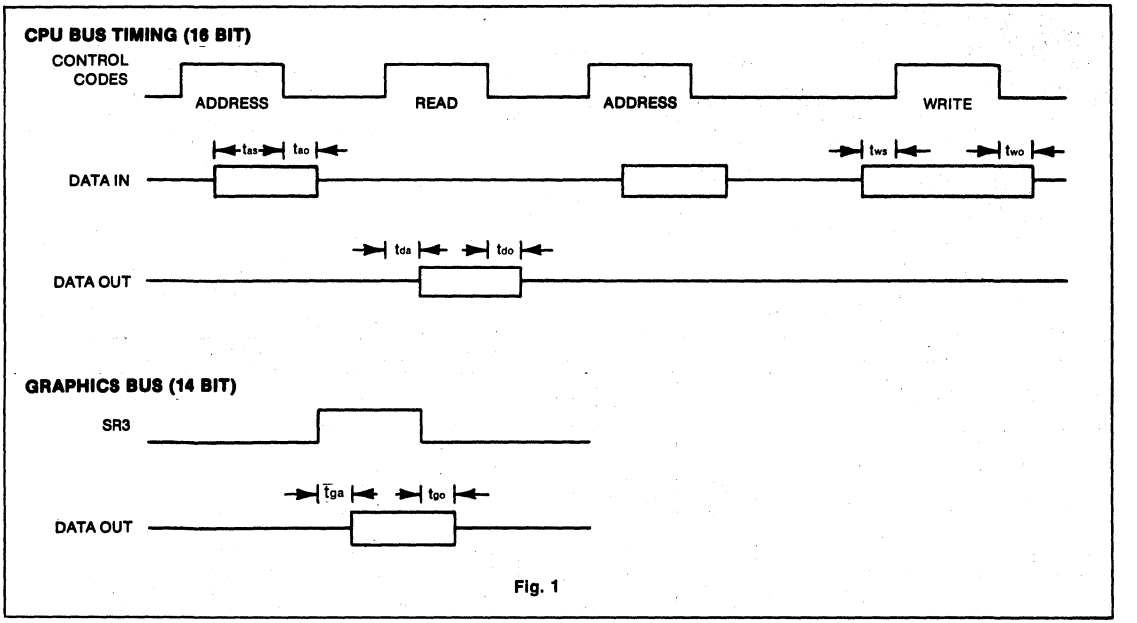


Fig. 1

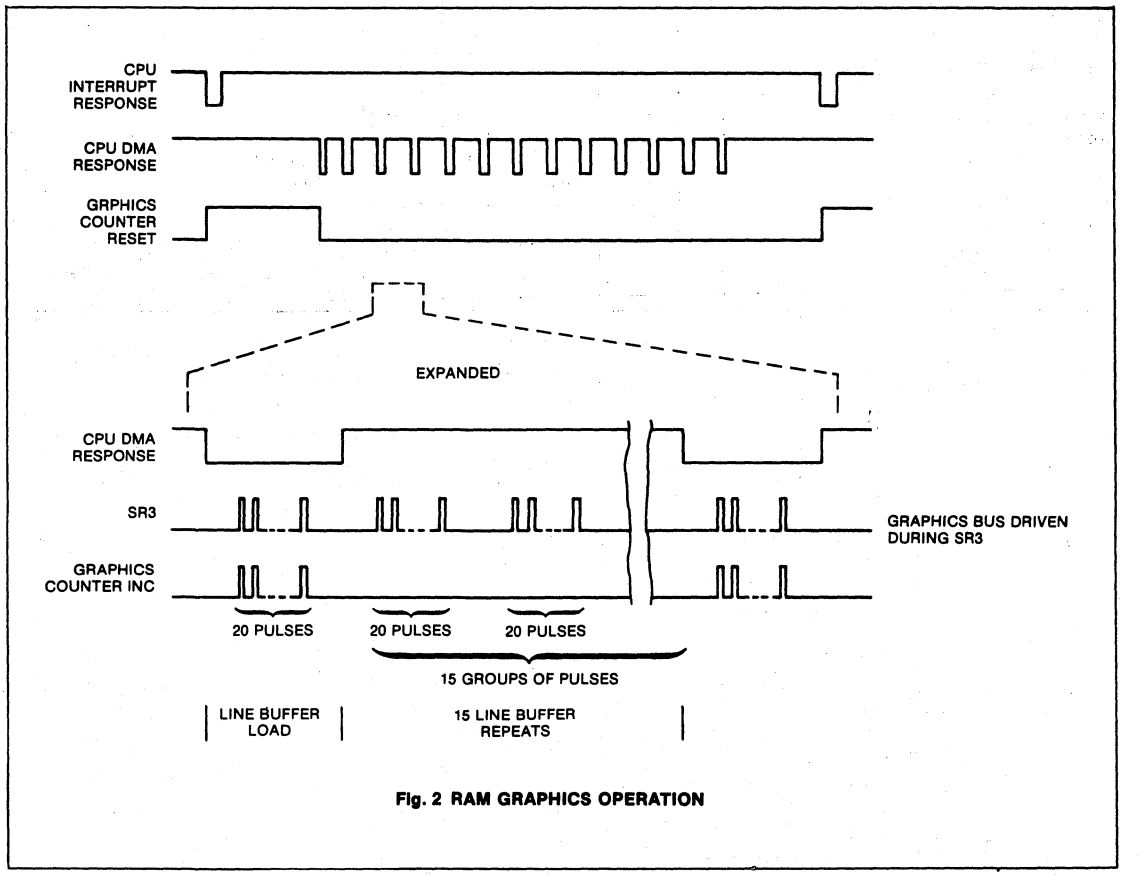


Fig. 2 RAM GRAPHICS OPERATION

Cartridge ROM

FEATURES

- Mask programmable storage providing 2048 x 10 bit words
- 16 bit on-chip address latch
- Memory map circuitry to place the 2K ROM page within a 65K Memory area
- 16 bit tri-state bus with higher 6 bits driven to zero during read operations

CIRCUIT REQUIREMENTS

The RO-3-9504 operates as the program memory for systems using a CP1610 microprocessor. It is configured as 2048 x 10 bit words and contains several features which reduce the device count in a practical microprocessor application.

DESCRIPTION

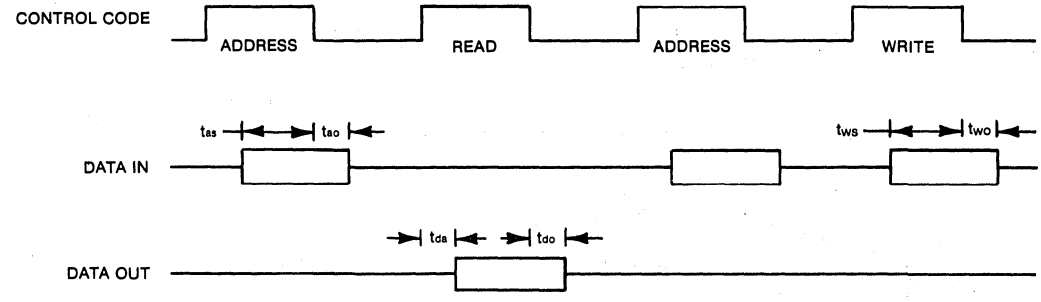
From initialization, the RO-3-9504 waits for the first address code, i.e., BAR. For this address code and all subsequent address sequences, the 9504 reads the 16-bit external bus and latches the value into its address register.

The 9504 contains a programmable memory map location for its own 2K page, and if a valid address is detected, the particular address location will transfer its contents to the chip output buffers. If the control code following the address cycle was a READ, the 9504 will output the 10 bits of addressed data and drive a logic zero on the top six bits of the bus:

INPUT CONTROL SIGNALS

BDIR	BC1	BC2	EQUIVALENT SIGNAL	RESPONSE
0	0	0	NACT	NACT
0	0	1	IAB	NACT
0	1	0	ADAR	ADAR
0	1	1	DTB	DTB (READ)
1	0	0	BAR	BAR
1	0	1	DWS	—
1	1	0	DW	—
1	1	1	INTAK	—

MEMORY TIMING RO-3-9504



PERSONAL TERMINAL

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +40°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +9.0V
V_{CC} with respect to V_{SS} ..... −0.2V to +9.0V

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

T_A = 0°C to +40°C
V_{CC} = +4.85V − + 5.15V
V_{SS} = 0.0V

Characteristic	Sym	Min	Typ	Max	Units	Conditions
DC CHARACTERISTICS						
Inputs						
Input Logic Low	V_{IL}	0	—	0.7	volts	
Input Logic High	V_{IH}	2.4	—	V_{CC}	volts	
Input Leakage	V_{IL}	—	—	10	μA	$V_{IN} = V_{CC}$
CPU BUS Outputs						
Output Logic Low	V_{OL}	0	—	0.5	volts	1 TTL Load
Output Logic High	V_{OH}	2.4	—	V_{CC}	volts	+100pF
Supply Current						
V_{CC} Supply	I_{CC}	—	—	120	mA	V_{CC} = 5.25V @ 40°C
AC CHARACTERISTICS						
Inputs						
Address Set Up	t_{as}	300	—	—	nsec	
Address Overlap	t_{ao}	—	50	—	nsec	
Write Set Up	t_{ws}	300	—	—	nsec	
Write Overlap	t_{wo}	—	50	—	nsec	
CPU BUS Outputs						
Turn ON Delay	t_{da}	—	—	300	nsec	1 TTL Load
Turn OFF Delay	t_{do}	—	—	200	nsec	+100pF

Programmable Sound Generator

FEATURES

- Full software control of sound generation
- Interfaces to most 8-bit and 16-bit microprocessors
- Three independently programmed analog outputs
- Two 8-bit general purpose I/O ports (AY-3-8910)
- One 8-bit general purpose I/O port (AY-3-8912)
- Single +5 Volt Supply

DESCRIPTION

The AY-3-8910/8912 Programmable Sound Generator (PSG) is a Large Scale Integrated Circuit which can produce a wide variety of complex sounds under software control. The AY-3-8910/8912 is manufactured in GI's N-Channel Ion Implant Process. Operation requires a single 5V power supply, a TTL compatible clock, and a microprocessor controller such as the GI 16-bit CP1600/1610 or one of GI's PIC 1650 series of 8-bit microcomputers.

The PSG is easily interfaced to any bus oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signalling and FSK modems. The analog sound outputs can each provide 4 bits of logarithmic digital to analog conversion, greatly enhancing the dynamic range of the sounds produced.

In order to perform sound effects while allowing the processor to continue its other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one effect is satisfied by the three independently controllable channels available in the PSG.

All of the circuit control signals are digital in nature and intended to be provided directly by a microprocessor/microcomputer. This means that one PSG can produce the full range of required sounds with no change in external circuitry. Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction with only the simplest electrical connections.

Since most applications of a microprocessor/PSG system would also require interfacing between the outside world and the microprocessor, this facility has been designed into the PSG. The AY-3-8910 has two general purpose 8-bit I/O ports and is supplied in a 40 lead package; the AY-3-8912 has one port and 28 leads.

PIN FUNCTIONS

DA7--DA0 (input/output/high impedance): pins 30--37 (AY-3-8910)
Data/Address 7--0: pins 21--28 (AY-3-8912)

These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG and to receive data from the PSG. In the data mode, DA7--DA0 correspond to Register Array bits B7--B0. In the address mode, DA3--DA0 select the register # ($0--17_8$) and DA7--DA4 in conjunction with address inputs $\overline{A9}$ and A8 form the high order address (chip select).

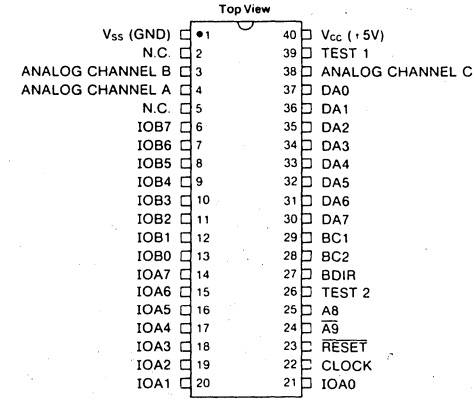
A8 (input): pin 25 (AY-3-8910)
pin 17 (AY-3-8912)
$\overline{A9}$ (input): pin 24 (AY-3-8910)
(not provided on AY-3-8912)

Address 9, Address 8

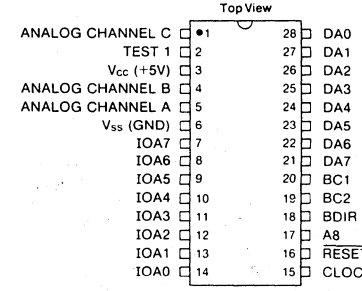
These "extra" address bits are made available to enable the positioning of the PSG (assigning a 16 word memory space) in a total 1,024 word memory area rather than in a 256 word memory area as defined by address bits DA7--DA0 alone. If the memory size does not require the use of these extra address lines they may be left unconnected as each is provided with either an on-chip pull down ($\overline{A9}$) or pull-up (A8) resistor. In "noisy" environments, however, it is recommended that A9 and A8 be tied to an external ground and +5V, respectively, if they are not to be used.

PIN CONFIGURATIONS

40 LEAD DUAL IN LINE
AY-3-8910



28 LEAD DUAL IN LINE
AY-3-8912



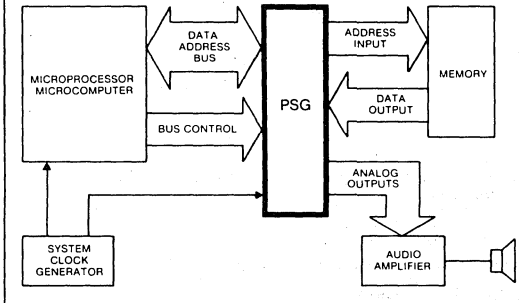


Fig. 1 SYSTEM BLOCK DIAGRAM

PERSONAL TERMINAL

RESET (input): pin 23 (AY-3-8910)
pin 16 (AY-3-8912)

For initialization/power-on purposes, applying a logic "0" (ground) to the Reset pin will reset all registers to "0". The Reset pin is provided with an on-chip pull-up resistor.

CLOCK (input): pin 22 (AY-3-8910)
pin 15 (AY-3-8912)

This TTL-compatible input supplies the timing reference for the Tone, Noise and Envelope Generators.

BDIR, BC2, BC1 (inputs): pins 27,28,29 (AY-3-8910)
pins 18,19,20 (AY-3-8912)

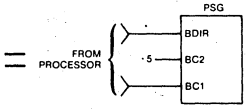
Bus DIRection, Bus Control 2,1

These bus control signals are generated directly by GI's CP1600 series of microprocessors to control all external and internal bus operations in the PSG. When using a processor other than the CP1600, these signals can be provided either by comparable bus signals or by simulating the signals on I/O lines of the processor. The PSG decodes these signals as illustrated in the following:

BDIR	BC2	BC1	CP1600 FUNCTION	PSG FUNCTION
0	0	0	NACT	INACTIVE. See 010 (IAB) below.
0	0	1	ADAR	LATCH ADDRESS. See 111 (INTAK) below.
0	1	0	IAB	INACTIVE. The PSG/CPU bus is inactive. DA7--DA0 are in a high impedance state.
0	1	1	DTB	READ FROM PSG. This signal causes the contents of the register which is currently addressed to appear on the PSG/CPU bus. DA7--DA0 are in the output mode.
1	0	0	BAR	LATCH ADDRESS. See 111 (INTAK) below.
1	0	1	DW	INACTIVE. See 010 (IAB) above.
1	1	0	DWS	WRITE TO PSG. This signal indicates that the bus contains register data which should be latched into the currently addressed register. DA7--DA0 are in the input mode.
1	1	1	INTAK	LATCH ADDRESS. This signal indicates that the bus contains a register address which should be latched in the PSG. DA7--DA0 are in the input mode.

While interfacing to a processor other than the CP1600 would simply require simulating the above decoding, the redundancies in the PSG functions vs. bus control signals can be used to advantage in that only four of the eight possible decoded bus functions are required by the PSG. This could simplify the programming of the bus control signals to the following, which would only require that the processor generate two bus control signals (BDIR and BC1, with BC2 tied to +5V):

BDIR	BC2	BC1	PSG FUNCTION
0	1	0	INACTIVE.
0	1	1	READ FROM PSG.
1	1	0	WRITE TO PSG.
1	1	1	LATCH ADDRESS.



ANALOG CHANNEL A, B, C (outputs): pins 4, 3, 38 (AY-3-8910)
pins 5, 4, 1 (AY-3-8912)

Each of these signals is the output of its corresponding D/A Converter, and provides an up to 1V peak-peak signal representing the complex sound waveshape generated by the PSG.

IOA7--IOA0 (input/output): pins 14--21 (AY-3-8910)
pins, 7--14 (AY-3-8912)

IOB7--IOB0 (input/output): pins 6--13 (AY-3-8910)
(not provided on AY-3-8912)

Input/Output A7--A0, B7--B0

Each of these two parallel input/output ports provides 8 bits of parallel data to/from the PSG/CPU bus from/to any external devices connected to the IOA or IOB pins. Each pin is provided with an on-chip pull-up resistor, so that when in the "input" mode, all pins will read normally high. Therefore, the recommended method for scanning external switches, for example, would be to ground the input bit.

TEST 1: pin 39 (AY-3-8910)
pin 2 (AY-3-8912)

TEST 2: pin 26 (AY-3-8910)
(not connected on AY-3-8912)

These pins are for GI test purposes only and should be left open—do not use as tie-points.

V_{CC}: pin 40 (AY-3-8910)
pin 3 (AY-3-8912)

Nominal +5Volt power supply to the PSG.

V_{SS}: pin 1 (AY-3-8910)
pin 6 (AY-3-8912)

Ground reference for the PSG.

ARCHITECTURE

The AY-3-8910/8912 is a register oriented Programmable Sound Generator (PSG). Communication between the processor and the PSG is based on the concept of memory-mapped I/O. Control commands are issued to the PSG by writing to 16 memory-mapped registers. Each of the 16 registers within the PSG is also readable so that the microprocessor can determine, as necessary, present states or stored data values.

All functions of the PSG are controlled through its 16 registers which once programmed, generate and sustain the sounds, thus freeing the system processor for other tasks.

REGISTER ARRAY

The principal element of the PSG is the array of 16 read/write control registers. These 16 registers look to the CPU as a block of memory and as such occupy a 16 word block out of 1,024 possible addresses. The 10 address bits (8 bits on the common data/address bus, and 2 separate address bits A8 and $\overline{A9}$) are decoded as follows:

* $\overline{A9}$	A8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	1	0	0	0	0	0	0	0	0
THRU									
0	1	0	0	0	0	1	1	1	1
HIGH ORDER (Chip Select)						LOW ORDER (Register #)			

* $\overline{A9}$ is not provided on the AY-3-8912.

The four low order address bits select one of the 16 registers (R0--$R17_8$). The six high order address bits function as "chip selects" to control the tri-state bidirectional buffers (when the high order address bits are "incorrect", the bidirectional buffers are forced to a high impedance state). High order address bits $\overline{A9}$ A8 are fixed in the PSG design to recognize a 01 code; high order address bits DA7--DA4 may be mask-programmed to any 4-bit code by a special order factory mask modification. Unless otherwise specified, address bits DA7--DA4 are programmed to recognize only a 0000 code. A valid high order address latches the register address (the low order 4 bits) in the Register Address Latch/Decoder block. A latched address will remain valid until the receipt of a new address, enabling multiple reads and writes of the same register contents without the need for redundant re-addressing.

Conditioning of the Register Address Latch/Decoder and the Bidirectional Buffers to recognize the bus function required (inactive, latch address, write data, or read data) is accomplished by the Bus Control Decode block.

SOUND GENERATING BLOCKS

The basic blocks in the PSG which produce the programmed sounds include:

Tone Generators	produce the basic square wave tone frequencies for each channel (A,B,C)
Noise Generator	produces a frequency modulated pseudo random pulse width square wave output.
Mixers	combine the outputs of the Tone Generators and the Noise Generator. One for each channel (A,B,C).
Amplitude Control	provides the D/A Converters with either a fixed or variable amplitude pattern. The fixed amplitude is under direct CPU control; the variable amplitude is accomplished by using the output of the Envelope Generator.
Envelope Generator	produces an envelope pattern which can be used to amplitude modulate the output of each Mixer.
D/A Converters	the three D/A Converters each produce up to a 16 level output signal as determined by the Amplitude Control.

I/O PORTS

Two additional blocks are shown in the PSG Block Diagram which have nothing directly to do with the production of sound—these are the two I/O Ports (A and B). Since virtually all uses of microprocessor-based sound would require interfacing between the outside world and the processor, this facility has been included in the PSG. Data to/from the CPU bus may be read/written to either of two 8-bit I/O Ports without affecting any other function of the PSG. The I/O Ports are TTL-compatible and are provided with internal pull-ups on each pin. Both Ports are available on the AY-3-8910; only I/O Port A is available on the AY-3-8912.

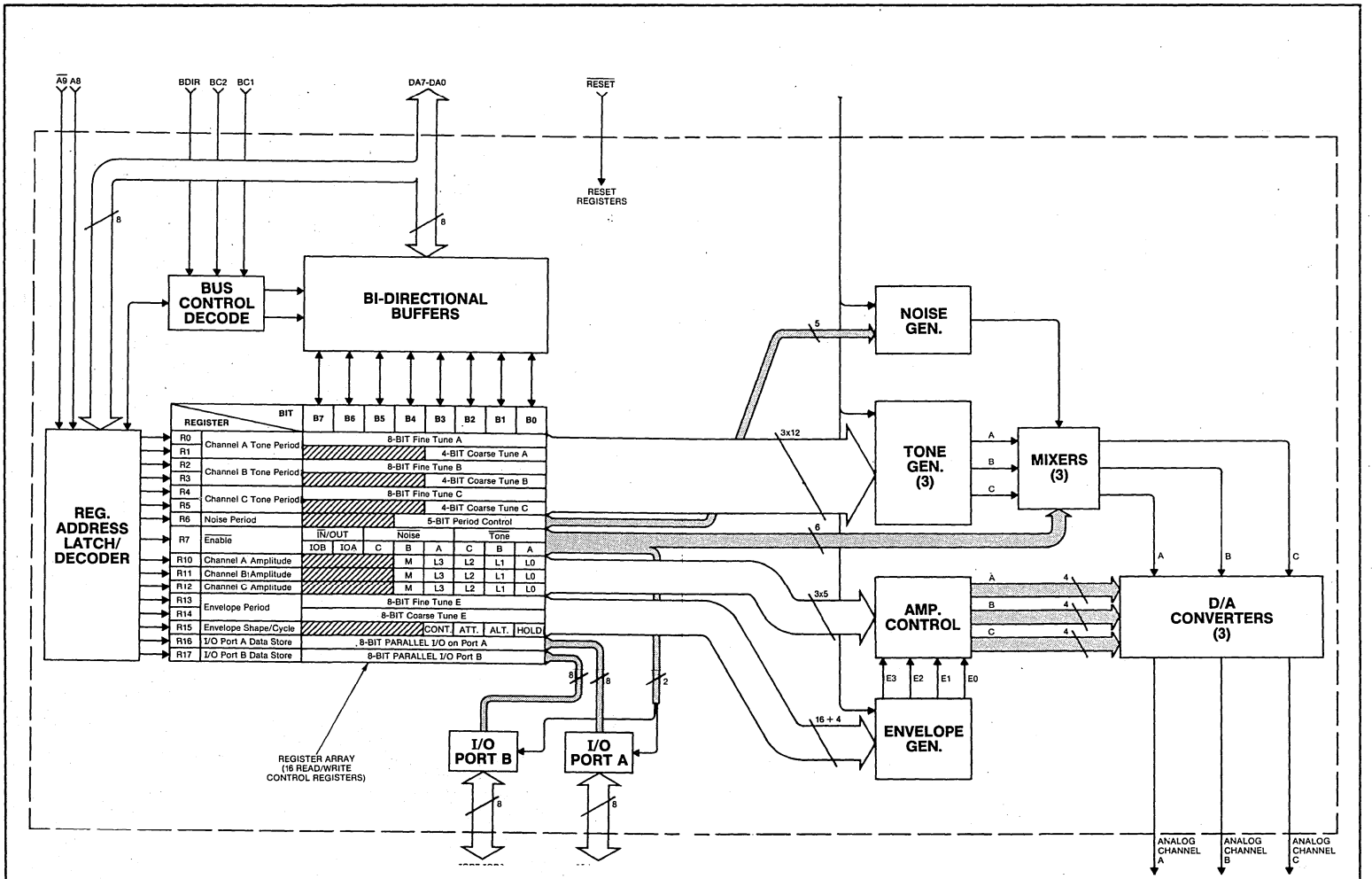


Fig. 2 PSG BLOCK DIAGRAM

OPERATION

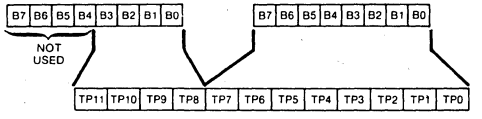
Since all functions of the PSG are controlled by the host processor via a series of register loads, a detailed description of the PSG operation can best be accomplished by relating each PSG function to the control of its corresponding register. The function of creating or programming a specific sound or sound effect logically follows the control sequence listed:

Operation	Registers	Function
Tone Generator Control	R0--R5	Program tone periods.
Noise Generator Control	R6	Program noise period.
Mixer Control	R7	Enable tone and/or noise on selected channels.
Amplitude Control	R10--R12	Select "fixed" or "envelope-variable" amplitudes.
Envelope Generator Control	R13--R15	Program envelope period and select envelope pattern

Tone Generator Control
(Registers R0, R1, R2, R3, R4, R5)

The frequency of each square wave generated by the three Tone Generators (one each for Channels A, B, and C) is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 12-bit Tone Period value. Each 12-bit value is obtained in the PSG by combining the contents of the relative Coarse and Fine Tune registers, as illustrated in the following:

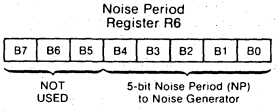
Coarse Tune Register	Channel	Fine Tune Register
R1	A	R0
R3	B	R2
R5	C	R4



12-bit Tone Period (TP) to Tone Generator

Noise Generator Control
(Register R6)

The frequency of the noise source is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 5-bit Noise Period value. This 5-bit value consists of the lower 5 bits (B4--B0) of register R6, as illustrated in the following:



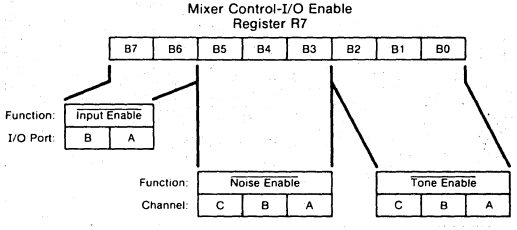
Mixer Control-I/O Enable
(Register R7)

Register 7 is a multi-function $\overline{\text{Enable}}$ register which controls the three Noise/Tone Mixers and the two general purpose I/O Ports.

The Mixers, as previously described, combine the noise and tone frequencies for each of the three channels. The determination of combining neither/either/both noise and tone frequencies on each channel is made by the state of bits B5--B0 of R7.

The direction (input or output) of the two general purpose I/O Ports (IOA and IOB) is determined by the state of bits B7 and B6 of R7.

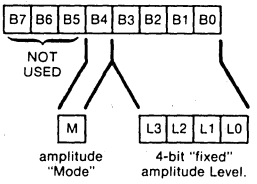
These functions are illustrated in the following:



Amplitude Control
(Registers R10, R11, R12)

The amplitudes of the signals generated by each of the three D/A Converters (one each for Channels A, B, and C) is determined by the contents of the lower 5 bits (B4--B0) of registers R10, R11, and R12 as illustrated in the following:

Amplitude Control Register #	Channel
R10	A
R11	B
R12	C

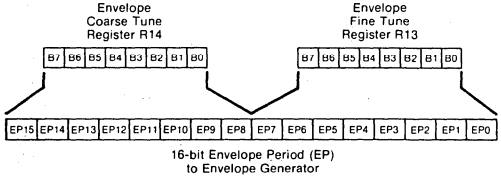


Envelope Generator Control
(Registers R13, R14, R15)

To accomplish the generation of fairly complex envelope patterns, two independent methods of control are provided in the PSG: first, it is possible to vary the frequency of the envelope using registers R13 and R14; and second, the relative shape and cycle pattern of the envelope can be varied using register R15. The following paragraphs explain the details of the envelope control functions, describing first the envelope period control and then the envelope shape/cycle control.

ENVELOPE PERIOD CONTROL (Registers R13, R14)

The frequency of the envelope is obtained in the PSG by first counting down the input clock by 256, then by further counting down the result by the programmed 16-bit Envelope Period value. This 16-bit value is obtained in the PSG by combining the contents of the Envelope Coarse and Fine Tune registers, as illustrated in the following:

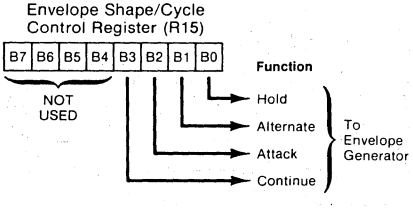


16-bit Envelope Period (EP) to Envelope Generator

ENVELOPE SHAPE/CYCLE CONTROL (Register R15)

The Envelope Generator further counts down the envelope frequency by 16, producing a 16-state per cycle envelope pattern as defined by its 4-bit counter output, E3 E2 E1 E0. The particular shape and cycle pattern of any desired envelope is accomplished by controlling the count pattern (count up/count down) of the 4-bit counter and by defining a single-cycle or repeat-cycle pattern.

This envelope shape/cycle control is contained in the lower 4 bits (B3--B0) of register R15. Each of these 4 bits controls a function in the envelope generator, as illustrated in the following:



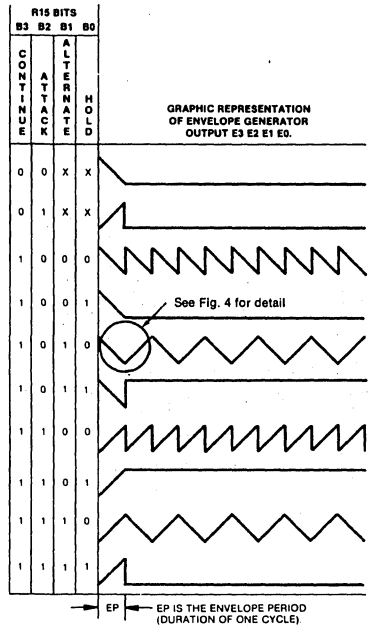


Fig. 3 ENVELOPE SHAPE/CYCLE OPERATION

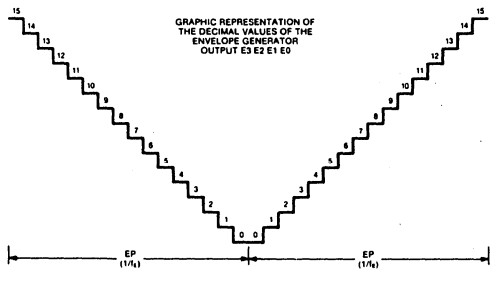


Fig. 4 DETAIL OF TWO CYCLES OF Fig. 3 (ref. waveform "1010" in Fig. 3)

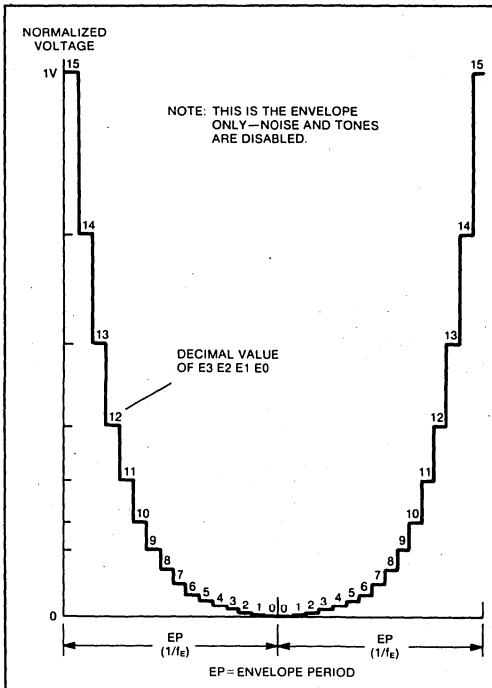


Fig. 5 D/A CONVERTER OUTPUT

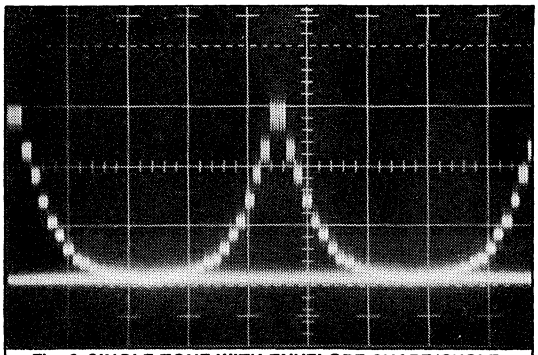


Fig. 6 SINGLE TONE WITH ENVELOPE SHAPE/CYCLE PATTERN 1010

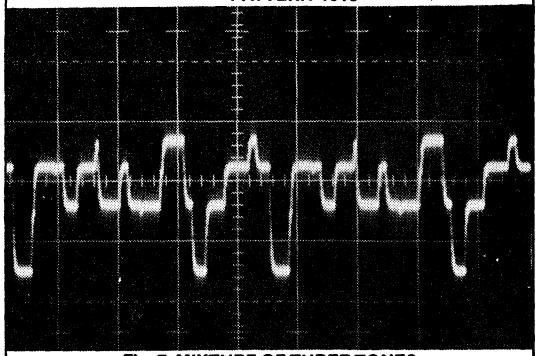


Fig. 7 MIXTURE OF THREE TONES WITH FIXED AMPLITUDES

I/O Port Data Store
(Registers R16, R17)

Registers R16 and R17 function as intermediate data storage registers between the PSG/CPU data bus (DA0--DA7) and the two I/O ports (IOA7--IOA0 and IOB7--IOB0). Both ports are available in the AY-3-8910; only I/O Port A is available in the AY-3-8912. Using registers R16 and R17 for the transfer of I/O data has no effect at all on sound generation.

D/A Converter Operation

Since the primary use of the PSG is to produce sound for the highly imperfect amplitude detection mechanism of the human ear, the D/A conversion is performed in logarithmic steps with a normalized voltage range of from 0 to 1 Volt. The specific amplitude control of each of the three D/A Converters is accomplished by the three sets of 4-bit outputs of the Amplitude Control block, while the Mixer outputs provide the base signal frequency (Noise and/or Tone).

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +40°C
V_{CC} and all other input/output voltages with respect to V_{SS} ..... −0.3V to +8.0V

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5V ±5%
V_{SS} = GND
Operating Temperature = 0°C to +40°C

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
All Inputs						
Logic "0"	V_{IL}	0	—	0.6	V	
Logic "1"	V_{IH}	2.4	—	V_{CC}	V	
All Outputs (except Analog Channel Outputs)						
Logic "0"	V_{OL}	0	—	0.5	V	I_{OL} = 1.6mA, 20pF
Logic "1"	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 100μA, 20pF
Analog Channel Outputs	V_O	0	—	60	dB	Test circuit: Fig. 8
Power Supply Current	I_{CC}	—	45	75	mA	
AC CHARACTERISTICS						
Clock Input						
Frequency	f_C	1.0	—	2.0	MHz	Fig. 9
Rise Time	t_r	—	—	50	ns	
Fall Time	t_f	—	—	50	ns	
Duty Cycle	—	25	50	75	%	
Bus Signals (BDIR, BC2, BC1)						
Associative Delay Time	t_{BD}	—	—	50	ns	
Reset						
Reset Pulse Width	t_{RW}	500	—	—	ns	Fig. 10
Reset to Bus Control Delay Time	t_{RB}	100	—	—	ns	
A9, A8, DA7--DA0 (Address Mode)						
Address Setup Time	t_{AS}	400	—	—	ns	Fig. 11
Address Hold Time	t_{AH}	100	—	—	ns	
DA7--DA0 (Write Mode)						
Write Data Pulse Width	t_{DW}	500	—	10,000	ns	Fig. 12
Write Data Setup Time	t_{DS}	50	—	—	ns	
Write Data Hold Time	t_{DH}	100	—	—	ns	
DA7--DA0 (Read Mode)						
Read Data Access Time	t_{DA}	—	250	500	ns	Fig. 13
DA7--DA0 (Inactive Mode)						
Tristate Delay Time	t_{TS}	—	100	200	ns	

**Typical values are at +25°C and nominal voltages.

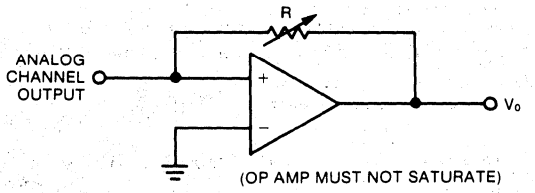


Fig. 8 ANALOG CHANNEL OUTPUT TEST CIRCUIT

TIMING DIAGRAMS

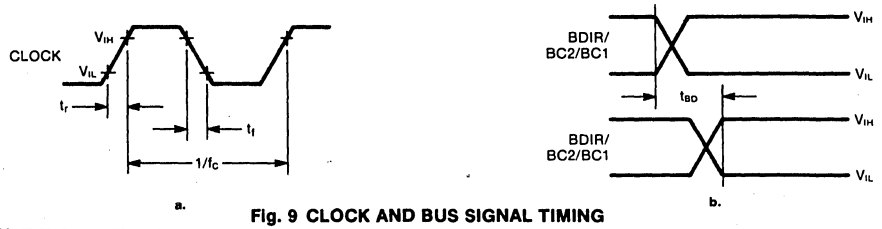


Fig. 9 CLOCK AND BUS SIGNAL TIMING

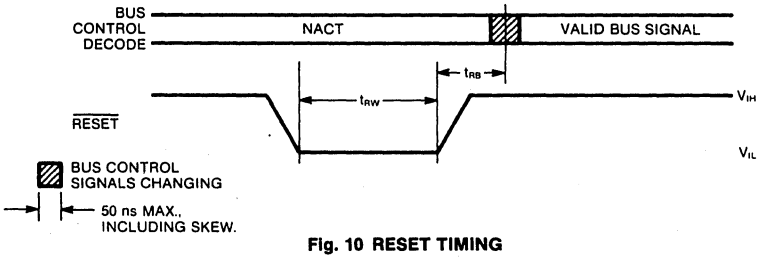
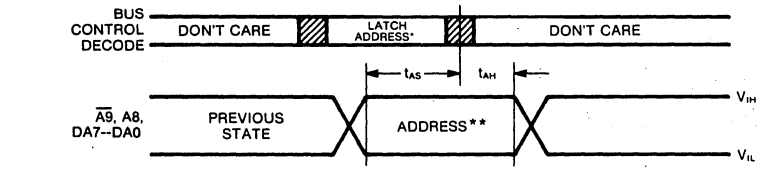


Fig. 10 RESET TIMING

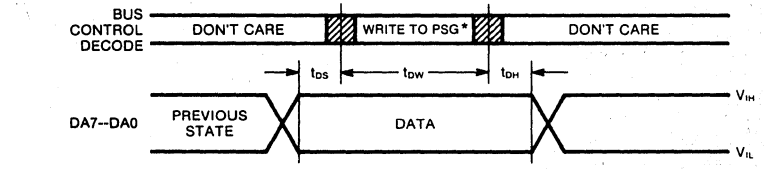


**REFER TO PARAGRAPH 2.1.1 FOR A DESCRIPTION OF "VALID" PSG ADDRESSING.

*ANY COMBINATION OF BDIR, BC2, BC1 WHICH DECODE "LATCH ADDRESS":

	BDIR	BC2	BC1
	0	0	1
or	1	0	0
or	1	1	1

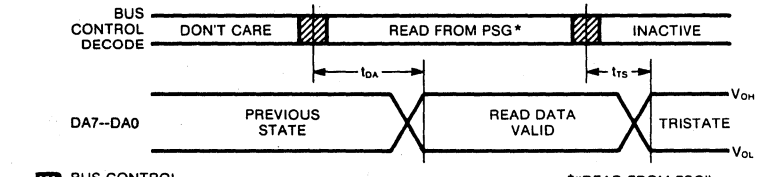
Fig. 11 LATCH ADDRESS TIMING



*"WRITE TO PSG":

BDIR	BC2	BC1
1	1	0

Fig. 12 WRITE DATA TIMING



*"READ FROM PSG":

BDIR	BC2	BC1
0	1	1

Fig. 13 READ DATA TIMING

Color Processor Chip

FEATURES

- Operation from 7.15909MHz crystal
- Five-line digital selection for 1 of 16 colors, blanking, Sync and color burst
- 3.579545MHz buffered output

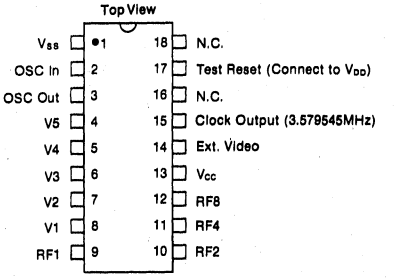
DESCRIPTION

The required color to be displayed for each 280 nsec PIXEL is decoded on a four line binary coded input. This selects one of sixteen possible colors. An external resistor network completes the D to A function as shown in the schematic Fig. 1 of this document. The waveform plus table illustrates the use of the five inputs to produce composite sync, color burst, line blanking, frame blanking and video.

The external video input pin provides the ability to superimpose white high resolution (140 nsec wide) video information over the picture (color image).

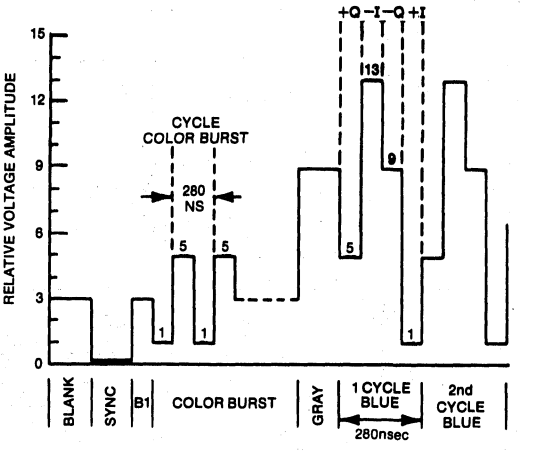
PIN CONFIGURATIONS

18 LEAD DUAL IN LINE



INPUT CODE ASSIGNMENT					TIME SLOT RELATIVE VOLTAGE AMPLITUDES				COLOR OUTPUT DESCRIPTION	
V5	V4	V3	V2	V1	+Q	−I	−Q	+I		
0	0	0	0	0	3	3	3	3	Black	
0	0	0	0	1	5	13	9	1	Blue	
0	0	0	1	0	8	0	4	12	Red	
0	0	0	1	1	4	4	12	12	Tan	
0	0	1	0	0	3	8	11	6	Grass Green	Group A
0	0	1	0	1	3	11	13	5	Green	
0	0	1	1	0	9	11	15	13	Yellow	
0	0	1	1	1	13	13	13	13	White	
0	1	0	0	0	9	9	9	9	Gray	
0	1	0	0	1	8	13	12	7	Cyan	
0	1	0	1	0	9	4	9	14	Orange	
0	1	0	1	1	4	4	8	8	Brown	
0	1	1	0	0	13	5	3	11	Magenta	Group B
0	1	1	0	1	12	12	6	6	Light Blue	
0	1	1	1	0	5	9	13	9	Yellow-Green	
0	1	1	1	1	10	5	2	7	Purple	
1	X	X	0	0	3	3	3	3	Blanking	
1	X	X	1	0	1	1	5	5	Color Burst	
1	X	X	0	1	0	0	0	0	Sync	
1	1	1	1	1	0	15	0	15	Test	

X = Don't Care



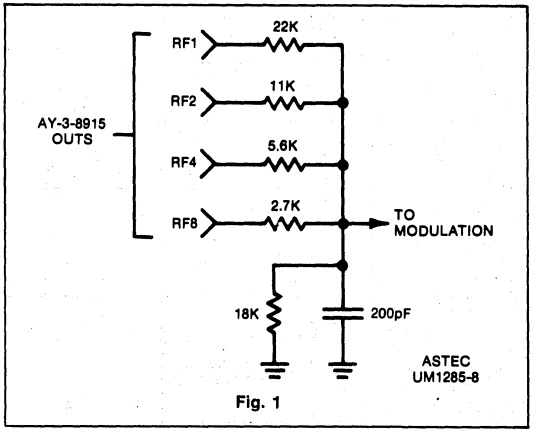


Fig. 1

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Temperature Under Bias ..... 0°C to +40°C
Storage Temperature ..... −55°C to +150°C
All Input or Output Voltages with Respect to V_{SS} ..... −0.2V to +9.0V
V_{CC} with respect to V_{SS} ..... −0.2V to +9.0V

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

T_A = 0°C to +40°C
V_{CC} = +4.85V − + 5.15V
V_{SS} = 0.0V

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Oscillator Freq. In.	—	—	—	—	MHz	7.15909MHz crystal Trimmed by external capacitor
3.579545MHz Clock Output						
Output Logic Low	V_{OL}	0	—	0.5	volts	
Output Logic High	V_{OH}	2.4	—	V_{CC}	volts	
Logic Inputs V1, V2, V3, V4, V5, EXT. VIDEO						
Input Logic Low	V_{IL}	0	—	0.7	volts	
Input Logic High	V_{IH}	2.4	—	V_{CC}	volts	
Outputs RF1, RF2, RF4, RF8						
Output ON	I	5.0	—	—	mA	V_{out} = +0.5V
Output OFF	I	—	—	10	μA	V_{out} = +2.4V
Supply Current						
V_{DD}	I_{CC}	—	—	80	mA	V_{CC} = 5.25V @ 40°C

GENERAL INFORMATION

INTRODUCTION

Teletext and Viewdata are the generic names for two basically similar systems for displaying pages of information on a TV screen.

Teletext (otherwise known as Ceefax, Oracle, Videotext)

In the Teletext system the data is coded onto normally unused lines of a television transmission. It has the following features:

(a) Being a broadcast system the data flow can be one way only. 'Pages' of data are sent continuously on a rotating basis and the decoder will grab the required page as it passes.

(b) The number of 'spare' TV lines is limited so for a reasonable access time the data bank is restricted to 100-800 pages per channel.

(c) Being broadcast the data may be 'live', it may update very rapidly and everyone receives the data simultaneously. Subtities and newsflashes are good examples of live data.

Viewdata (otherwise known as Prestel, Bildschirmtext).

In the Viewdata system the decoder is connected to the users telephone line and uses the public telephone network in order to transmit information to and from a computerized data bank. It has the following features.

(a) There is a direct and individual connection to the user and the data flow may be two way. The user thus requests the page he wants directly.

(b) The data bank may be as large as desired, there are no system limitations.

(c) Being an individual connection the service may be a personal one and the data content may reflect this, and may indeed be restricted to a selected group of users.

TELEVIEW

Televiewis a General Instruments' 3 chip integrated circuit kit which forms the basis of an inexpensive, comprehensive Viewdata and Teletext system.

Other optional circuits provide additional features such a Infra Red Remote Control, Viewdata modem, Autodialler and Terminal identifier, and various TV Digital Tuning Systems.

The kit provides switchable Viewdata or Teletext operation with automatic selection of "on" and "off hours" operation. Provision has been made for addressing up to 8 pages of memory thus giving great flexibility and economy of operation.

The system is organized around parallel Data and Address highways, this allows easy expansion of the system and the connection of other equipment such as Home Computers and Disc Memories.

A single chip microcomputer is used to control the system and to interface to the user. The microcomputer allows easy alteration of the system features enabling manufacturers to have personalized systems if desired.

As far as possible adjustable and critical components have been eliminated and the circuitry has been designed to facilitate the use of single sided printed circuit boards.

TELEVIEW FEATURES

- Switchable Viewdata — Teletext, 625 line system with 24 rows of 40 characters
- Up to 8 page stores
- Microcomputer controlled, gives system flexibility
- Data bus organization for easy system expansion
- On/Off hours operation
- Don't care digit feature in Teletext
- Half page expansion feature
- Black/White output for Monochrome TV and Printers
- Special Graphics feature for high resolution
- Boxed clock capability in Teletext
- Selectable character rounding
- Simple printed board layout
- 4 x 4, ASCII, REMOTE Keyboard options
- Low power consumption typically +12V at +12V at 10mA) + 5V at 400mA) for a single page store − 5V at 100mA)

SYSTEM DESCRIPTION

The system consists of four basic blocks.

(a) Data Acquisition
This block acquires data from either the TV IF (Teletext) or the telephone line (Viewdata) and after verification passes it to the Page Store.

(b) Page Store
The page store, of which there may be up to 8, is the repository for the information to be displayed. It is written into by the Data Acquisition block and read by the Video Generator.

(c) Video Generator
The Video Generator reads the information in the store, decodes it into a dot pattern and outputs video signals to TV tube.

The information to be displayed is chosen by the user via the Controller.

(d) Controller
The Controller (which is a single chip microcomputer) is primarily the interface between the operator and the system.

Fig. 1 shows a typical complete system broken up into the blocks described.

An important feature to note is the way that each block in the system communicates to the others by means of a 10 bit Address highway and an 8 bit Data Highway. The interchange of data is controlled by the signals TS1 and TS2 which are provided by the Video Generator.

See TELEVIEW, CPSS 70005 SYSTEM DESCRIPTION for full description of the system.

OPERATING TELEVIEW

Teleview provides a number of features over and above those normally provided for Teletext and Viewdata systems.

Most of these features concern the Keyboard operations, which have been designed for ease of use with a minimum number of keys and no lock up situations.

Key Functions—The best way to describe the features is with reference to a typical keyboard (See Fig. 12).

Picture Text—Repeated operation of this key switches the system between Picture and Text modes.

Mix—Repeated operation of this key switches the system between Mix and Normal modes. In the Mix Mode Captions, subtitles and Newsflashes are inset into the picture.

Half Page—Repeated operation of this key cycles the system from Normal to Upper Half Expanded to lower Half Expanded back to Normal. Operation of the P key restores Normal Mode.

Store Select—Operating Store Select and Digit 1-8 selects a new store for display (assuming that more than one is provided).

Box Clock—Operation of this key when in Picture Mode causes the Clock to be Boxed into the picture in Double Height Characters. A second operation cancels the command.

Hold—Operation of this key will hold displayed the current one of a set of rotating pages. If more than one store is provided the remainder of the set will be automatically stored in the unselected stores.

Reveal—Repeated operation of this key Reveals and Conceals concealed information.

Update (Clear)—Operation of this key removes the information from the display until the page is updated. A second operation restores the display.

Update (Clear)—Operation of P or Store Select also restores the display. (In Viewdata mode this keys acts as a Clear.)

Roll Headers—Operation of this key starts the Teletext headers rolling.

Cursor OFF Operation of these keys switch the cursor
Cursor ON ON and OFF in Viewdata mode.

Rounding OFF—Operation of this key removes the character rounding and inhibits the flashing of characters. Normally used when printing. Reception of a new page or operation of Cursor ON or OFF restores rounding.

P (*) Page No. Key. Operation of this key primes the system to accept a 3 digit page number. (* in Viewdata mode.)

T (#) Time Key. Operation of this key primes the system to accept a 4 digit time code. (// in Viewdata mode.)

Initialization—At Power Up the page stres are cleared and up to 10 characters of text are inserted in the middle of the page.

For PIC 1650-513 VIEWDATA in White is displayed and Text mode is selected.

For PIC 1650-514 TELEVIEW in White is displayed and Picture mode is selected.

For PIC 1650(IR)-516 TELEVIEW in Yellow is displayed and Picture mode is selected.

For PIC 1650 (ASCII)-516 TELEVIEW in Cyan is displayed and picture mode is selected.

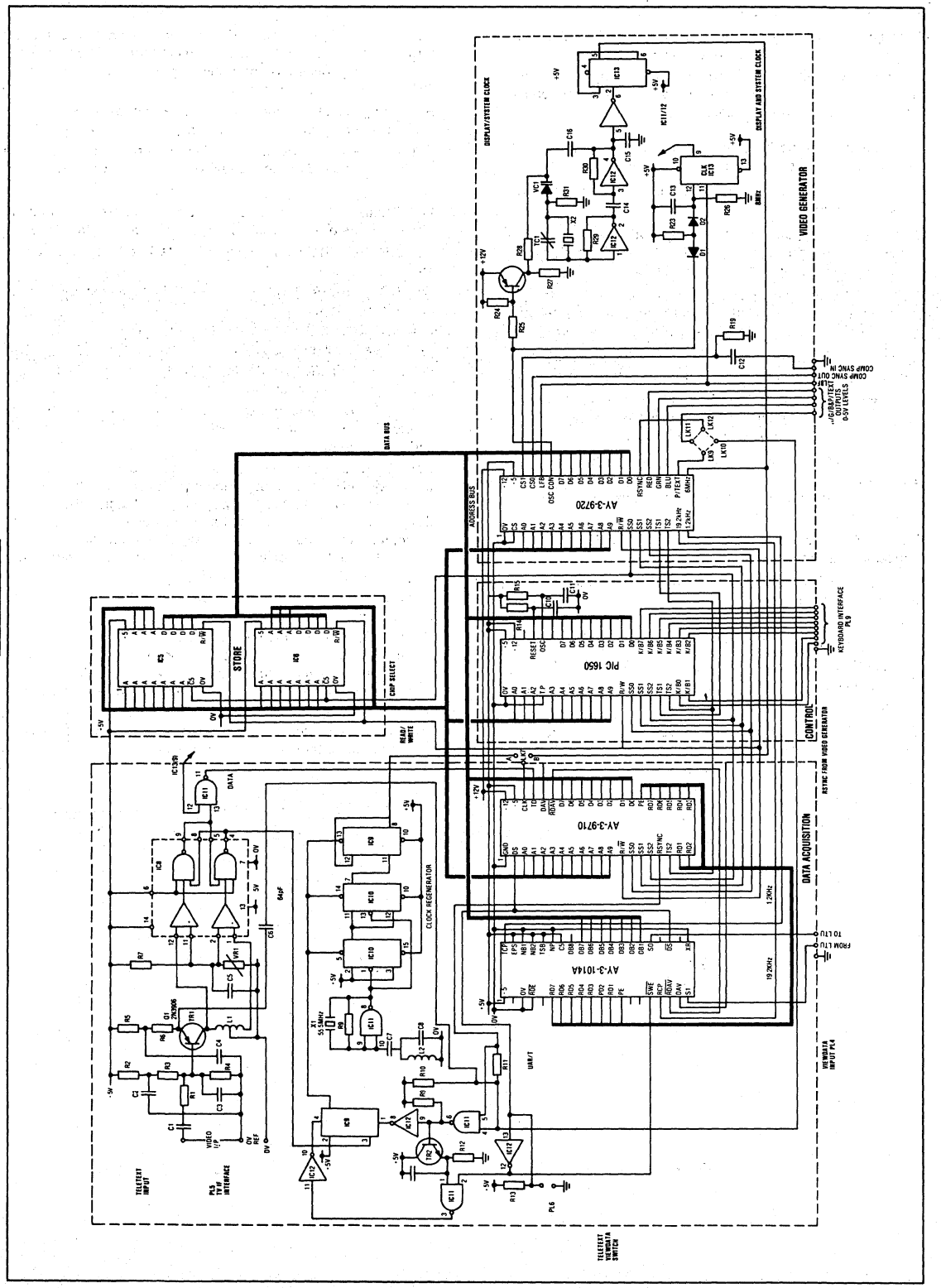
Page No.X00 is selected to be stored in store 7 (so that the Teletext index is immediately available). (Note; alternative initialization can be provided).

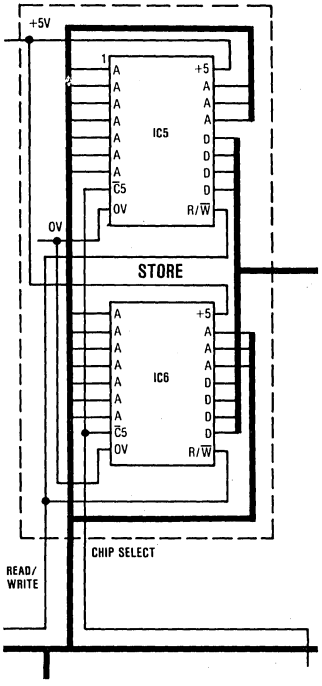
Page Selection—In Teletext mode pages are selected by pressing the P key and entering a page number. Televiewhas the ability to accept don't care digits (-) as well as normal digits (0-9). Operation of the Update Key (which has no use at this time) enters the (-) so, if for instance, 1-0 were keyed every tenth page starting at page 100 would be displayed as soon as it was transmitted (approximately at 2 sec. intervals).

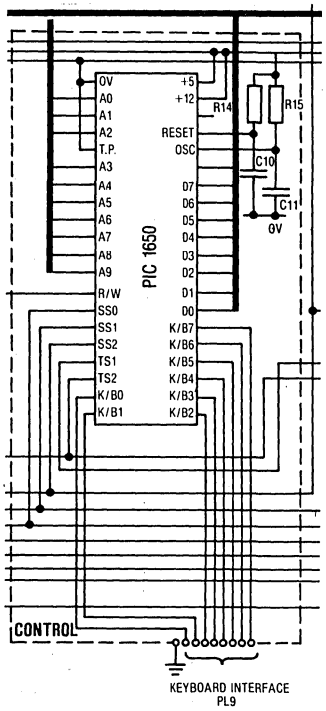
Operation of the time code Key T terminated the page no enty and fills any unentered page digits as blanks.

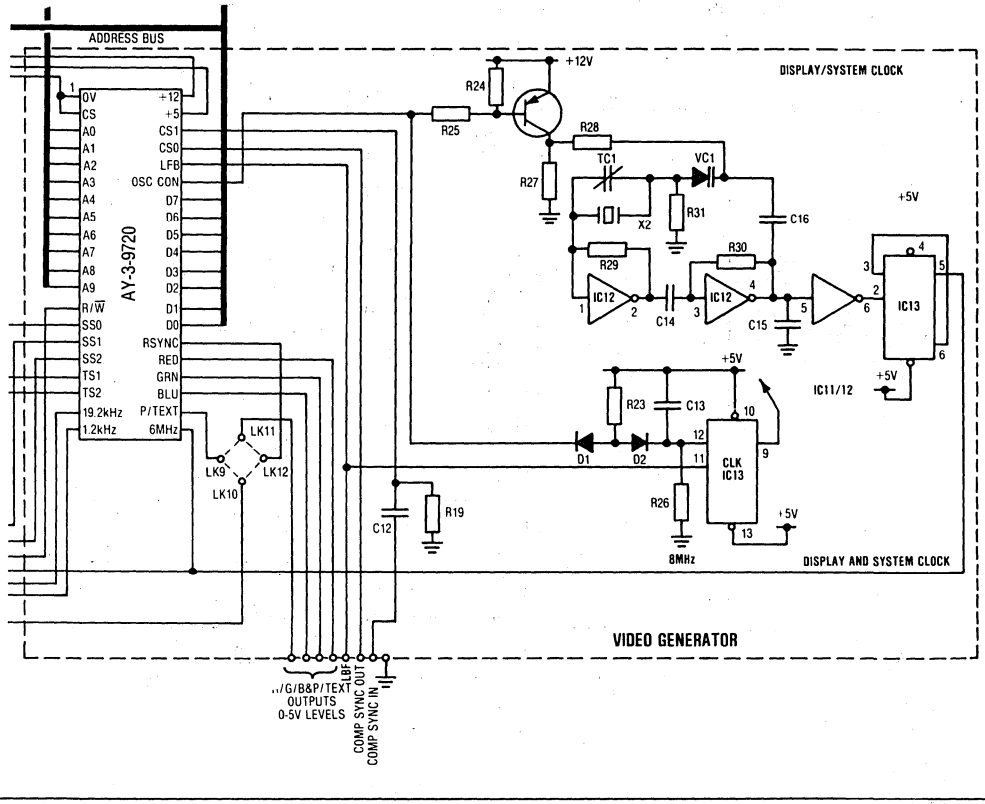
The rolling of pages described above can be stopped by pressing Store Select or Hold. If the Hold key is pressed and more than one store is provided subsequent pages will automatically be stored. The P key will also stop rolling but the page may be erased.

Page selection may also take place in the Picture mode in which case the page header will be boxed (in double height characters) for 5 seconds after each digit is pressed.

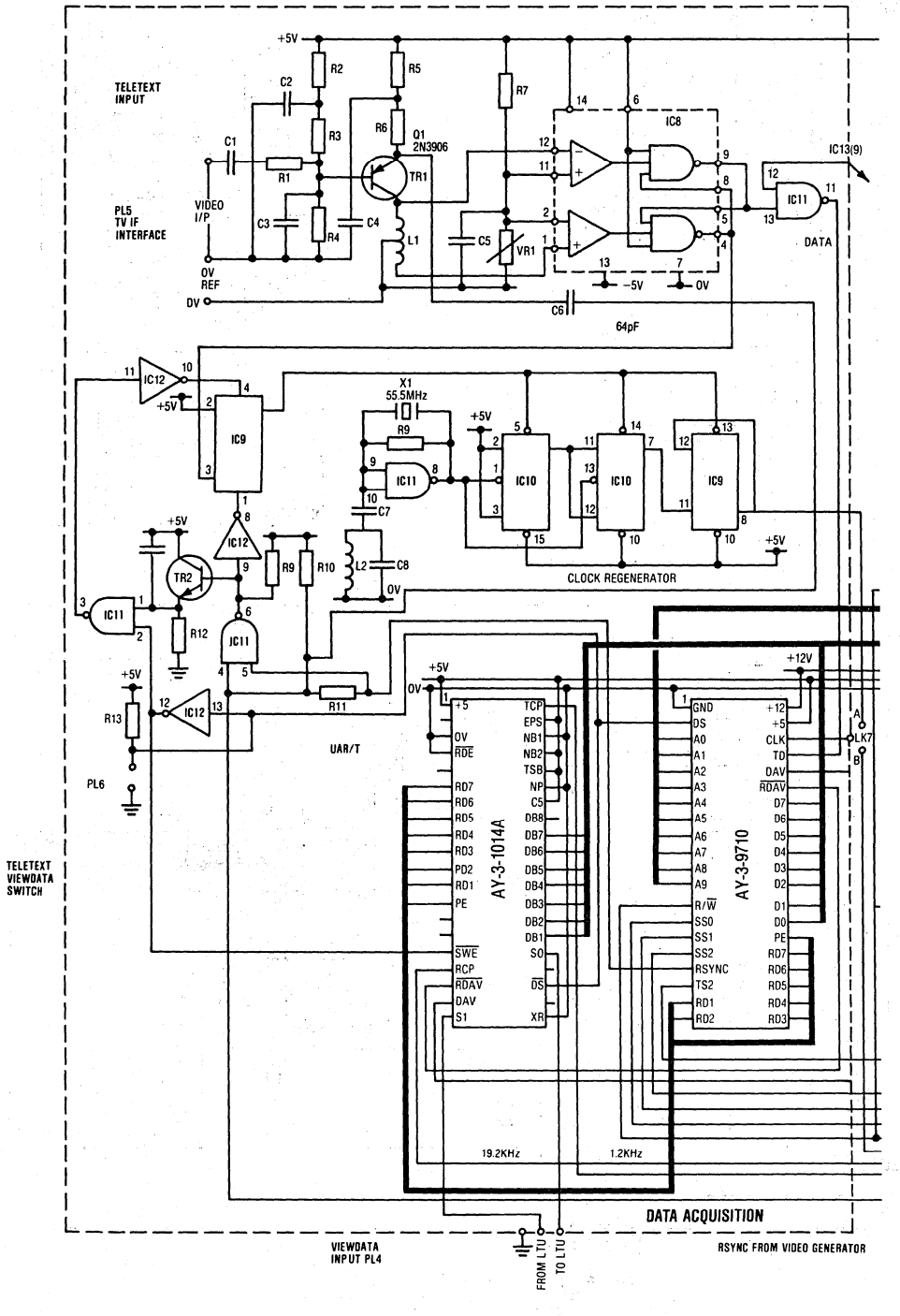

DISPLAY/SYSTEM CLOCK
DISPLAY AND SYSTEM CLOCK
VIDEO GENERATOR
DATA BUS
ADDRESS BUS
AY-3-9720
PIC 1650
KEYBOARD INTERFACE PL9
STORE
CHIP SELECT
READ/WRITE
CONTROL
AY-3-9710
DATA ACQUISITION
RSYNC FROM VIDEO GENERATOR
AY-3-1014A
CLOCK REGENERATOR
UART
FROM LTU
TO LTU
VIEWDATA INPUT P14
TELETEXT INPUT
PL8 VIDEO INTERFACE
PL6
TELETEXT VIEWDATA SWITCH
VIDEO INPUT
OV REF
2N3906
55.5MHz
64pF
1.2KHz
19.2KHz
6MHz







PERSONAL TERMINAL


TELETEXT INPUT
PL5 TV IF INTERFACE
VIDEO I/P
0V REF
0V
+5V
R1
R2
R3
R4
R5
R6
R7
C1
C2
C3
C4
C5
C6
64pF
Q1 2N3906
TR1
L1
VR1
IC8
IC11
IC13(9)
DATA
-5V
0V
IC12
IC9
IC10
X1 55.5MHz
R9
C7
C8
L2
R10
TR2
CLOCK REGENERATOR
IC11
R12
R11
R13
PL6
UART
TELETEXT VIEWDATA SWITCH
AY-3-1014A
AY-3-9710
+12V
19.2KHz
1.2KHz
DATA ACQUISITION
VIEWDATA INPUT PL4
FROM LTU
TO LTU
RSYNC FROM VIDEO GENERATOR
CLK7

Teleview Controller

FEATURES

- Microcomputer Based Circuit
- PIC 1650A-513-Accepts full ASCII Keyboard input for Viewdata reception
- PIC 1650A-514-Accepts basic 4 x 4 Keyboard matrix for either Viewdata or Teletext reception
- PIC 1650A-516-Accepts full ASCII Keyboard input or Remote Control receiver (AY-3-8475) interface with up to 24 keys.

DESCRIPTION

The PIC 1650A-513, 514 and 516 are special programmed versions of the standard General Instrument PIC 1650A microcomputer circuit. The PIC 1650A contains a central processing unit, RAM registers, Program ROM and a clock generator on a single chip. The program is contained within the ROM which consists of powerful 12-bit words placed in permanent memory. The I/O lines have been dedicated through the program to contain a 10 bit address port and an 8 bit data port, for the Teleview control functions. An 8 bit input port for Keyboard input information, two time slot inputs, and three output control bits for RAM chip selection to store up to eight pages are also provided.

The three current preprogrammed PIC 1650A Teleview Control chips are as follows:

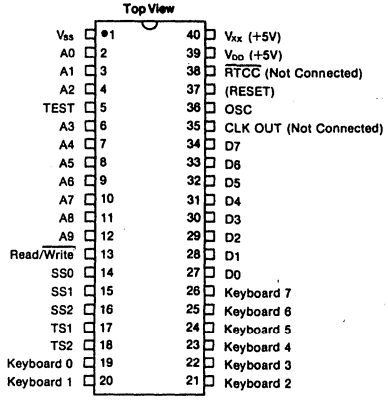
PIC 1650A-513- Accepts full ASCII Keyboard input for Viewdata reception. Powers up to Viewdata Text Mode.

PIC 1650A-514- Accepts basic 4 x 4 Keyboard matrix for either Viewdata or Teletext. Powers up to Picture Mode.

PIC 1650A-516- Accepts full ASCII Keyboard or Remote Control receiver (AY-3-8475) interface with up to 24 keys. Powers up to Picture Mode.

PIN CONFIGURATIONS

40 LEAD DUAL IN LINE



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... −0.3V to +15V

Storage temperature ..... −55°C to +150°C

Standard Conditions (unless otherwise stated)

Supply Voltage = V_{SS} = 0v (Substrate voltage)

V_{DD} = +5 ± 5%

V_{XX} ± +5 ± 5%

Temperature range = 0°C to +70°C

* Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Characteristic	Min	Max	Units	Conditions
Address Inputs				
High level	2.4	V_{DD}	V	
Low level	−0.2	0.8	V	
Data Outputs				
High level	2.4	V_{DD}	V	I_{OH} = −100μA provided
Low level	0	0.45	V	I_{OL} = 1.0mA, V_{XX} = 4.5V
Keyboard Inputs				
High level	2.4	V_{DD}	V	
Low level	−0.2	0.8	V	
Time Slot Input TS1, TS2				
High level	2.4	V_{DD}	V	
Low level	−0.2	0.8	V	
Control function Outputs Read/write, SS0, SS1, SS2				
High level	2.4	V_{DD}	V	I_{OH} = −100μA provided
Low level	0	0.45	V	I_{OL} = 1.0mA, V_{XX} = 4.5V
Power				
V_{DD} Supply Current	—	55	mA	No loads
V_{XX} Supply Current	—	5	mA	No loads

PERSONAL TERMINAL

The Teleview Data Acquisition Chip

FEATURES

- Process Teletext and Viewdata input data
- Direct interface with Teleview highways
- Direct interface with standard UAR/T (AY-3-1014A)
- TTL compatible serial teletext data input
- Full checking of teletext data including parity, hamming and data frequency
- "Don't Care" digit facility
- Non-used viewdata control codes made available to Control processor
- Addresses up to eight page Stores

DESCRIPTION

The Data Acquisition (DA) chip takes data from either the TV (teletext) or telephone line (viewdata) via the appropriate interface, processes it according to type and user requests and loads the display data in the correct position in one of eight page Stores.

The processing of teletext and viewdata information is described in separate sections as is the interchange of data with the rest of Teleview system.

INTRODUCTION

The Data Acquisition chip is one of the set of LSI devices comprising the G.I. TELEVIEW (Teletext/Viewdata) system. It may receive data from a TV signal or Telephone line via an appropriate interface and process the data accordingly. Under instruction from a control device it will acquire the requested data and load it into the correct location in the preselected page Store. Control information extracted from the incoming data will be provided to the Teleview system.

The device is fabricated in G.I.'s N-channel metal gate MOS process providing direct TTL interfacing, high speed and good reliability. It is supplied in a 40 lead dual-in-line package.

TELETEXT

If pin 2 is held low the DA will receive data via the serial Teletext data input.

While TS2 is true the DA will monitor RSYNC and the address highways. If a pulse appears on RSYNC it will process a teletext data-line. At other times while TS2 is true it will respond to signals on the address highway and interchange data with a Control Device.

While TS2 is false the DA will do nothing.

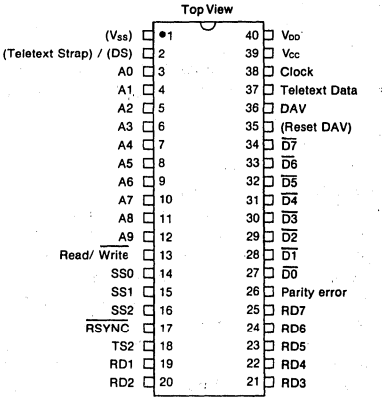
TELETEXT DATA RECEPTION

Data is extracted from the TV video signal by an external circuit called the Data Grabber. This circuit provides a serial data signal and a clock to the DA's input.

A 0.5 μsec pulse will appear on the RSYNC line just before a possible teletext line. The DA will recognize this pulse and monitor the serial data input for clock run-in. It will count four positive transitions of the serial data input and check the frequency of the signal by ensuring that six clock pulses have been received in that time. It will then output a second RSYNC pulse to resynchronize the Data Grabber. If the check fails or the clock pulse counter times out more than two to three teletext characters the DA will go back to its idle state waiting for RSYNC or Data Interchange.

PIN CONFIGURATIONS

40 LEAD DUAL IN LINE



After a valid clock run-in has been detected teletext data is clocked into a serial to parallel converter and Framing Code waited for. Again a time out will cause DA to go idle while the detection of Framing Code will byte synchronized the S-P converter and start the DA receiving the Teletext data as shown in Fig. 1.

The first two words following the Framing Code have data protected by Hamming Code and the appropriate checks and corrections are performed. If the row address indicates that the data is a Page Header (Row O) then the following 8 words are also processed by the Hamming Code circuit. If any Hamming Code fails such that it cannot be corrected, then that data line is rejected.

Requests for pages of teletext data are input to the DA during the Data Interchange periods, described later. When a new page is selected the Page and Time store in the DA is loaded with all '1's indicating "don't care" digits. As keys are pressed by the user of the Teleview system the values are loaded into the DA in the appropriate position.

A comparator in the DA compares Magazine, Page and Time digits one at a time as they are received in the data stream with the digits stored. The comparator will give a true output if the digit compares exactly or if the stored digit is all 1 (value 15). Where an incoming digit has a range less than 4 bits, e.g. time hours tens has the range 0-3 or 2 bits, the unused bits will be made to compare.

Every line of data received is checked for comparison on Magazine number. If this does not compare and the row address indicates that the row is not a Page Header then that row is rejected.

If the Magazine number does not compare and it is a Page Header then, with the exception of Rolling Headers, it is again rejected.

From the time that the DA is told that the P key has been pressed until the selected page has been captured for the first time all Page Headers that compare on Magazine number are loaded into

PIN FUNCTIONS

Pin No.	Name	Function
1	V_{SS}	This is the negative supply for the device and the reference for all signals and electrical parameters.
2	(Teletext Strap)/(DS)	When strapped to V_{SS} (low level) the DA chip will process Teletext. In Viewdata it is the data strobe output to the UAR/T (active low).
3-12	A0 to A9	The 10 bits of address connected to the Address Bus of the Televiewsystem. As outputs they are tri-state and active push-pull for high speed driving the Store. They are also inputs to enable the device to be addressed.
13	Read/ $\overline{\text{Write}}$	The read/write control of the page Stores. The Stores will output data (read) when this signal is high.
14-16	SS0-SS2	Three bits of Store Select code enabling one of eight page Stores. Normally true logic levels but if three or less Stores active low signalling on individual bits may directly enable the Stores.
17	(RSYNC)	A low going pulse indicates to the DA the start of a teletext line. The DA will output a low going pulse within a few microseconds to resynchronize the Data Grabber.
18	TS2	The second of the two time slot bits which, when true, indicates that the DA may use the Data and Address highways.
19-25	RD1 - RD7	Received Data taken directly from the UAR/T.
26	Parity error	The parity error signal from the UAR/T.
27-34	(D0) - (D7)	Data I/Os for connection directly to the Televiewdata highway. As an output the active state is low and there is a passive pull-up on chip so that the signals on the highway may be "wire-ored".
35	(Reset DAV)	An output, low active signal to the UAR/T which will reset its data available output.
36	DAV	The Data Available signal from the UAR/T to indicate a character is available at the RD1-7 pins.
37	Teletext data	Serial data input from Data Grabber. TTL compatible.
38	Clock	Normally the teletext clock running at 6.9375MHz and synchronized to the teletext data by (RSYNC). In Viewdata only applications a 6MHz clock as used by the Video Generator may be input here. TTL compatible.
39	V_{CC}	Connected to +5V. This has a low current requirement and is used mainly for the output drivers.
40	V_{DD}	Connected to +12V, the main positive supply for the device.

the Store except those with the Interrupted Sequence bit (C9) set. This mode of display is referred to as Rolling Headers and provides an indication to the user that data is being received. During this mode the Magazine Serial bit (C11) will override the Magazine comparison. A page of data may be captured when the page number has been fully entered, i.e. the 3rd digit has been received or the T key has been pressed, and a Page Header is received whose Magazine, page and time digits compare with those stored in the DA. That header and all subsequent data lines with correct Magazine number will be stored up to and excluding the next Page Header of correct Magazine number. A "page being received" indication will be set at this time for transmission to the Control device.

Whenever a Page Header is received that fully compares the Control bits accompanying that Header will be stored for subsequent transmission to the Control.

When the content of a data line is ready to be stored that data is loaded into the appropriate Store as defined by the signal from the Control device. Its position in the Store is defined by the Row Address of that data line, the location of the first character being 40 times the Row Address (with the exception of the Page Header which does not have the first 8 characters), with following characters being stored in the next 39 locations of Store.

Each character is checked for odd parity and if the check fails that character is not written. The write signal is removed to avoid overwriting a possible valid character already existing in Store. The last eight characters of every Page Header contain the current clock time and are always written to Store.

VIEWDATA

With pin 2 connected to the Data Strobe input to a UAR/T and not held to earth the DA will process Viewdata.

While TS2 is true the DA is active as far as the Televiewhighways are concerned and it will monitor RSYNC and the Address highway.

When an RSYNC pulse appears the DA will process any Viewdata character it has available. Whenever it is not processing characters it may receive characters asynchronously from the telephone line, via the exclusive connection to the UAR/T, and store them within the DA. Up to three characters may be received and stored before the next processing period when they may be loaded into the page Store. Data Interchange with the televiewsystem may occur when TS2 is high.

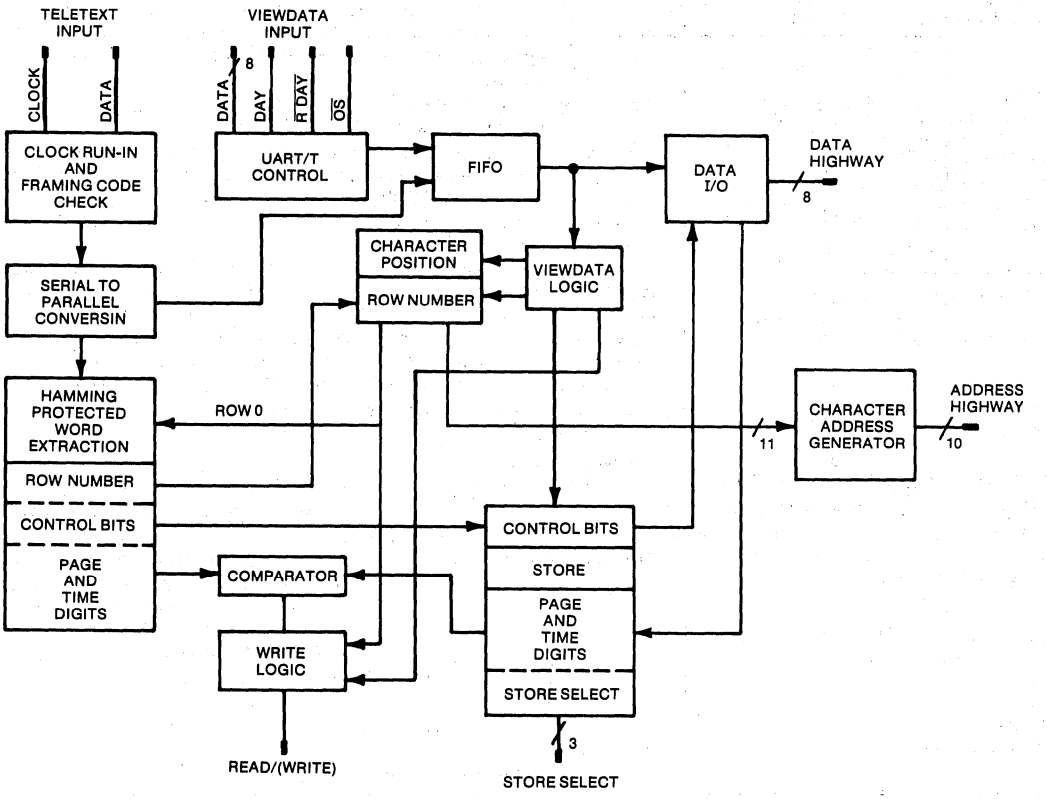
ASYNCHRONOUS DATA RECEPTION

The standard UAR/T (AY-3-1014A) will convert the serial data received via the modem to parallel data for inputting to the DA and indicate a character is ready by the data available (DAV) line. At any time, except when actually processing previously received characters, the DA will read the data and acknowledge on RDAV, a minimum of 3 μsec after the DAV signal.

VIEWDATA CHARACTER PROCESSING

The eight bit input consists of seven bits of data plus a parity fail indication. The codes are shown in Fig. 2.

Characters intened for storage are loaded into the Store in a



AY-3-9710 DATA ACQUISITION CHIP

location determined by the Character Address counter which is always arranged to point to the position in Store into which the next character will be written. The counter is manipulated by the Control Characters appearing in Cols 0 and 1 in the character table.

0/8, Back Space, will cause the Character Address counter to be decremented by one.

0/9, Horizontal Tab, will cause the Character Address counter to be incremented by one.

0/10, Line Feed, will increment by 40.

0/11, Vertical Tab, will decrement by 40.

0/12, Form Feed, will reset to zero.

0/13, Carriage Return, will position the Character Address counter to the beginning of the current block of 40.

0/14, Cursor Home, will reset to zero.

A character in columns 2-7 will be written into the appropriate Store at the location indicated by the Character Address counter which will then be incremented by one.

The ESC character (1/11) will cause some modification of the following character as follows:

if the character is in cols 4 or 5 it will be written to Store with the most significant bit changed to zero.

if the character is in col 3 it will not be written to Store but made ready for transmitting to the Control device.

any other characters, except NUL, will cancel the ESC sequence and be ignored.

The Form Feed character (0/12) will cause the F bit to be set in the appropriate DA to Control signalling word.

All other control characters in cols 0 and 1, except NUL, will be sent to the Control at the appropriate time.

If any character has the parity fail indication set then the character 7/15 will be written to Store. At the start of a processing period (i.e. at RSYNC) if a character is available for processing then the DA will erase the Cursor bit by reading the location pointed to by the Character Address counter and re-writing it. Since the DA never writes the 8th bit in the Store the cursor will be removed.

DATA INTERCHANGE

During the DA's active period, indicated by TS2, when it is not performing any data processing then it will monitor the Address highway for the following codes.

1111XXXX01 indicates the DA should receive data from the data highway.

1111XXXX10 indicates that the DA should send data to the data highway.

1111X0XXXX indicates that the DA should provide control to the UAR/T.

In the Receive mode the Control device may send data according to codes in Fig. 3. The most significant bit of the data acts as a strobe which will cause the other 7 bits to be received and stored in the DA. Magazine, Page and Time digits will be stored in the appropriate location in the digit store, the Store Select number

will be stored for use when accessing the Store and the indications of P and T keys being pressed will also be latched for use in the processing period.

The receiving of data from the Control is completely asynchronous to the DA's internal clock and is controlled entirely by the Strobe bit.

The Send mode will cause the DA to apply the first code, shown in Fig. 4, to the data highway. When the code has been read by Control the signal will be acknowledged by Control forcing all 1s (low levels) which will step the DA on to the second word and so on. The Strobe bit is used in this case to indicate that the data is appearing for the first time and once read by Control, is cleared until new data is available. The exception is the first word which always has the Strobe set.

The UAR/T control is recognized by the DA since it has the UAR/T connections and in this mode a Strobe on the data highway will cause the DA to provide a data strobe (DS) to the UAR/T.

During the Data Interchange period the DA will monitor the Store Select lines and if they are all taken low it will output the current content of the Character Address counter to the address highway so that the control may know where to insert the Cursor.

Control to Data Acquisition Signalling

Active low signalling, most significant bit is a strobe.

Highway Free	0000	0000
Magazine Number	1000	Dddd
Page number tens	1001	Dddd
units	1010	Dddd
Store Select	1011	OS_{SS}
Key pressed	1011	$10K_K$
Spare Code	1011	1100
Spare Code	1011	1101
Spare Code	1011	1110
Dummy Code	1011	1111
Time, hours tens	1100	Dddd
units	1101	Dddd
minutes tens	1110	Dddd
units	1111	Dddd

Where K_K is key identification:

P	00
T	01
Spare 1	10
Spare 2	11

S_{SS} is store select number, 000 to 111. Codes 110, 101 and 011 may be used to address 3 store without decoding and for this veason the system is originally initialized to code 110.

D_{DDD} Digit key value, initially values 0-9 and 15 used although any value may be sent. For Teletext the magazine range is 0-7, Time hours tens range 0-3, Time minutes tens range 0-7. In addition digit 15 is recognized by the DA as a 'don't care' digit causing automatic comparison.

Data Acquisition to Control Signalling

Active low signalling, most significant bit is a strobe. Signals acknowledged by the Control forcing all ones. Control word 1 is sent first and is alwasy sent.

1000 T S_{SS}

where T is the Teletext bit, 1 = Teletext

S s s is the Store Select number the DA is currently using.

Control words 2-4 depend on whether Teletext or Viewdata is being processed.

Teletext

Control word 2	1001	PBR	C_4	C_6	C_5
Control word 3	1010	C_{10}	C_9	C_8	C_7
Control word 4	1011	C_{14}	C_{13}	C_{12}	C_{11}

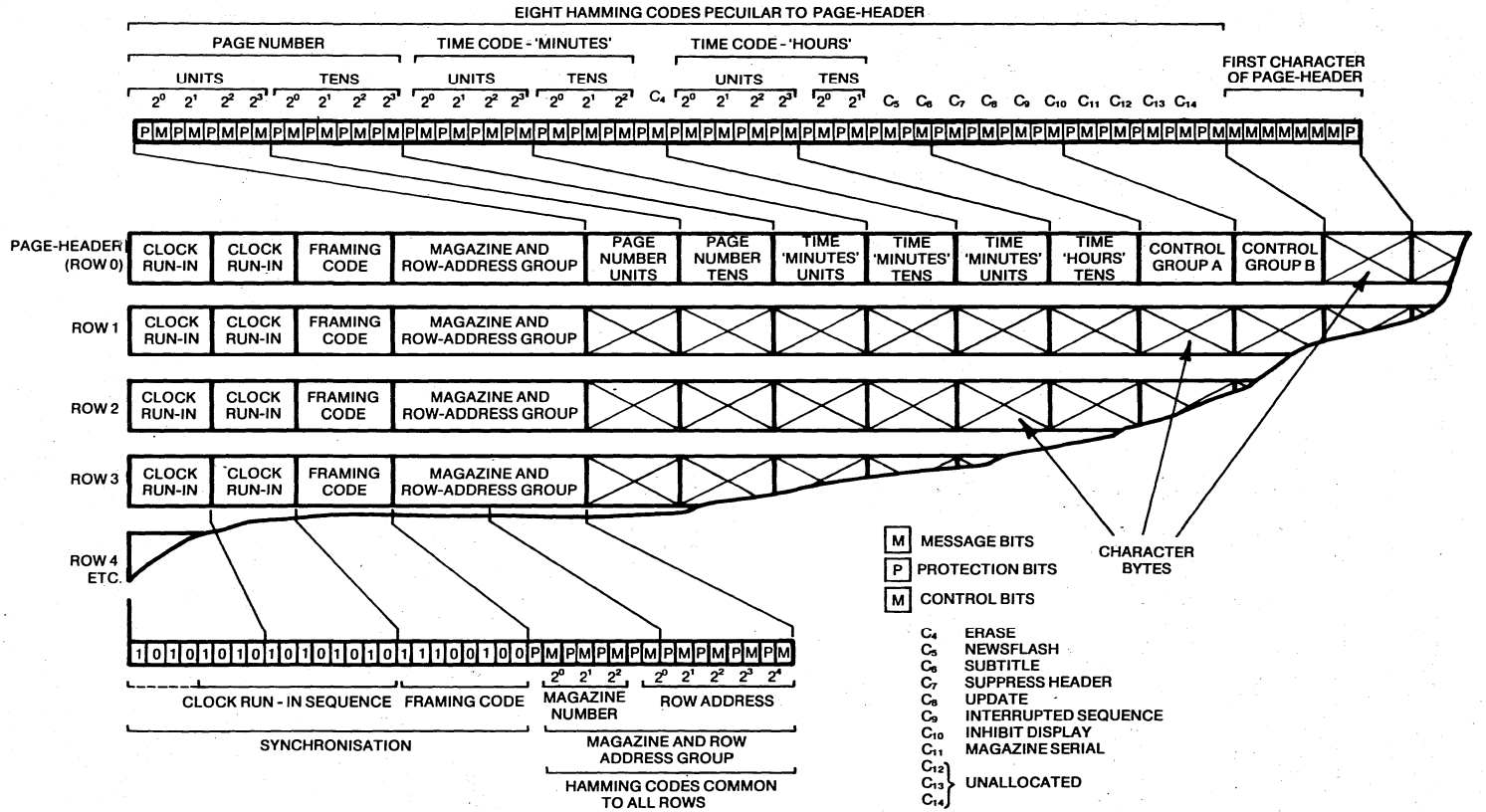
Sent* only when Valid Header recieved.
PBR is set when a page is being received.
C_4 to C_{14} are the Teletext Control Bits.

Viewdata

Control word 2	1001	X	F	0	0
Control word 3	1010	b7	0	b6	b5
Control word 4	1011	b4	b3	b2	b1

Sent* only when a Control Character received by DA.
F is set when Form Feed character detected.
b1-b7 are the 7 bits comprising the Viewdata Character.

*NOTE: that 'sent' means the Strobe bit is set. The other seven bits are actually put onto the highway at the request of the Control and may be used if appropriate (page being received, for example).



SYNCHRONISATION AND HAMMING CODES AT START OF PAGE-HEADER AND ROW TRANSMISSIONS

VIEWDATA TRANSMISSION CODES

	b_7	0	0	0	1	0	1	1	0	1	1	0	1	1	1	1	1
	b_6	0	0	1	0	1	0	1	0	1	0	1	0	1	1	0	1
	b_5	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
bit/s	$b_7b_6b_5b_4b_3b_2b_1$	Col / Row	0	1	2	2a	3	3a	3b	4	4b	5	5b	6	6a	7	7a
	0 0 0 0	0	NUL		Sp		0			@		P		—		p	
	0 0 0 1	1		Cursor DC1 On	1		1		Set Verify Mode (1)	A	Alpha$^{N}_{Red}$	Q	Graphics$_{Red}$	a		q	
	0 0 1 0	2	STX	DC2	"		2		Set Verify (2)	B	Alpha$^{N}_{Green}$	R	Graphics$_{Green}$	b		r	
	0 0 1 1	3	ETX	DC3	£		3		Set Verify (3)	C	Alpha$^{N}_{Yellow}$	S	Graphics$_{Yellow}$	c		s	
	0 1 0 0	4		Cursor DC4 Off	$		4		Set Program Mode	D	Alpha$^{N}_{Blue}$	T	Graphics$_{Blue}$	d		t	
	0 1 0 1	5	ENQ	NAK	%		5		Tape Pause on Playback		Alpha$^{N}_{Magenta}$	U	Graphics$_{Magenta}$				
	0 1 1 0	6	ACK		&		6		Tape Start	F	Alpha$^{N}_{Cyan}$	V	Graphics$_{Cyan}$	f		v	
	0 1 1 1	7			'		7		Tape Stop	G	Alpha$^{N}_{White}$	W	Graphics$_{White}$	g		w	
	1 0 0 0	8	Cursor ← BS	CAN	(		8			H	Flash	X	Conseal$_{Display}$	h		x	
	1 0 0 1	9	Cursor → HT		)		9			I	Steady	Y	Contig$_{Graphics}$	i		y	
	1 0 1 0	10	Cursor ↓ LF		*		:			J		Z	Separated$_{Graphics}$	j		z	
	1 0 1 1	11	Cursor ↑ VT	ESC	+		;			K		—		k		¼	
	1 1 0 0	12	Cursor Home & Clear FF	SS2	,		<			L	Normal$_{Height}$	½	Black$_{Background}$	l		ll	
	1 1 0 1	13	Cursor← CR	SS3	—		+			M	Double$_{Height}$	→	New$_{Background}$	m		¾	
	1 1 1 0	14	SO	Cursor RS Home	.		>			N		↑	Hold$_{Graphics}$	n		÷	
	1 1 1 1	15	SI		/		?			O		‡‡	Release$_{Graphics}$	o		▮	

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... −0.3V to +15V
Storage temperature ..... −55°C to +150°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

Supply voltages = V_{SS} = 0V (substrate voltage)
V_{CC} = +5V ± 5%
V_{DD} = +12V ± 5%
Temperature range = 0°C to +70°C

Characteristic	Min	Typ	Max	Units	Conditions
Address Outputs (tri-state)					
High level	+2.4	—	V_{CC}	V	I_{OH} = −320μA
Low level	—	+0.2	+0.4	V	I_{OL} = 3.2mA
Capacitance	—	—	12	pF	V = 0V
Trise, Tfall	—	—	200	ns	C_{LOAD} = 100pF
Leakage, high impedance state	—	—	5	μA	V_{OUT} = 0V or +5V
Data Outputs (passive pull-up)					
High level	+2.4	—	V_{CC}	V	I_{OH} = −320μA
Low level	—	+0.2	+0.4	V	I_{OL} = 3.2mA
Capacitance	—	—	12	pF	V = 0V
R/(W) and Store Select Outputs					
High level	+2.4	—	V_{CC}	V	I_{OH} = −320μA
Low level	—	+0.2	+0.4	V	I_{OL} = 3.2mA
Capacitance	—	—	7	pF	V = 0V
Current sourced, 'off' state	1.2	—	2.6	mA	V_{OUT} = 0V
(RDAV) and (DS) Outputs					
High level	+2.4	—	V_{CC}	V	I_{OH} = −50μA
Low level	—	+0.2	+0.4	V	I_{OL} = 100μA
Capacitance	—	—	7	pF	V = 0V
RSYNC Output (Open Drain)					
Low level	—	+0.2	+0.4	V	I_{OL} = 4mA
Leakage, output off	—	—	10	μA	V = +12V
INPUTS					
High level	+2.0	—	V_{DD}	V	
Low level	V_{SS}	—	+0.8	V	
Leakage (except I/Os)	—	—	5	μA	V = +12V
POWER					
V_{CC} supply current	—	—	15	mA	V_{CC} = +5.0V
V_{DD} supply current	—	—	55	mA	V_{DD} = +12.0V

Video Generator Chip

FEATURES

- Direct interfacing with the TELEVIEW busses
- Provides master timing signals for the other TELEVIEW chips to indicate the status of the display scan
- Can address up to eight Page Stores
- Provides the address information to scan the allocated Page Store
- Provides composite synchronizing signals for the receiver for 'Off-Hours' working
- Provides various display facilities

DESCRIPTION

The Video Generator chip is one of a set of LSI chips used in the General Instrument TELEVIEW Teletext/Viewdata system. It reads the contents of a Page Store and generates outputs suitable for driving a normal color television receiver to display the contents of the Page Store.

The chip also monitors the composite synchronizing signals within the receiver and locks the total TELEVIEW system onto the incoming signals. When no transmission is taking place the chip develops a composite sync signal which is used to synchronize the receiver.

The device is fabricated in General Instrument's N-channel metal gate MOS process providing direct TTL interfacing, high speed and good reliability.

OPERATION

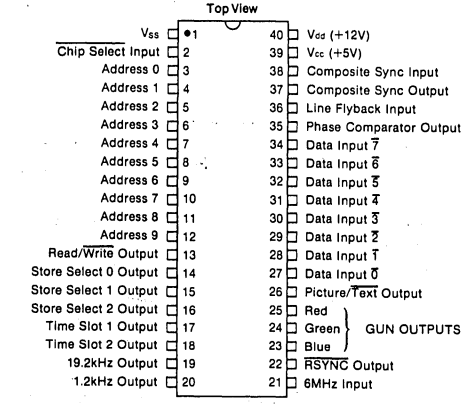
The Video Generator Chip contains the logic and control functions to interrogate a selected TELEVIEW Page Store and display the contained information at the correct period within the raster scan on a normal TV receiver. The chip also generates the master timing signals TS1 and TS2 which indicate the raster status to the Control processor and Data Acquisition chips.

The basic block diagram of the chip is shown in Fig. 1 and major functional blocks are described below.

Line Synchronizing Detector and Generator— The prime function of this block is to detect negative going sync. signals from the incoming mixed sync and to synchronize the TELEVIEW system with the transmitted signal. This is necessary for News flashes and subtitling functions. When the incoming transmission is turned off, (i.e. goes "off-hours"), this is recognized by the detector after three frames of missing sync. pulses. The internal link between Comp. Sync In and Comp. Sync Out is removed and an internally generated "Comp Sync" is switched to the Comp. Sync Out pin. Thus the receiver will continue in lock but synchronized to the Video Generator. Similarly if the normal transmission resumes the fact that external sync pulses are being received is recognized by the Video Generator and the chip will re-synchronize itself with the incoming transmission. Because the Video Generator is aware of the status of the mixed sync at all times the chip can detect frame sync, line sync and even or odd frames. Thus with this information the chip can continuously monitor the current line number. The relevant sections of the line scan are decoded and are indicated externally by the TS1, TS2 time slot outputs. These signals are fully described in Fig. 3, but there are four periods i.e.

PIN CONFIGURATIONS

40 LEAD DUAL IN LINE



a) Writing to RAM.
This occurs during Teletext lines during the frame fly-back period, under control of the D.A. chip.

b) Reading from RAM.
This occurs under control of the Video Generator chip between lines 48 and 288, and is when the display is active.

c) Data Interchange Periods.
The Interchange of information between D.A. and Control Processor and Video Generator occurs during these periods (23-47 and 289-6). Total flexibility is available to the Control Processor at these times as it becomes 'bus master', the peripherals being serviced under the control of the processor.

As the chip is aware of the raster status the chip also starts and stops the Address counter/latch combination which is used to scan the relevant Page Memory. The form of the generated sync pulses are shown in Fig. 2.

Address Counter/Latch— The address counter is a binary counter which is incremented at the character display rate (1MHz). It can also be loaded from a latch which contains the start address of each character row. Since each character consists of 10 vertical lines of raster scan, the counter is incremented 40 times from a start address and then is reloaded with the same start address ready for the next raster scan of the same forty characters. This occurs nine times. On the last line the counter is incremented an extra count and this new address is stored in the latch. This address being the start address of the next row of forty characters. The above sequence is then repeated.

If one is displaying only one half of a page with all characters in double height, the Video Generator scans the same forty addresses nineteen times and stores the new address on the twentieth raster scan. If one is in the bottom half of the page, the address counter must be initialized to 480.

BLOCK DIAGRAM

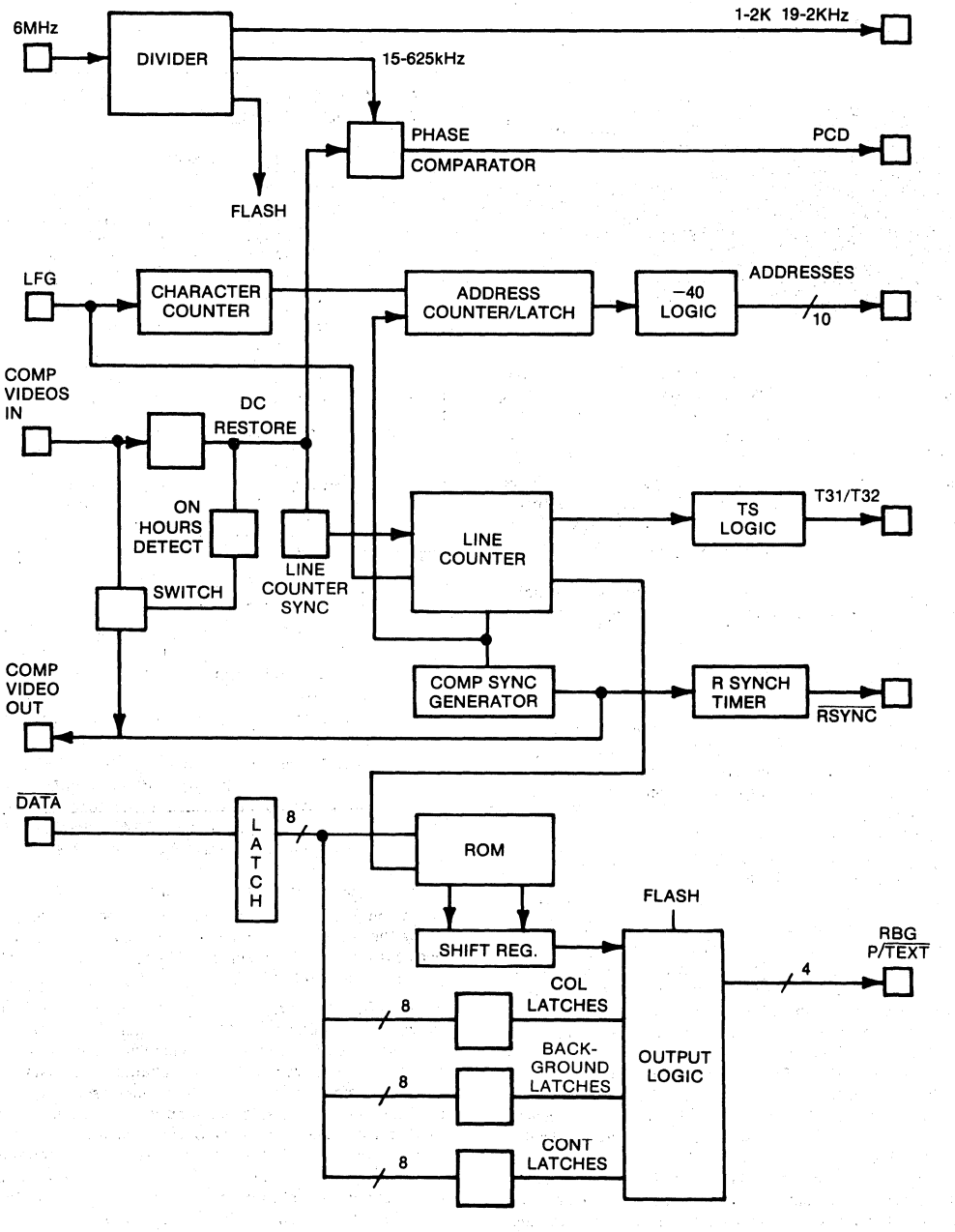


Fig. 1

AY-3-9725 VIDEO GENERATOR CHIP

The display format of 40 characters, each 1μs wide, occurs on a line of 64μs duration thus leaving a border of 12μs on each end of the character row. This address counter is actually started some 4μs before the start of the proper character display thus allowing time for address generation, RAM access time, ROM access time and display processing, these actions being pipelined. Facilities are also provided such that the output address can be reduced by 40 thus allowing accessing of the character in the row above. This is a necessary operation for a 'Double Height' display option which will be discussed later. This facility is inhibited when we are only displaying one half of a page. The address so produced is presented on the address bus and the required Page Memory is activated by the Store Select Outputs. The address drivers are tristate thus allowing easy bus interface.

Input Latches and Character Read-Only Memory—The data being read from the required Page Memory is placed on the Data Bus and is latched into the Data Bus latches. A total of 650ns is allowed for the RAM read cycle and thus quite slow Random Access memories may be used. Having been latched by the Video Generator chip the seven bit character is used to address the character Read Only Memory. This memory is organized as 96 characters each of 45 dots (5 x 9 array).

Data Control Latches—Certain characters indicate to the Video Generator a change in display status. These characters are contained within columns 0 and 1 of the normal Teletext/Viewdata character set and may be used to change character color, background color, height etc. These facilities, and the control of them, are fully described in the British Broadcasting Teletext Specification (Sept. 1976) published by the BBC, IBA and BREMA.

Output Logic and Drivers—The output logic reads the character ROM into a six bit parallel to serial shift register. This operation occurs at the left-hand side of the character to be displayed, the data in the register is then shifted out at 6MHz (character dot-rate) the data bits selecting between character and background information. This information is used to drive the fast Gun output drivers. These outputs have to be closely matched for propogation delay and rise and fall time to ensure good legibility.

DATA INTERCHANGE

During the TS11 timeslot the Video Generator can send information to or receive information from other devices attached to the TELEVIEW system busses. This is normally used by the control chip to update the control and display latched within the Video Generator. The Video Generator is enabled to receive by putting the address 1111XX0XXX on the address highway (active high).

The latches are updated by the following control words, active low signalling, most significant bit is a strobe.

Highway Free	0	0	0	0	0	0	0	0	
Control Word 1	1	0	0	0	T	S	s	s	
Control Word 2	1	0	0	1	X	C_4	C_6	C_5	Teletext
Control Word 3	1	0	1	0	C_{10}	C_9	C_8	C_7	Teletext
Control Word 4	1	0	1	1	C_{14}	C_{13}	C_{12}	C_{11}	Teletext
Control Word 2	1	0	0	1	X	F	0	0	Viewdata
Control Word 3	1	0	1	0	b_7	0	b_8	b_5	Viewdata
Control Word 4	1	0	1	1	b_4	b_3	b_2	b_1	Viewdata
Store Select for Display	1	1	0	0	SP	D	d	d	
Key Data	1	1	0	1	P	*	*	*	
Other Facilities	1	1	1	0	X	X	M	BC	

The Control bits are as follows:

T	TELETEXT MODE i.e. NOT VIEWDATA
S_{SS}	Identification of Store being written to
D_{DD}	Identification of Store being displayed from
C_4/F	Erase page (Rows 1-23 Teletext, Rows 0-23 Viewdata)
C_5	Newsflash (TELETEXT ONLY)
C_6	Subtitle (TELETEXT ONLY)
C_7	Suppress Header (TELETEXT ONLY)
C_8	Update Indicator (TELETEXT ONLY)
C_9	No action (TELETEXT ONLY)
C_{10}	Inhibit display (TELETEXT ONLY)
C_{11}	No action
C_{12}-C	Switches rounding off if all set
b_7-b_1	Cursor bits (Viewdata Only)
001 0001	Cursor ON
001 0100	Cursor OFF
F	Form feed or first appearance
SP	Sets Picture/Text to picture (For initialization)
P	P Key pressed
M	Mix Mode
BC	Box Clock (Teletext Only)
***	These are coded as follows
001	Picture/Text Key pressed
010	Reveal/Conceal Key pressed
011	Update/Clear Key pressed
100	½ Page Key pressed (Cycles Full, Top, Bottom, Full etc.).

PIN FUNCTIONS

Pin No.	Name	Functions
1	V_{SS}	This is the negative supply for the chip and is used as a reference for all the electrical parameters.
2	$\overline{\text{Chip Select}}$ Input	The Chip can be put into its passive state with all Bus and Gun outputs off by taking this input high. This input is internally loaded low. This facility is useful in comprehensive display systems, where several devices may be required to drive the display.
3-12	Addresses 0-9	These pins are connected to the Address Bus of the TELEVIEW system. They are used for address Input/Output.
13	Read/$\overline{\text{Write}}$ Output	This output is used to drive the Random Access Memories forming the Page Memory.
14-16	Store Select Outputs 0-2	These outputs are used to select the required page store.
17,18	Time Slot Outputs 1 and 2	These outputs are generated by the Video Generator from the status of the raster scan and are used to indicate this status to other chips within the TELEVIEW system.
19,20	19.2KHz and 1.2KHz Outputs	These outputs provide 19.2KHz and 1.2KHz square wave signals which are used by the UAR/T as reception and transmission clocks respectively.
21	6MHz Input	This input is fed from a 6MHz oscillator which may be phase locked to the normal transmission. During 'off-hours' working a crystal oscillator is normally used.
22	$\overline{\text{RSYNC}}$ Output	This output is an open-drain output and is used to indicate the presence of Teletext lines to the D.A.Chip and Data Grabber. The timing of this signal is indicated in Fig. 4.
23-25	Red, Green and Blue Gun Outputs	These outputs are push-pull outputs which go high to turn on the relevant color gun for displaying. These outputs are closely matched for propogation delay and rise and fall times.
26	Picture/$\overline{\text{Text}}$ Output	This output is used by the TELEVIEW system to indicate to the receiver if data is to be displayed and is used to change the display from normal video to data video from the Red, Green and Blue chip outputs. In the mix mode this generates Black and White data video. It will then be matched to the gun outputs for propogation delay and rise and fall times.
27-34	Data Inputs $\overline{\phi}$ to $\overline{7}$	The Data Inputs from the communication highway between the Video Generator and the Control Processor and Page Memory.
35	Phase Comparator Output	In on-hours operation the display Line Flyback signal is compared for phase with an internal 64μs period signal derived from the 6MHz display clock. The output is a pulse which, when integrated, produces a voltage for controlling a V.C.O. 6MHz display oscillator, thus locking the display to the incoming picture. In off hours operation this open drain output goes low permanently, and thus can be used as an indication of on-hours/off-hours status.
36	Line Flyback Input	The Line Flyback input is a signal from the display deflection circuitry which is used for positioning the display on the T.V. screen.
37	Comp. Sync Output	The Comp. Sync Output outputs either the Comp. Video input in 'on-hours' operation or an internally generated Comp. sync signal in 'off-hours' operation.
38	Comp. Sync Input	The Comp. Sync Input monitors the composite video being received and extracts synchronizing information and 'on-hours' 'off-hours' information for the Video Generator.
39	V_{CC}	This pin is connected to the +5.0V supply. This supply has a low current requirement .
40	V_{DD}	The V_{DD} forms the positive supply for the chip.

DISPLAY OPTIONS

Logic is contained on the Video Generator chip to process the Display Modes as described in the Broadcast Teletext Specification. These facilities are outlined below. Some extra facilities are also included.

Character Set

The chip can display 96 Alphanumeric characters and 64 Graphic shapes which may be either contiguous or separated. The alphanumeric format is determined by a 4320 bit Read Only Memory organized as:

96 (character) x 5 (dots) x 9 (lines) = 4320

The graphic shapes are determined directly from the bits of the character code Fig. 5.

Display and Background Color

The characters and the background can be displayed in one of seven colors. In addition the background may be black. This information is stored in two sets of three latches representing character and background colors.

Conceal and Flash

Selected characters can be concealed and optionally released by the viewer. Selected characters can be flashed on command. The flashing is controlled by an on-chip flash oscillator. During the flash period or when concealed only background information is displayed.

Boxing

Text or graphics characters can be inserted in a normal video picture when required. This is achieved by means of the Picture-/$\overline{\text{Text}}$ output which can be used externally to switch the guns between Picture and text signals.

Double Height

Double height characters are characters contained between the control characters "Double Height" and "Normal Height" (or end of line). When a "Double Height" control character is read from the RAM only the top half of the subsequent character(s) are displayed during the 10 raster scans. During the next 10 scan lines, 40 is subtracted from the addresses being output on A0-A9 so the same 40 addresses are read for another 10 times. Characters which are not double height are displayed as the background color and the bottom(s) of the double height character(s) is (are) displayed.

Hold Graphics

When this latch is set, any subsequent control characters (except Double/Normal Height or change alpha/graphics) are displayed as the last graphics characters.

Special Graphics

This is a high resolution graphics facility, not available in normal Teletext/Viewdata systems. There is a one to one correspondence between data bits b_1, b_2, b_3, b_4, b_5, b_7 and the six dots in each horizontal line of a character. This gives an overall graphics resolution of 6 x 20 for each character.

Box Clock

The last eight characters of the top row (Row 0) of a teletext page can be boxed in double height into a normal television picture. These eight characters contain the time in BBC/IBA broadcasts.

Half-page Operation

This allows either the top or bottom half of a normal Teletext/Viewdata page to be displayed over the whole screen, with each character in double height. This makes the display easier to read from a distance. Double height characters are ignored in this mode.

Black and White Output

In normal operation this is the Picture/Text output and is used to blank the normal picture information for boxing newsflashes or displaying a page of teletext information, etc.
In the mix mode this outputs black and white teletext information which is matched to the Gun Output signals in delay and drive. This can be used to superimpose text onto a picture by "cutting away" the picture below text data or as an output for Black and White displays or printers.

Character Rounding Inhibit

Normally characters are rounded, i.e. half dots are added to smooth diagonals on an interlaced television display. This can be switched off when outputting to a printer.

Cursor

The cursor is stored as bit eight in the Page Store Data Character. It is displayed as a flashing bar on the bottom line of a character. The flashing is complementary to the normal character flashing and any character information on the bottom line (tails or graphics information) is suppressed to improve legibility.

SIGNAL DETECTION CRITERIA

The Video Generator detection circuitry for incoming sync signals is designed to prevent mis-operations in the presence of noise. The criteria for detection is defined below.

Line Sync

The Comp. Video Input must be negative for greater than 3μs.

Frame Sync

The Comp. Video Input must be negative for greater than 10μs and at least 310 lines (Line Flyback pulses) must have occurred since the previous Frame Sync detection.

Odd Frame Detection

Odd Frame Detection occurs when a Line Flyback pulse falls in a window 326-354 uS after Frame Sync Detection. However this detection must disagree with the internal Odd/Even frame status for 4 successive full frames before the internal status is inverted.

On-Hours/Off-Hours Detection

The Line Flyback pulse is compared for synchronism with the detected Line Sync such that the negative edge of Line Flyback should occur within 14μs of the negative edge of an incoming Line Sync signal. If such synchronism does not occur the number is accumulated and if more than 16 occur for two successive ½ frames the logic deems that the composite sync does not represent a valid transmitted signal and the Video Generator goes "Off-Hours". If however, less than eight occur in any two successive ½ frames, the logic deems that a valid Comp. Sync is being received and the system goes "On-Hours". If between eight and sixteen occurrances of no synchronism happen, then the system stays as it was.

ELECTRICAL CHARACTERISTICS

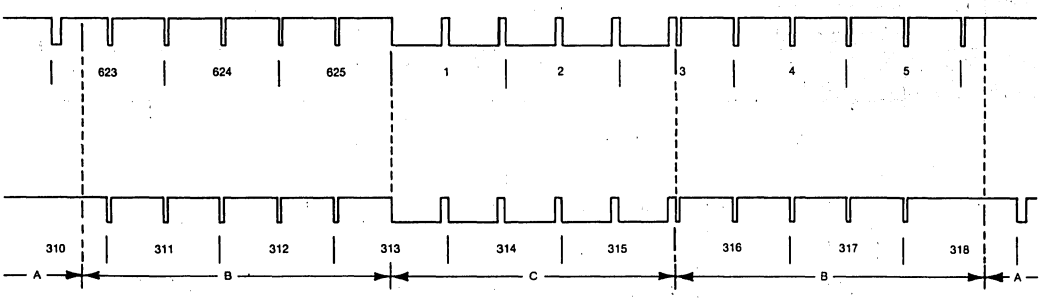
Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... −0.3 to +15V
Storage temperature range ..... −55°C to +150°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise indicated)
V_{SS} = 0V (substrate voltage) V_{CC} = +5V ± 5% V_{DD} = +12V ± 5% Operating Temperature T_A = 0°C to +70

Characteristic	Min	Typ	Max	Units	Conditions
INPUTS					
Chip Select					
Input Logic High	2.0	—	V_{DD}	V	
Input Logic Low	V_{SS}	—	0.8	V	
Input Current	25	—	120	μA	V_{IN} = 5V
COMP					
Input Logic High	2.5	—	V_{DD}		
Input Logic Low	V_{SS}	—	0.3		
Input Capacitance	—	—	15	pF	V_{IN} = 0V
6MHz					
Input Logic High	2.0	—	V_{DD}	V	
Input Logic Low	V_{SS}	—	0.8	V	
Input Capacitance	—	—	25	pF	V_{IN} = 0V
Mark to Space Ratio	45:55	—	55:45		
Frequency	1.0	—	6.5	MHz	
ALL OTHER INPUTS					
Input Logic High	2.0	—	V_{DD}	V	
Input Logic Low	V_{SS}	—	0.8	V	
Input Capacitance	—	—	15	pF	V_{IN} = 0V
Input Leakage	—	—	10	μA	V_{IN} = 12V
OUTPUTS					
Addresses, Read/Write					
Store Select (Tri-state)					
Logic High Output	2.4	—	V_{CC}	V	I_{OH} = -320μA
Logic Low Output	V_{SS}	0.2	0.4	V	I_{OL} = 3.2mA
Capacitance	—	—	15	pF	V_{IN} = 0V @ 1MHz
T_{RISE}, T_{FALL}	—	—	200	ns	C_{LOAD} = 100pF
Leakage (Disabled)	—	—	10	μA	V_O = 0V, 5V
TIME SLOTS (TS1, TS2)					
(PUSH-PULL)					
Logic High Output	2.4	—	V_{CC}	V	I_{OH} = -320μA
Logic Log Output	V_{SS}	0.2	0.4	V	I_{OL} = 3.2mA
T_{RISE}, T_{FALL}	—	—	200	ns	C_{LOAD} = 100pF
COMP VIDEO (PUSH—PULL)					
Logic High Output	4	—	V_{DD}	V	I_{SOURCE} = −500μA) } Off Hours Mode
Logic Low Output	V_{SS}	—	0.4	V	I_{SINK} = 1.6mA) }
Capacitance	—	—	20	pF	
Series Resistance	—	—	100	ohms	Comp. Video In = 2V), On Hours Mode
RSYNC (OPEN DRAIN)					
Logic Low Output	V_{SS}	—	0.4	V	I_{OL} = 4.0mA
Logic High leakage	—	—	10	μA	V_O = 5V
Capacitance	—	—	15	pF	V_{IN} = 0V
PHASE COMPARATOR (OPEN DRAIN)					
Logic Low Output	V_{SS}	—	0.5	V	I_{OL} = 5mA
Logic High Leakage	—	—	10	μA	V_O = 5V
Capacitance	—	—	15	pF	V_{IN} = 0V
R.G.B. GUN OUTPUTS					
PICTURE/TEXT OUTPUTS (TRISTATE)					
Logic High Output	V_{CC}-1	—	V_{CC}	V	I_{SOURCE} = 2mA
Logic Low Output	V_{SS}	—	1	V	I_{SINK} = 5mA
Capacitance	—	—	20	pF	V_{IN} = 0V
T_{RISE}, T_{FALL} (10%-90%)	—	—	30	ns	C_O = 30pF
Differential T_{RISE}, T_{FALL}	—	—	30	ns	C_O = 30pF Picture/$\overline{\text{Text}}$ matched in mix mode only
Leakage (Disabled)	—	—	10	μA	V_O = 0, 5V[1]
POWER					
V_{CC} Supply	—	—	25	mA	V_{CC} = 5V
V_{DD} Supply	—	—	80	mA	V_{DD} = 12V



A. LINE SYNC PULSES NEGATIVE. 5μS WIDTH. 64μS PERIOD.
B. EQUALIZING PULSES NEGATIVE. 2μS WIDTH. 32μS PERIOD.
C. BROAD PUSLES POSITIVE 4μS WIDTH. 32μS PERIOD.
ALL NEGATIVE EDGES AT 64μS OR 32μS INTERVALS.

Fig. 2 COMPOSITE SYNC

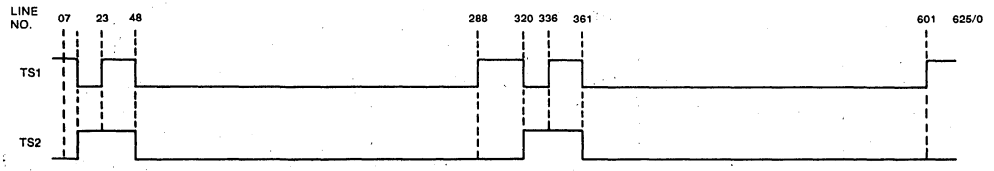


Fig. 3 TIME SLOT OUTPUTS

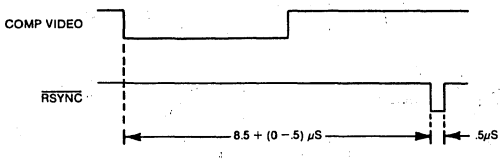
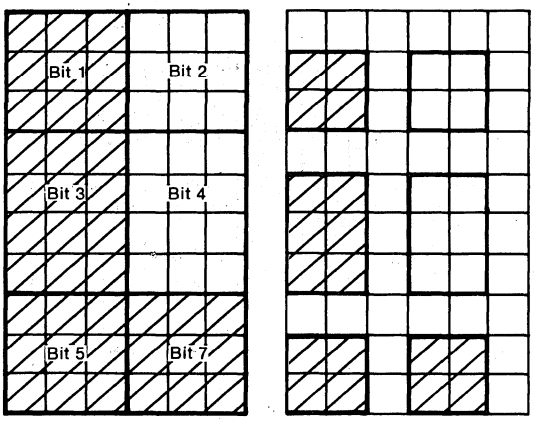


Fig. 4 $\overline{\text{RSYNC}}$ TIMING



BIT 1 IS LEAST SIGNIFICANT, BIT 6 = 1

SHADED EXAMPLE 1110101

Fig. 5 GRAPHICS FORMAT

b_7 b_6 b_5 →						0 0 0	0 0 1	0 1 0		0 1 1		1 0 0	1 0 1	1 1 0		1 1 1	
Bits	b4	b3	b2	b1	Col Row	0	1	2	2a	3	3a	4	5	6	6a	7	7a
	0	0	0	0	0	NUL①	DLE①			0		@	P	—		p	
	0	0	0	1	1	Alpha^N Red	Graphics Red	!		1		A	Q	a		q	
	0	0	1	0	2	Alpha^N Green	Graphics Green	"		2		B	R	b		r	
	0	0	1	1	3	Alpha^N Yellow	Graphics Yellow	£		3		C	S	c		s	
	0	1	0	0	4	Alpha^N Blue	Graphics Blue	$		4		D	T	d		t	
	0	1	0	1	5	Alpha^N Magenta	Graphics Magenta	%		5		E	U	e		u	
	0	1	1	0	6	Alpha^N Cyan	Graphics Cyan	&		6		F	V	f		v	
	0	1	1	1	7	Alpha^{N}② White	Graphics White	'		7		G	W	g		w	
	1	0	0	0	8	Flash	Conceal Display	(		8		H	X	h		x	
	1	0	0	1	9	Steady②	Contiguous② Graphics	)		9		I	Y	i		y	
	1	0	1	0	10	End Box②	Separated Graphics	*		:		J	Z	j		z	
	1	0	1	1	11	Start Box	ESC①	+		;		K	←	k		¼	
	1	1	0	0	12	Normal② Height	Black② Background	,		<		L	½	l		‖	
	1	1	0	1	13	Double Height	New Background	-		=		M	→	m		¾	
	1	1	1	0	14	Special Graphics	Hold Graphics	.		>		N	↑	n		÷	
	1	1	1	1	15	Normal② Graphics	Release② Graphics	/		?		O	#	o		■	

①These control characters are reserved for compatability with other data codes.

②These control characters are presumed before each row begins
Codes may be referred to by their column and row e.g. 2/5 refers to %

Character rectangle

Black represents display color

White represents background

Fig. 6 TELETEXT CHARACTER CODES

Telecommunications 6

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
			Telephony
5 CHANNEL RELAY DRIVER	Isolates +5V logic and exchange-powered relays.	AY-5-9050	6-4
PUSH BUTTON TELEPHONE DIALLERS	Converts push button input to rotary dial pulses.	AY-5-9100	6-6
		AY-5-9151A/52	6-10
		AY-5-9153A/54A	6-10
		AY-5-9158	6-16
REPERTORY DIALLER	Stores ten 22 digit telephone numbers.	AY-5-9200	6-19
DUAL-TONE MULTI-FREQUENCY GENERATORS	Generates DTMF/tone telephone frequencies.	AY-3-9400	6-25
		AY-3-9401	6-25
		AY-3-9410	6-25
CLOCK GENERATOR	Generates 2-phase clocks from a single power supply.	AY-5-9500	6-28
DUAL-TONE MULTI-FREQUENCY RECEIVERS	Detects and converts DTMF/tone telephone frequencies.	AY-5-9801	6-32
		AY-5-9802	6-32
		AY-5-9803	6-32
		AY-5-9804	6-32
		AY-5-9805	6-32
		AY-5-9807	6-32
		AY-5-9808	6-32
CODEC	Duplex Delta-Sigma/PCM converter.	AY-3-9900	6-37
MICRO-COMPUTER DIALLERS	A single-chip microcomputer pre-programmed for in-telephone applications.	TZ-2001	6-44
		TZ-2002	6-44
		TZ-2003	6-44
			Telecom Hybrids
UNIVERSAL ACTIVE FILTERS	Generate any filter response by means of external connections.	ACF 7092C	6-52
LOW PASS FILTERS	PCM transmit filter.	ACF 7270C	6-56
	PCM receive filter.	ACF 7271C	6-58
BAND PASS FILTERS	Full wave detector and a factory tunable four pole fixed bandwidth band pass filter.	ACF 7300C	6-60
		ACF 7301C	6-62
		ACF 7302C	6-63
	Detects and passes the 2600Hz signalling frequency.	ACF 7310C	6-66
	DTMF/tone detection band pass filters.	ACF 7323C	6-68
		ACF 7363C	6-68
		ACF 7383C	6-68
	Detects and passes the 2800Hz signalling frequency.	ACF 7328C	6-70
BAND REJECTION FILTERS	Rejects the 2600Hz signalling frequency.	ACF 7410C	6-72
		ACF 7412C	6-73
		NCS 2061	6-74
	Rejects the 2800Hz signalling frequency.	NCS 2062	6-74
BAND SEPARATION FILTERS	Isolates low and high groups of DTMF frequencies.	ACF 7711C	6-75
	DTMF Low Group Band Splitting Filter.	ACF 7720	6-77
	DTMF High Group	ACF 7721	6-78
			Data Communications
UAR/T	Complete 5-8 bit receiver/transmitter interface.	AY-5-1013A	6-80
		AY-6-1013	6-80
		AY-3-1014A	6-80
		AY-3-1015D	6-80
16 CHANNEL MULTIPLEXER	Multiplexes 16 analog channels with on-chip logic control.	AY-5-1016	6-93
		AY-6-4016	6-93

TELECOM

Telephony

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
5 CHANNEL RELAY DRIVER	Isolates +5V logic and exchange-powered relays.	AY-5-9050	6-4
PUSH BUTTON TELEPHONE DIALLERS	Converts push button input to rotary dial pulses.	AY-5-9100	6-6
		AY-5-9151A/52	6-10
		AY-5-9153A/54A	6-10
		AY-5-9158	6-16
REPERTORY DIALLER	Stores ten 22 digit telephone numbers.	AY-5-9200	6-19
DUAL-TONE MULTI-FREQUENCY GENERATORS	Generates DTMF/tone telephone frequencies.	AY-3-9400	6-25
		AY-3-9401	6-25
		AY-3-9410	6-25
CLOCK GENERATOR	Generates 2-phase clocks from a single power supply.	AY-5-9500	6-28
DUAL-TONE MULTI-FREQUENCY RECEIVERS	Detects and converts DTMF/tone telephone frequencies.	AY-5-9801	6-32
		AY-5-9802	6-32
		AY-5-9803	6-32
		AY-5-9804	6-32
		AY-5-9805	6-32
		AY-5-9807	6-32
		AY-5-9808	6-32
CODEC	Duplex Delta-Sigma/PCM converter.	AY-3-9900	6-37
MICRO-COMPUTER DIALLERS	A single-chip microcomputer pre-programmed for in-telephone applications.	TZ-2001	6-44
		TZ-2002	6-44
		TZ-2003	6-44

Five Channel Relay Driver/High Voltage Interface

FEATURES

- Reference voltages generated and regulated on-chip from a single power supply
- High noise immunity
- High reliability and low cost using P-channel MTNS process (approved to BPO D4000)
- Defined output states under external fault conditions
- Provides isolation between +5V logic and exchange powered relays
- TTL compatible
- Supplies continuous load currents up to 250mA.

DESCRIPTION

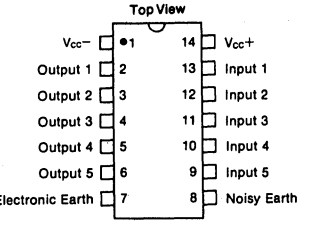
The circuit contains five individual channels, each comprising a logic section which switches a high current output driver. Delay circuitry is incorporated to improve rejection of noise interference on the inputs. The input logic levels are standard TTL compatible, and since only a very small input current is required, a resistor of up to 10K may be connected in series to protect the preceding logic under fault conditions.

Each output driver is capable of supplying 50mA to a load connected directly to a nominal −48V exchange supply, and when higher currents and/or lower output voltages are required, channels may be paralleled externally to provide up to 250mA. Each driver operates as a buffer with a high impedance input and a high current output able to withstand large negative voltages in the OFF condition. In the ON condition, each output may be considered as a resistor of 40Ω maximum with a current rating of 50mA.

Isolation is provided between the logic circuitry and the exchange (noisy) earth. Although the exchange earth may fluctuate by ±4V, malfunction of the logic circuitry will not occur since the exchange earth is at −5V with respect to the logic supply.

PIN CONFIGURATION

14 LEAD DUAL IN LINE



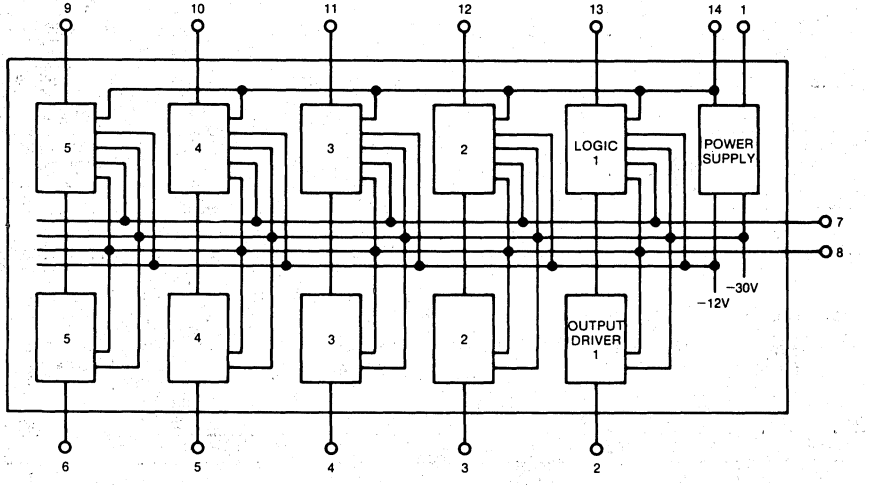
CIRCUIT FUNCTION

Input State	Output State
Logic '0'	On
Logic '1'	Off
Open Circuit	Off

CIRCUIT FUNCTION UNDER FAULT CONDITIONS

Fault Condition	Output State
V_{CC}+ open circuit	Off
Electronic earth open circuit	Not defined
Noisy earth open circuit	Off

BLOCK DIAGRAM



TELECOM

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Maximum continuous power dissipation 800mW
Maximum continuous supply voltage (V_{CC}+) ..... +7.0V
Minimum continuous supply voltage (V_{CC}+) ..... −0.3V
Maximum continuous supply voltage (V_{CC}−) Pin 8 = 0V ..... −60V
Maximum continuous positive input voltage Pin 7 = 0V ..... +7.0V
Maximum continuous negative input voltage Pin 7 = 0V ..... −12V
Maximum continuous positive output voltage Pin 8 = 0V ..... +4.0V
Maximum continuous negative output voltage (output off) ..... −65V
Maximum continuous negative output current per channel 60mA
Maximum continuous noisy earth voltage with respect to electronic earth ..... ±5.25V
Operating temperature range ..... 0°C to 70°C
Storage temperature range ..... −55°C to 125°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

Positive supply (V_{CC}+) = +4.75V to +5.25V
Negative supply (V_{CC}−) = −44V to −52V
Noisy earth wrt 0V = ±4.0V
Ambient temperature = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Supply current (I_{CC})	—	3.5	5.0	mA	V_{CC}+=5.25V; V_{CC}−=−52V; Outputs on
Outputs Off					
Logic '1' Input voltage	3.0	—	V_{CC}+	Volts	V_{CC}+=5.25V; V_{CC}−=−44V
Logic '1' Input current	—	7	25	μA	V_{CC}+=5.25V; V_{IN} ⩾3.0V; Pin 7=0V
Outputs On					
Logic '0' Input voltage	−12.0	—	0.4	Volts	V_{CC}+=4.75V; V_{CC}−=−52V
Logic '0' Input current	—	7	25	μA	V_{CC}+=5.25V; V_{IN}⩽0.4V; Pin 7=0V
Output On Resistance (R_{ON})	—	20	40	Ω	V_{CC}+=4.75V; V_{CC}−=−44V; I_{out}=50mA
On State Output Voltage	0.2	1.0	2.0	Volts	V_{CC}+=4.75V; I_{out}=50mA; Pin 8=0V
Output Leakage Current (Off)	—	50	200	μA	V_{CC}+=4.75V; $\overline{V_{out}}$ =−60V; Pin 8=0V
Output Leakage Current (Off)	—	60	1000	μA	V_{CC}+=4.75V; V_{out}=−65V; Pin 8=0V
Propagation Delay and Transition Time (T_{pon} + T_{on} and T_{poff} + T_{off})	—	50	300	μs	See Fig. 1

**Typical values are at +25°C and nominal voltages.

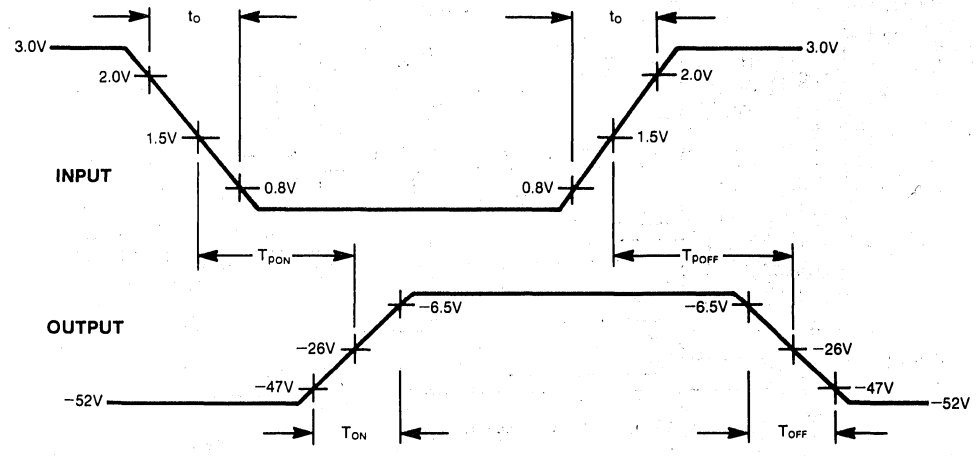


Fig.1 TRANSITION TIME

TELECOM

Push Button Telephone Diallers

FEATURES

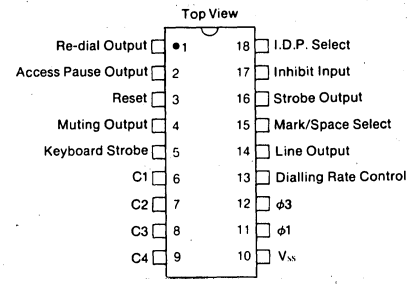
- 20 Digit Storage
- Selectable dialling rate
- Selectable mark/space ratio
- Selectable Inter-Digit Pause
- Dynamic circuitry — low power consumption
- Re-dial of last number
- Access Pause Facility
- Companion Repertory Dialler chip (AY-5-9200)

DESCRIPTION

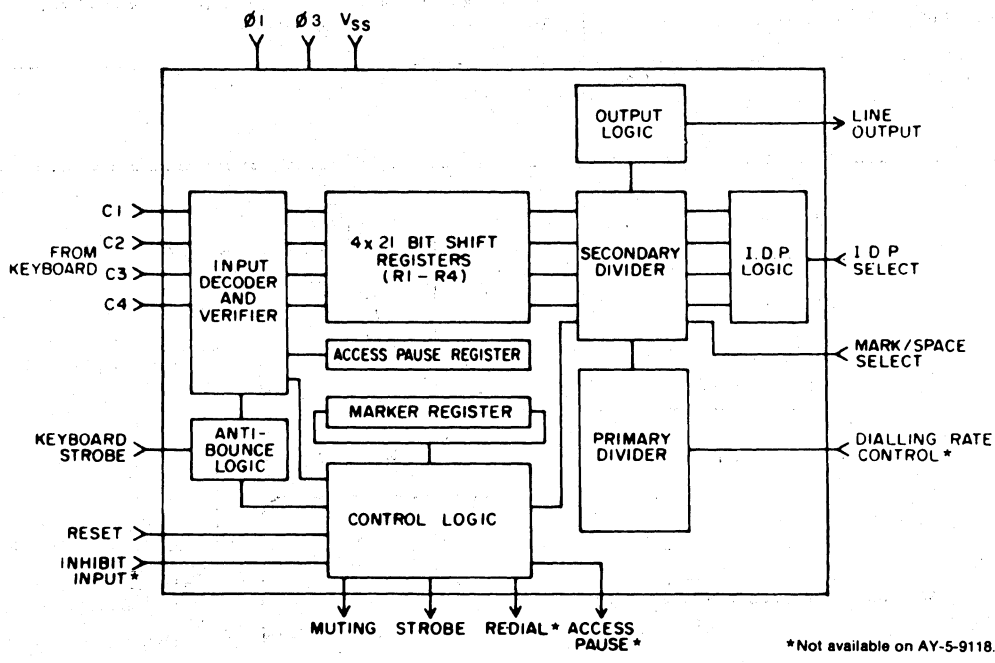
The AY-5-9100 Series Push Button Dialler provides all of the logic required to convert a push button input to a series of pulses suitable for simulating a telephone dial. Pulse repetition rate, interdigital pause, and mark-space ratio are all programmable. Outputs are provided for line pulsing and muting. An "inhibit input" is provided to allow redial of one number of up to 20 digits. An "Access pause" capability is provided to allow automatic operation with a PBX or WATS line system. The low power consumption enables line-powered operation in a PBX or similar system. An AY-5-9100 Series circuit may be operated alone or in conjunction with the AY-5-9200 repertory dialler.

PIN CONFIGURATION

18 LEAD DUAL-IN-LINE
AY-5-9100



BLOCK DIAGRAM



*Not available on AY-5-9118.

TELECOM

PIN FUNCTIONS

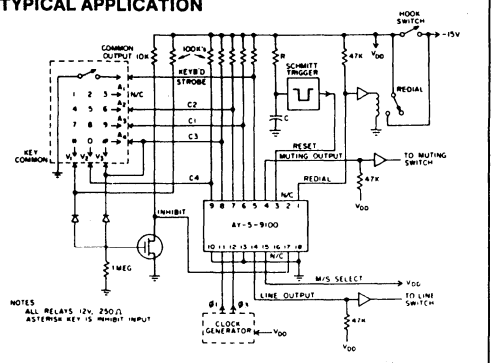
Pin No.	Name/Description
1	**Re-Dial Output:** A logic "0" at this output indicates that redial mode has been selected.
2	**Access Pause Output:** A logic "0" at this output indicates that an access pause is required.
3	**Reset:** A logic "0" on this input clears all shift registers and resets all counters. Reset should be applied after power on to clear the device.
4	**Muting Output:** The muting output goes to logic "0" whenever data is being entered or transmitted. It returns to logic "1" when the access pause output turns on and when transmission is complete.
5	**Keyboard Strobe:** This is the common signal from all the keys. A logic "0" on this input indicates that either the inhibit input or C1-C4 are to be read.
6-9	**C1-C4** These are the keyboard data inputs. They are encoded as follows to allow simple interface with a standard push button)2-of-7) keyboard .

Digit	Impulses	C1	C2	C3	C4
1	1	1	1	1	1
2	2	1	1	1	0
3	3	1	1	0	1
4	4	1	0	1	1
5	5	1	0	1	0
6	6	1	0	0	1
7	7	0	1	1	1
8	8	0	1	1	0
9	9	0	1	0	1
0	10	1	1	0	0
Access Pause	—	0	0	1	1

10	**Vss**
11	**ϕ1**
12	**ϕ3**
13	**Dialling Rate Control** This input controls the line pulsing frequency as follows: (See Note 1):

Input	Line Pulse Rate
ϕ1	600 p.p.s.
ϕ3	20 p.p.s.
V_{SS}	10 p.p.s.

TYPICAL APPLICATION



Pin No.	Name/Description
14	**Line Output** A logic "0" on this output is a line pulse "mark" or "break."
15	**Mark/Space Select** The mark to space ratio is controlled by this input as follows:

Input	Mark	Space
ϕ1	70	30
ϕ3	50	50
Logic 0	66 2/3	33 1/3
Logic 1	60	40

These ratios are exact and do not depend on clock frequency.

16	**Strobe Output** This output goes to logic "0" to indicate that a digit is being out-pulsed.
17	**Inhibit Input** The inhibit input is used to inhibit out-pulsing and to place the device in re-dial mode.

The keyboard strobe must be taken to logic "0" at any time the inhibit input is strobed, except when an Access Pause is being signalled.

This input normally operates as a "toggle flip-flop". If it is taken to a logic "1" any time other than when an access pause is being signalled, the circuit will lock into the redial mode and the redial output will go to logic "0". The chip will remain in the re-dial mode until this input is taken to logic "1" again.

If the chip is cleared before inhibit is toggled, digits entered are accepted, but out-pulsing does not commence until the inhibit is re-strobed. If a number is being outpulsed when the inhibit is strobed, dialling ceases until the inhibit is re-strobed. If the inhibit is strobed when a dialling sequence is completed, the redial output goes to logic "0" and the number is stored. Re-strobing the inhibit starts the dialing sequence.

When an access pause is signalled, this input no longer operates as a toggle, but rather as a gate, with a logic "1" inhibiting further out-pulsing.

18	**I.D.P. Select** This input controls the inter-digital-pause as follows: (See Note 1):

Input	10p.p.s.	20p.p.s.	600p.p.s.
ϕ3	400ms	200ms	6.66ms
V_{SS}	800ms	400ms	13.33ms
ϕ1	1000ms	500ms	18.33

A pre-digital pause equal in length to the inter-digital pause precedes the first digit of any number.

NOTE 1: Line Pulse Frequency and Inter-Digital Pause are specified with an 18KHz clock frequency.

TELECOM

OPERATION

The 4 bit code from the keyboard arrives on inputs C1-C4 of the Push Button Dialler. A fifth input from the keyboard, the Keyboard Strobe, is also required. In its quiescent state the five inputs are at logic 1 (–volts). A logic 0 on the Keyboard Strobe input indicates to the input circuitry that it is to read the data on C1-C4, thus allowing 1111 as an allowable code from the keyboard.

When a digit key is depressed the logic detects the 1-0 transition on the Keyboard Strobe input. When this occurs a timer with a minimum count time of 4.2 msec is started. If the common input is removed before this period has elapsed, the counter will be reset to its starting state. If the Keyboard Strobe input is stable for at least 8.7 msec the code is fed to the code verifier and converter.

If the code is invalid, it is ignored. If valid it is converted to the proper BCD code and written into recirculating shift registers R1-R4. If an access pause is decoded, it is written into the access pause register.

Simultaneous with the data being written into R1-R4, the muting output goes to logic "0", to disconnect the transmission circuitry. When all digits that have been keyed into the circuit have been dialled out the muting output returns to logic "1".

During dialling if an access pause is required, the muting output will reconnect the transmission circuitry so that the caller can listen for the dial tone and ensure himself that the system is functioning correctly.

The digit store has a capacity of 20 digits. The numbers are read non destructively allowing redial.

Four 21 bit registers hold the number in BCD format; the number is stored in parallel. A fifth register holds a marker bit (Signified as A) showing the first number entered. This fifth register has a gated 22nd bit allowing the marker bit (A) to be 'slipped' backwards one bit with respect to the number. Gating ensures that all numbers are sequentially entered, the first aligning itself with the marker A. When the first number is to be loaded into the counter, A is decoded in its 21st position and the parallel enable signal reads the first digit into the counter. Gating is enabled to allow A to be shifted through the 22nd bit of the marker store, so aligning itself with the next number to be dialled out. When A is decoded at the 21st bit and no number is in the stored digit register, A remains aligned in this state until 'redial' is depressed and the marker store goes into its 22nd bit mode until A aligns with the first digit.

Gating ensures that only 20 digits are entered into R1-4. One empty state at least is required to indicate to the system that a number is complete.

TIMING DIAGRAMS (L = Low = Logic "1"; H = High = Logic "0")

Fig.1 Clock Waveforms

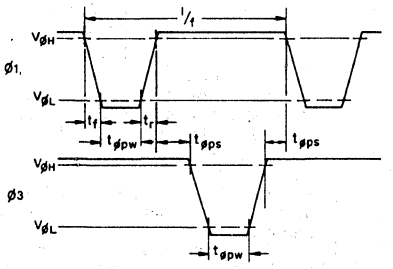


Fig.2 Reset and Keyboard Strobe Timing

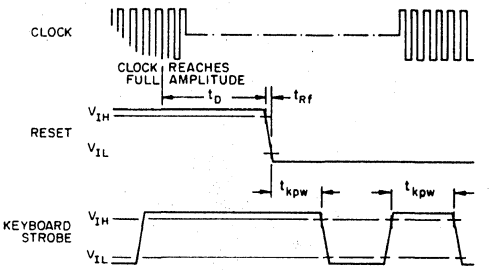


Fig.3 Line, Muting and Strobe Output Timing

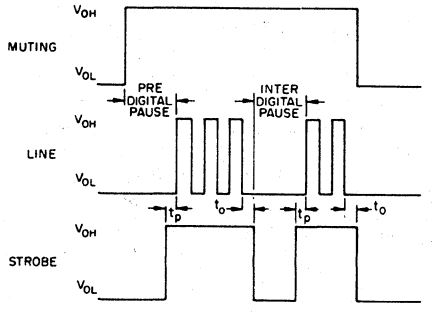
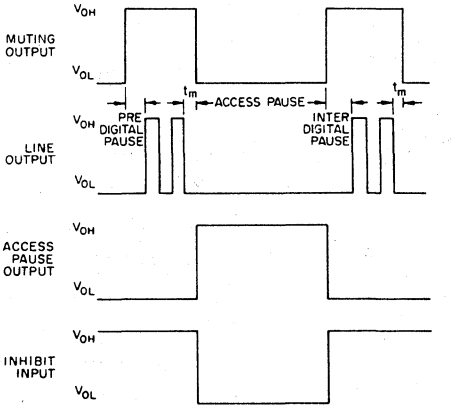


Fig.4 Line, Muting and Access Pause Output Timing



TELECOM

ELECTRICAL CHARACTERISTICS

Maximum Ratings *

Input Voltages (with respect to V_{SS}) . . . . . −20V to +0.3V
Storage temperature. . . . . −65°C to +150°C
Operating temperature . . . . . −25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V T_A = −25°C to +70°C

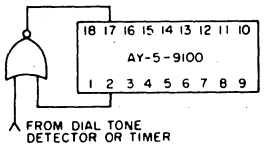
Negative logic conventions are followed for this data sheet.

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
Clocks (see Fig.1)						
Logic '1'	$V\phi_L$	−13.5	—	−16.5	V	
Logic '0'	$V\phi_H$	+0.3	—	−1.0	V	Match clocks within 0.5V
Frequency	f	10	18	30	kHz	See Note 2
Capacitance	$C\phi$	—	90	150	pF	Each clock input, $V\phi$=0V, f=1MHz
Rise Time	t_r	.1	—	8	μs	
Fall Time	t_f	.1	—	4	μs	
Leakage	$I_{L\phi}$	—	—	30	μA	$V\phi$=−16.5, T_A=+80°C
Pulse Width	$t\phi_{PW}$	5	—	40	μs	
Pulse Separation	$t\phi_{PS}$	5	—	40	μs	
All Outputs (Note 3)						
On Resistance (Logic '0')	R_{ON}	—	—	1	kΩ	V_{OH}=−1 volt
Off Leakage (Logic '1')	I_{LL}	—	—	10	μA	V_{OL}=−10V. T_A=25°C
Line Output (See Fig.3)						
Strobe-Line Delay	t_p	—	—	3	ms	
Line-Strobe Delay	t_o	33	—	—	ms	MARK/SPACE=66 2/3–33 1/3 (t_o increases for other MARK/SPACE RATIOS)
Muting Output (See Fig.3, 4)						
Line-Muting Delay	t_m	33	—	—	ms	MARK/SPACE = 66 2/3–33 1/3 (t_m increases for other MARK/SPACE RATIOS)
All Inputs (Except Reset)						
Logic '1'	V_{IL}	−4.0	—	−16.5	V	
Logic '0'	V_{IH}	+0.3	—	−1.0	V	
Leakage	I_{LI}	—	—	1	μA	V_I=−16.5, T_A=25°C
Rise and Fall Time	t_r, t_f	—	—	10	μs	
Capacitance	C_I	—	—	5	pF	V_I=0V, F=1MHz
Keyboard Strobe Input (See Fig.2)						
Pulse Width	t_{KPW}	10	—	—	ms	Effective only when RESET input is at Logic '1'
Reset Input (See Fig.2)						
Logic '1'	V_{IL}	−4.0	—	−16.5	V	
Logic '0'	V_{IH}	+0.3	—	−1.0	V	
Leakage	I_{LI}	—	—	1	μA	Vin=−16.5, T_A=25°C
Capacitance	C_I	—	—	5	pF	Vin=0V, f=1MHz
Fall Time	t_{Rf}	3	—	100	μs	
Delay Time	t_D	3	—	—	ms	After clocks reach full amplitude
Power	—	—	0.9	2	mW	$V\phi$=16.5V

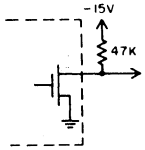
** Typical values are at +25°C and nominal voltages.

NOTES: 2. Line Pulse Rate depends upon frequency of clock input. Standard clock frequency is 18kHz.
3. Outputs require external pull-down resistors (47K typical).

ACCESS PAUSE OPERATION



TYPICAL OUTPUT INTERFACE



TELECOM

Push Button Telephone Diallers

FEATURES: AY-5-9151A

- 2.5V to 5V and 200μA operation, plus standby mode
- Frequency of on-chip clock set by external RC network
- Selectable break: make ratio and interdigital pause
- Uses 3 x 4 matrix keyboard with no keyboard ground or common contact
- Keyboard inputs have antibounce protection
- Input pull-up or pull-down resistors on-chip
- Data entry inhibited and error signal produced if more than one key is pressed
- Redial and access pause controlled from keyboard
- 22 digit capacity including access pauses
- Dialler reset for line power breaks >200ms.

FEATURES: AY-5-9152. Same as AY-5-9151A except:

- Break: Make fixed at 60:40 plus:
- Two antiphase mask outputs for driving bistable relay

FEATURES: AY-5-9153A. Same as AY-5-9151A when in 3 x 4 matrix keyboard mode plus:

- Pin selectable options of 1 of 12 keyboard, 2 of 7 keyboard with common and 4 bit binary with common
- Repertory dialler capability when used with AY-5-9200
- 8 bit output for displaying number in digit store
- Simple call-barring facility using display outputs

FEATURES: AY-5-9154A. Same as AY-5-9153A except:

- Break: Make fixed at 60:40 plus:
- Two antiphase mask outputs for driving bistable relay

DESCRIPTION

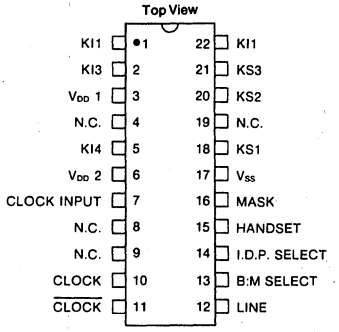
This range of CMOS Pushbutton diallers consists of four devices AY-5-9151A to AY-5-9154A, all of which perform the function of converting input data (e.g. from a keyboard) into a series of pulses suitable for loop disconnect dialling. The series is based on two devices: a simple, basic dialler circuit and a more complex and versatile device which accepts a variety of data entry codes and has a display facility.

The use of CMOS technology results in low voltage and current requirements, enabling easy interfacing with a variety of telephones. The versatility of the devices and the low external component count enables the building of sophisticated, reliable telephones at low cost.

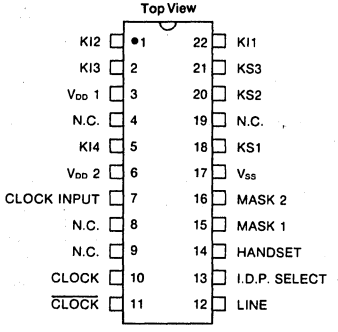
PIN CONFIGURATIONS

22 LEAD DUAL IN LINE

AY-5-9151A*



AY-5-9152*

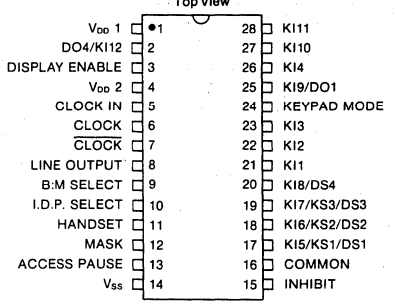


*The AY-5-9151A and AY-5-9156 are also available in 18 lead D.I.L. ceramic packages. Contact factory for pin out.

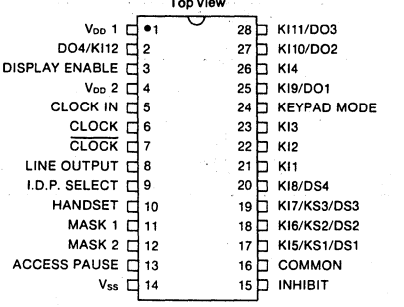
PIN CONFIGURATIONS

28 LEAD DUAL IN LINE

AY-5-9153A



AY-5-9154A



TELECOM

PIN FUNCTIONS

V_{SS} - The negative supply to the device. All voltages are referenced to this pin.

V_{DD1} - The positive supply to the digit store and write counter. Power must be maintained on this pin if the redial function is used.

V_{DD2} - The positive supply to the clock generator and control logic. V_{DD2} should rise to 2.5V withing 20 ms of switch-on.

Clock In, Clock, Clock - These pins are connected to an external RC network which controls the frequency of the clock generator and hence the timing of the line and mask outputs.

Handset Input - The state of the handset is used to control this input, a logic 1 on the input indicating that the handset is on-hook and a logic 0 indicating that the handset is off-hook. This input is used to reset the control logic depending on the past history of the input.

If the input is taken from logic 1 to logic 0, and the clock is not oscillating, a reset pulse is produced when clock pulses are detected. The device is then ready for operation.

If the input is taken to logic 1 for less than 200ms and the clock generator is operating throughout this period, a reset pulse is not produced when the input is taken back to logic 0. Thus short breaks in line power will not affect the operation of the circuit.

If the input is taken to logic 1 for more than 200ms, and clock pulses are present throughout this period, a reset pulse will be generated at the end of the 200ms period.

Line Output - The loop disconnect dial pulses appear at this output. It is an open drain output with the source of the output transistor being connected to V_{SS}. A break period corresponds to this transistor being switched on and a make period or IDP corresponds to the transistor being switched off. The first digit of any outdialling sequence is preceded by a pre-digit pause equal in length to an interdigital pause.

Mask Output/Mask 1 Output - This is a push-pull output and is used to mute the telephone speech circuit. A logic 1 indicates that the speech circuit is to be muted, this occurring immediately on recognition of an input from the keypad.

Mask 2 Output — The AY-5-9152 and AY-5-9154A are fixed at 60:40 Break:Make ratio and a Mask 2 output is substituted for the Break: Make input. The mask 2 output is identical to the mask 1 but is driven in antiphase to enable a bistable mask relay to be used.

On initial application of power, a pulse is produced on Mask 1 and Mask 2 outputs to reset a bistable relay which may be connected to these outputs.

IDP Input - This pin is used to select the duration of the interdigital pause. With a clock frequency of 18kHz, interdigital pauses of 700, 800 or 900ms may be selected. A further option for test purposes enables the IDP to be fixed at 13.3ms and the impulsing rate to be fixed at 600 impulses per second.

Break: Make Ratio — A choice of four break:make ratio is available as a pin programmable option, 70:30, 66.6:33.3, 60:40 and 50:50.

Display Enable - When display data is being output from the dialler, this output goes to a logic 1.

Common Input - When a 4 bit code is used for data input a logic 1 on this input strobes the data into the device. Antibounce protection is provided for this input. A steady logic 1 of less than 5ms duration will not be recognized and a steady logic 1 of greater than 10ms duration will be recognized. This input has a pull down resistor to V_{SS}.

Inhibit Input - This is used to inhibit outdailling. If a logic 1 is placed on this input while a digit is being dialled, outdialling will cease when the digit has been completed. If the logic 1 appears during an IDP, outdialling will cease immediately. When outdialling has ceased, the Mask 1 output goes to logic 0 and Mask 2 goes to logic 1. When the input is taken to logic 0, the Mask signal reappears and dialling continues, starting with an IDP.

Access Pause Output - When an access pause is reached in the dialling sequence, this output goes to a logic 1. By connecting this to the inhibit input, further outdialling will be prevented.

Keyboard Mode - The data on this pin determines whether the device will accept data from:

a) 1 of 12 keyboard with keyboard ground
b) 2 of 7 keyboard with keyboard ground and common switch
c) 4 bit binary code with common signal
d) 4 + 3 matrix keyboard without keyboard ground and common switch

When modes b, c or d are in use with the AY-5-9153A or AY-5-9154A data in the form of two, four-bit words is available for display purposes, except when a key is pressed.

Keyboard Inputs/Keyboard Scans/Display Outputs 1 of 12 Mode - All twelve pins are used as keyboard inputs, on-chip pull-up resistors to logic 1 being incorporated. A logical AND of the twelve inputs produces an on-chip Any Key Down signal when any input is taken to logic 0. Detection of this signal initiates an anti-bounce period and at the end of this period, the data on the twelve inputs is read into the digit store, provided the Any Key Down signal is present throughout this period. Any further data is then inhibited until an antibounce period has been completed with all keys up. If, during the anti-bounce period, the Any Key Down signal disappears, the anti-bounce timer will be reset.

2 of 7 Mode - Keyboard inputs 1-4 are used for the 4-bit data, the common input strobing the data into the digit store. On-chip pull down resistors to logic 0 are incorporated on the four data inputs and the common input. When the common input is taken to logic 1, an antibounce timer is started and if the common input is at logic 1 throughout, the data is read at the end of the period. Further data is then inhibited until the common input has been at logic 0 for an antibounce period.

Binary Mode - The 4-bit word is entered into the digit store via inputs 1-4 by use of the common input, in a similar manner to the 2 of 7 mode. On-chip pull down resistors to logic 0 are incorporated. When data is not being read into the device (i.e. when the common input is at logic 0) these four inputs are used as output pins for a 4-bit word for digit display purposes as described later.

4 x 3 Matrix Mode — This function will be described for the AY-5-9151A and AY-5-9152. The mode of operation is slightly different for the AY-5-9153A and AY-5-9154A, as explained later.

A pulse to logic 0 is sequentially switched around the three keyboard scan outputs, taking 5ms for a complete scan cycle. When a key is pressed the pulse appears on one of the four keyboard inputs 1-4 (provided with pull-up resistors to logic 1), and if it occurs on the same input on the next scan cycle, the data is entered into the digit store. Before a second key depression may be recognized, the first key must be released and a full scan cycle completed without a pulse on any input.

If two keys are pressed during the same scan cycle, the data will be rejected and again a full scan cycle must be completed without a pulse appearing on any of the inputs before another key depression may be recognized.

If a key is pressed during an inhibit period, or two keys are pressed simultaneously, all three scan outputs will go to logic 0 until the key or keys is/are released.

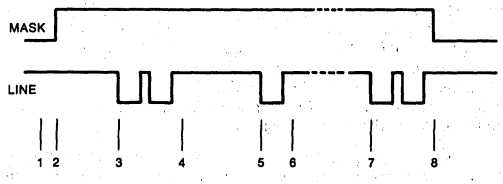
Display Scans/Display Outputs - Data for the first 16 digits and access pauses in the store is available for display.

The position of a digit within a telephone number is indicated by a 4 bit binary word from the Display Scan outputs. Display Scan 1 is the least significant bit and Display Scan 4 is the most significant bit. Binary word 0000 corresponds to the left-hand digit of the display (the first number entered) and 1111 corresponds to the right-hand (16th) digit of the display.

The digit being output is available as a 4 bit word on the display outputs (Display Out 1 = least significant bit). Binary word 0001 represents digit 1 and so on to 0000 = digit 10. Access pauses are represented by 1011.

When in the 2 of 7 mode or the Binary mode, the display data is inhibited by the appearance of the common signal. When in the 4×3 matrix mode, depression of a key causes display scan data to appear on the keyboard inputs. The dialler then reverts to the normal keyboard scanning mode of operation.

LINE AND MASK OUTPUT TIMING



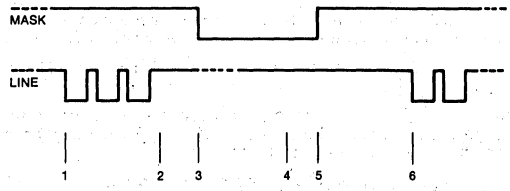
The above sequence of events is that which occurs when the digit store is initially empty. The time intervals quoted in the following explanation are valid only for a clock frequency of 18kHz. The time intervals are inversely proportional to the clock frequency.

	Event	Time Interval
1	The first key is depressed and the anti-bounce timer is started	T_{1-2} = 5-10ms after end of bounce
2	The data from the keyboard is accepted. The mask output appears and the pre-digital pause commences. This is the same duration as the inter-digital pause and is pin selectable.	T_{2-3} = 700, 800 or 900ms
3	Dialling of the first digit starts. The example shown is a digit 2.	T_{3-4} = n × 100ms where n = digit dialled
4	End of 1st digit and start of inter-digital pause.	T_{4-5} = 700, 800 or 900ms
5	Dialling of 2nd digit starts. The example shown is a digit 1.	T_{5-6} = n × 100ms where n = digit dialled
6	End of 2nd digit and start of inter-digital pause.	T_{6-7} = 700, 800 or 900ms

Dialling of further digits continues in a similar manner until the last digit.

7	Dialling of last digit commences, in this case a digit 2.	T_{7-8} = n × 100ms where n = digit dialled
8	End of last digit and end of mask signal.	

EFFECT OF ACCESS PAUSE ON LINE AND MASK OUTPUT TIMINGS



The following time intervals are valid only for a clock frequency of 18kHz.

	Event	Time Interval
1	Dialling of the last digit before the access pause commences. A digit 3 is shown in this example.	T_{1-2} = n × 100ms where n = digit dialled.
2	The end of the last digit before the access pause.	T_{2-3} = 700, 800 or 900ms
3	The mask signal is removed so that the telephone user can listen for the appearance of the second dial tone.	
4	The telephone user presses the # key to release the access pause. The antibounce timer is started.	T_{4-5} = 5-10ms
5	The data from the # key is accepted or the inhibit input is taken to logic 0 and the mask signal reappears. A pre-digital pause equal in length to an inter-digital pause starts.	T_{5-6} = 700, 800 or 900ms
6	The digit after the access pause is dialled out. Dialling then continues as normal.	

Access Pause and Redial Operation

These facilities are available on all devices, control being via the keypad or data input codes. The 1 of 12 keypad and 4 × 3 keypad use the '*' button to insert an access pause and the '#' button to release the access pause.

The '#' button may also be used to redial the number in the digit store. If the redial mode is used, power must be maintained on V_{DD1} at all times.

TELECOM

PIN SELECTABLE OPTIONS

a) Break:Make Ratio

Ratio	Voltage On Pin
70:30	Clock
66.6:33.3	V_{DD}
60:40	V_{SS}
50:50	$\overline{\text{Clock}}$

b) IDP (with 18kHz clock frequency)

IDP	Voltage On Pin
700ms	V_{DD}
800ms	V_{SS}
900ms	Clock
13.3ms	$\overline{\text{Clock}}$

c) Keyboard Mode

Mode	Voltage On Pin
2 of 7	V_{DD}
3 × 4	V_{SS}
1 of 12	Clock
Binary	$\overline{\text{Clock}}$

DATA INPUT CODES

KI = Keyboard Input

Binary

KI 4	KI 3	KI 2	KI 1	Digit
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	Access Pause
1	1	0	0	Redial

2 of 7

KI 1	KI 2	KI 3	KI 4	Digit
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
1	0	0	0	7
1	0	0	1	8
1	0	1	0	9
0	0	1	1	10
1	1	0	0	Access Pause
1	1	0	1	Redial

4-bit codes other than those shown above are ignored.

DATA OUTPUT CODES

Display Scan (DS)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

DS4	DS3	DS2	DS1	Position
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

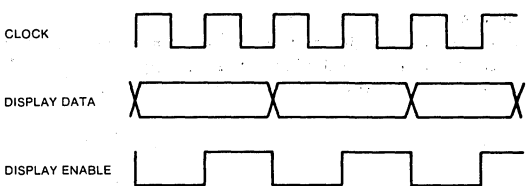
Display Outputs (DO)

DO4	DO3	DO2	DO1	Digit
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
0	0	0	0	0
1	0	1	1	Access Pause

The Display Scan outputs are continuously incremented, and the Display outputs changed accordingly, to enable the display of all the digits in the digit store by the use of multiplexing.

The Display Scan code is incremented at half the clock frequency.

The relationship between Clock, Display Data out and Display enable is as follows.



TELECOM

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... +7.0V to −0.3V
Storage Temperature Range ..... −65°C to +150°C

*Exceeding these ranges could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
$V_{DD1} = V_{DD2}$ = 2.5 V to 5.0V ($V_{DD1} \geq V_{DD2}$)
T_A = −25°C to +80°C

Clock frequency = 18kHz The device will function correctly from 8kHz to 50kHz but all timings (break period, IDP etc.,) will be directly dependent on the clock period.

Characteristic	Min.	Typ.	Max.	Units	Conditions
Inputs					
IDP, B:M, Key Pad Mode					
Logic '0' Level	−0.3	—	0.2	V	
Logic '1' Level	V_{DD2} −0.2	—	V_{DD2}+0.3	V	
All Other Inputs					
Logic '0' Level	−0.3	0	0.5	V	Note 1
Logic '1' Level	V_{DD2} −0.5	V_{DD}	V_{DD2} +0.3	V	
Capacitance	—	—	10	pF	$V_{IN} = V_{SS}$, f = 1MHz
CURRENT SOURCE TO V_{DD2}					
Keyboard Inputs	2	—	60	μA	
CURRENT SINK TO V_{SS}					
Keyboard Inputs Common IDP, B:M	3	—	90	μA	
	0.6	—	15	μA	
Clock In Leakage Current	—	—	20	nA	T_A = +25° C $V_{IN} = V_{SS}$ or V_{DD1}
Key Depression Period	10	—	—	ms	
OUTPUTS					
LINE:					
Logic '0' Output Current	2	—	—	mA	V_O = 1.0V
Logic '1' Leakage Current	—	—	1	μA	V_O = 5.0V
MASK:					
Logic '0' Output Current	2	—	—	mA	V_O = 1.0V
Logic '1' Output Current	2	—	—	mA	$V_O = V_{DD2}$ −1.0V
ALL OTHER OUTPUTS:					
Logic '0' Output Current	0.1	—	—	mA	V_O = 1.0V
Logic '1' Output Current	0.1	—	—	mA	$V_O = V_{DD}$ −1.0V
CLOCK FREQUENCY	17.2	—	18.6	kHz	$V_{DD1} = V_{DD2}$ = 3.75V
	14.3	—	—	kHz	$V_{DD1} = V_{DD2}$ = 2.5V
	—	—	19.5	kHz	$V_{DD1} = V_{DD2}$ = 5.0V
Temperature Stability	—	—	±2	%	Relative to value at +25° C V_{DD2} = 5.0V
	—	—	±5	%	Relative to value at +25° C V_{DD2} = 2.5V
SUPPLY CURRENT					
I_{DD1}	—	—	7	μA	V_{DD1} = 5.0V, V_{DD2} = 0V
I_{DD2}	—	—	200	μA	V_{DD2} = 5.0V, Note 2

NOTES:

1. The device will function correctly with a maximum logic '0' of 1.0V and a minimum logic '1' of V_{DD} −1.0V. However, use under these conditions may result in an increased supply current.
2. Measured with Break: Make, IDP, Inhibit and Keyboard Mode inputs at V_{SS}, and with no keys depressed.

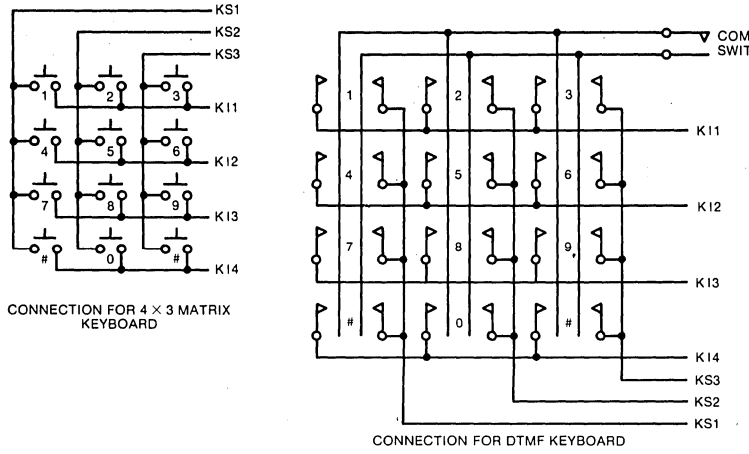


Fig. 1 KEYBOARD CONNECTIONS FOR AY-5-9151A & AY-5-9152

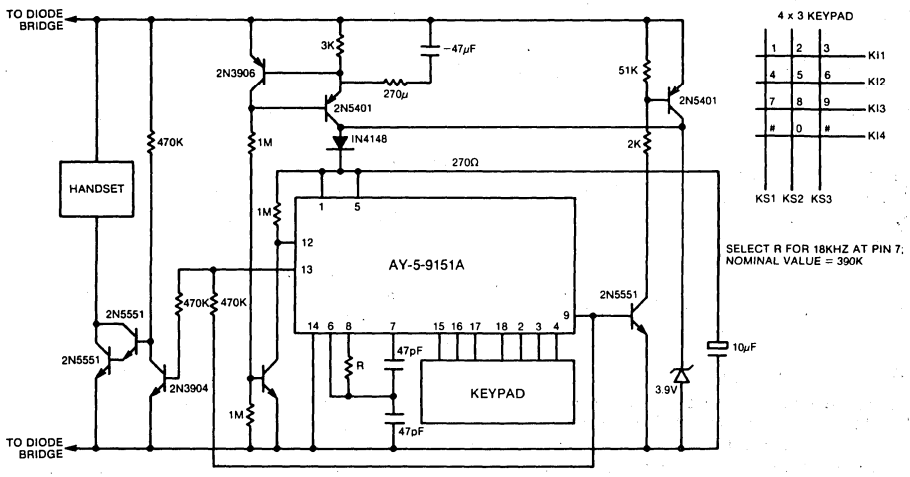


Fig. 2 PROVISIONAL PUSH-BUTTON DIALLER CIRCUIT USING AY-5-9151A

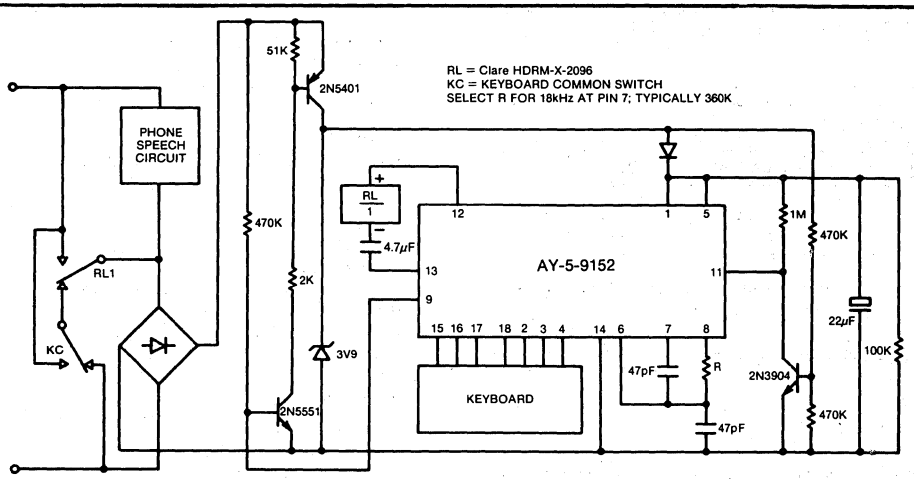


Fig. 3 PUSHBUTTON DIALLER USING MASK RELAY

Loop Disconnect Dialler

FEATURES

- 2.5 to 5.0V supply voltage
- Low power standby mode for redial
- On-chip clock generator
- 4 × 3 matrix single contact keypad
- Pin selectable IDP
- On-chip input pull up/down devices
- Redial and access pause controlled from keypad
- 22 digit capacity including access pauses
- Plastic or Ceramic package

DESCRIPTION

The AY-5-9158 is a CMOS loop disconnect dialler with full access pause and redial capabilities, featuring pin-programmable Interdigital Pause. The use of a low voltage CMOS process realizes well known advantages of low power and high noise immunity, particularly desirable features in a loop disconnect telephone dialler.

PIN FUNCTIONS

V_{ss}

This should be connected to the negative terminal of the power supply to the dialler. Voltages on all other pins of the dialler are normally referenced to this pin.

V_{dd}

This should be connected to the positive supply of the dialler. If the redial facility is required, power must be maintained on this pin when the handset is on-hook

Clock Input, Clock and Clock

The clock pulse generator consists of two inverters, the frequency of oscillation being controlled by external components connected to these three pins. The circuit is sufficiently versatile to allow the use of a variety of external component configurations. Figure 1 shows the configuration used throughout this data sheet. Details of the performance of this circuit are given in the section describing electrical characteristics.

IDP Select

The signal applied to this pin controls the duration of the interdigital pause as follows:

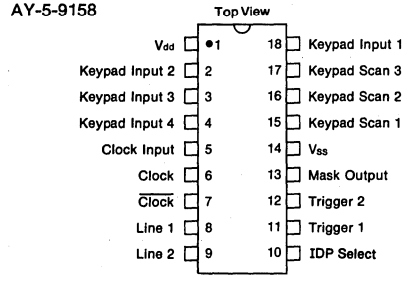
Voltage on Pin	IDP
V_{SS}	800ms
Clock	500ms

The pin may also be connected to CLOCK. This increases the keypad scan frequency and outdialling frequency by a factor of 15 to facilitate high speed testing of the device. The data on this pin is read during a reset controlled by the Trigger 1 input. This pin has an on-chip pull down device to V_{SS}.

Line 1 and Line 2 Outputs

The loop disconnect dial pulses appear at these outputs. The ouput stage is a push-pull type with separate pins for the drains of the output transistors as shown in Figure 2. During a dial pulse break period, the N channel device is off and the P channel device is on, creating a logic 1 at the Line 2 output. During a make period and an IDP the N channel device is on and the P channel device is off, creating a logic 0 at the Line 1 output. The timing of the Line 1 output relative to the Mask output is shown in Figure 3. The Break:Make ratio is fixed at 66.7:33.3.

PACKAGE INFORMATION
PIN CONFIGURATION
18 LEAD DUAL IN LINE
AY-5-9158



Mask Output

This is a push-pull output and is used to control the muting of the telephone speech circuit during dialling. A logic 1 indicates that the telephone is to be muted, the transition to logic 1 occurring immediately on recognition of a key depression.

Keypad Scans 1-3

These are push-pull outputs used to scan the keypad columns at a rate of 200Hz. Figure 4 shows how these outputs are connected to the keypad.

Keypad Inputs 1-4

The keypad contacts are used to connect one keypad scan output to one keypad input to enable recognition of a key depression. Each of these inputs has an on-chip pull up device to V_{dd}. For a description of how the keypad inputs recognize data, see Section 2.

Trigger 1 and Trigger 2

These are connected to the input and output respectively of two inverters in series as shown in Figure 5. Connection of resistors R1 and R2 allows a Schmitt trigger circuit to be realized, the switching thresholds being determined by the values of these resistors. The characteristic of the Schmitt trigger is shown in Figure 6. If the input voltage V_T is lower than the lower threshold V_{TL}, the clock generator is stopped and the scan outputs become high impedance. In this state the dialler consumes only a small leakage current and data in the RAM is maintained. If V_T is increased and exceeds V_{TH} the clock generator is started, the read and write counters are reset and a pulse appears at the Mask output as shown in Figure 7. The duration of the pulse is 16-19ms for a clock frequency of 18kHz.

ELECTRICAL CHARACTERISTICS

Maximum Ratings

Permanent damage may result if these ratings are exceeded.
Functional operation is not guaranteed under these conditions.
Voltage on any pin with respect to V_{SS} ..... +7.0 to −0.3
Storage temperature range ..... −65°C to +150°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

V_{SS} = 0.0V
V_{DD} = 2.5V to 5.0V
Ambient temperature = −25°C to +80°C
Clock frequency = 18kHz nominal (set by components shown in Fig. 1)

Characteristics	Min	Typ	Max	Units	Conditions
Supply Current					
I_{DD}	—	—	7	μA	V_{dd} = 5.0, V_{TL} = 0.0
	—	90	240	μA	V_{dd} = V_{TL} = 5.0V Note 1.
Inputs					
KEYPAD SCANS:					
Logic '0'	−0.3	—	0.5	V	
Logic '1'	V_{DD}	—	V_{DD}	V	
	−0.5	—	+0.3	V	
IDP:					
Logic '0'	−0.3	—	0.2	V	
Logic '1'	V_{dd}	—	V_{dd}	V	
	−0.2	—	+0.3	V	
V_{TH}	1.98	—	2.34	V	V_{DD} 3.6V, with specified Values of R1 and R2.
V_{TL}	1.26	—	1.62	V	Note 2.
CURRENT SOURCE TO V_{DD}:					
Keypad Inputs	2	—	60	μA	V_{IN} = V_{SS}
CURRENT SINK TO V_{SS}:					
IDP	0.6	—	15	μA	V_{IN} = V_{DD}
LEAKAGE CURRENT:					
Trigger 1, Clock 1	—	—	20	nA	T_A = +25°C, V_{IN} = V_{DD} or V_{SS}
Outputs					
MASK:					
Logic '0' Output Current	2	—	—	mA	V_O = 1.0V
Logic '1' Output Current	2	—	—	mA	V_O = V_{dd} −1.0V
LINE 1:					
Logic '0' Output Current	2	—	—	mA	V_O = 1.0V
Logic '1' Leakage Current	—	—	1	μA	V_O = V_{DD}
LINE 2:					
Logic '0' Leakage Current	—	—	1	μA	V_O = V_{SS}
Logic '1' Output Current	2	—	—	mA	V_O = V_{DD} −1.0V
KEYPAD SCANS, Trigger 2:					
Logic '0' Current	100	—	—	μA	V_O = 1.0
Logic '1' Current	100	—	—	μA	V_O = V_{DD} −1.0V
Clock Frequency	17.2	—	18.6	kHz	V_{DD} = 7.75V
	14.3	—	—	kHz	V_{DD} = 2.5 T_A = +25°C
	—	—	19.5	kHz	V_{DD} = 5.0
Clock Frequency Temperature Stability	—	—	±2	%	Relative to value at V_{DD} = 5.0V
	—	—	±5	%	Relative to value at V_{DD} = 2.5

NOTES:
1. Measured with IDP at V_{SS}, Keypad Inputs at V_{DD} and all outputs open circuit.
2. Values of R1 and R2 yet to be defined.

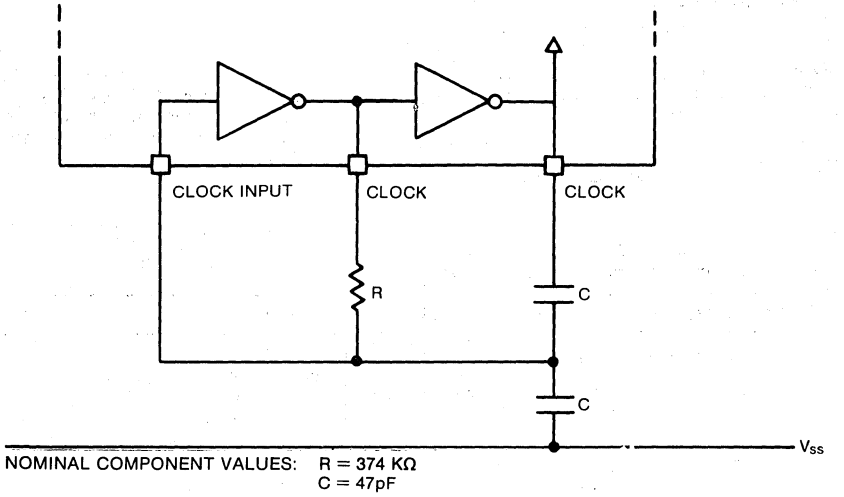


Fig. 1

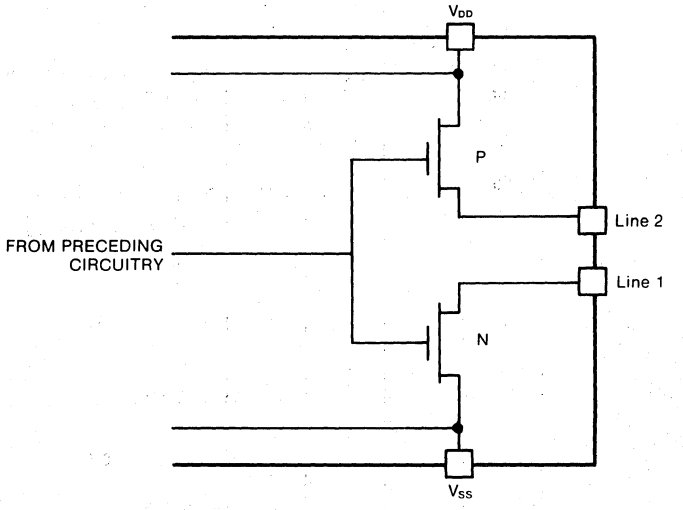
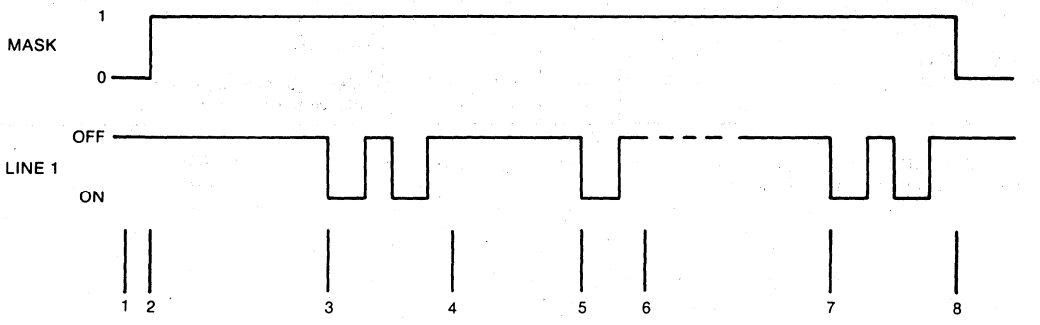


Fig. 2



The above sequence of events is that which occurs when the digit store is initially empty. The time intervals quoted in the following explanation are valid only for a clock frequency of 180kHz. The time intervals are inversely proportional to the clock frequency.

Fig. 3

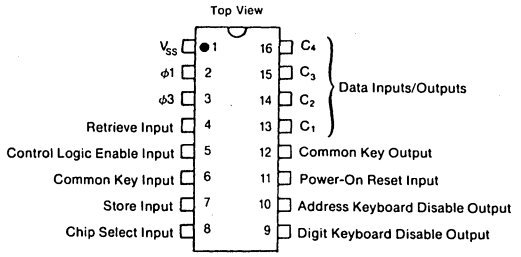
Repertory Dialler

FEATURES

- Stores 10 x 22 digit telephone numbers, including access pauses
- Devices can be 'stacked' to give a store expandable in blocks of 10 numbers
- Operates in conjunction with the AY-5-9100 Push-Button Dialler
- Single or Dual Keyboard operation
- Interfaces to standard MF Tone Dialler Keyboards
- Applications in Repertory Diallers and Security Systems
- Will operate MF Tone Diallers such as the AY-3-9400
- Low power consumption, typically 2.25mW

PIN CONFIGURATION

16 LEAD DUAL IN LINE



DESCRIPTION

The AY-5-9200 is a 10 number store designed to work in conjunction with the AY-5-9100 Push Button Telephone circuit to form a Repertory Dialler, each of the 10 numbers containing up to 22 digits or access pauses.

The keyboard, AY-5-9100 and as many AY-5-9200's as required are all connected to a 4 line data bus. Numbers for direct dialling are routed to the AY-5-9100, numbers to be stored go straight to the AY-5-9200. Numbers that are being retrieved are transmitted from the AY-5-9200 to the AY-5-9100 while control outputs from the AY-5-9200 determine the routing of the data.

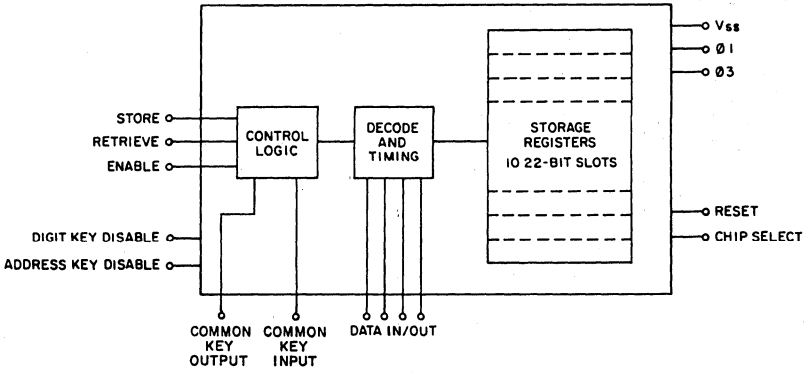
The system may operate either with a single 12 button keyboard, which is used for both address and digit entry, or with separate address and digit keyboards. Single keyboard operation would normally be employed in a 10 number Repertory Dialling telephone. Dual keyboard operation is usual for 10 to 100 number Repertory Diallers.

The AY-5-9200 may also be used in MF tone dialling systems, the output data rate being directly compatible.

Four phase logic is used to achieve minimum power consumption, the circuits being manufactured using the MTNS P-channel nitride MOS process.

TELECOM

BLOCK DIAGRAM



Pin.No.	Name	Function
1	V_{SS}	This is the ground and substrate connection and is used as a reference for all the electrical parameters.
2-3	Clocks $\phi 1, \phi 3$	These inputs form the two supply clocks, and alternate negative-going pulses are required. These are described in the Electrical Characteristics and fig. 1. Any deviation from the nominal 18KHz will result in a proportional modification of the on-chip timings.
4	Retrieve Input	The retrieve input must be taken to a logic '1' for at least 10ms to indicate when a retrieve operation is to be performed. Anti-bounce logic is provided on this input.
5	Control Logic Enable Input	This input must be taken to a logic "1" for the duration of any store or retrieve operation. The control logic is reset when the input returns to logic '0'. Anti-bounce is provided for this input.
6	Common Key Input	This input is taken from the common contact on all keyboards. A '1' to '0' transition will indicate a key closure. Anti-bounce is provided to ensure only a single depression is read.
7	Store Input	This input must be taken to a logic '1' for the duration of any store operation. Anti-bounce logic is provided for both logic transitions.
8	Chip Select Input	When at logic '0' all inputs and outputs (except for Common Key input and output) are inhibited. It may be permanently wired to logic '1' if only one AY-5-9200 is used in the system.
9	Digit Keyboard Disable Output	The digit keyboard must be disabled while information is being transferred from the Store chip to the Push Button Dialler during a Retrieve operation. This output goes to a logic '0' during this period. In a single keyboard system this output is the one to be used.
10	Address Keyboard Disable Output	The address keyboard is to be disabled, both during a Retrieve operation when information is being transferred between chips and during the Store operation after an address has been allocated, until the Store operation is finished. This output goes to a logic '0' during these periods.
11	Power-On-Reset Input	An initial reset is required for clearing the chip when power is initially applied. This input must be held at a logic '0' initially, going to a logic '1' to activate the chips.
12	Common Key Output	This output is fed directly to the Common Key input of the associated AY-5-9100 Push Button Dialler and goes to a logic '0' to indicate a valid code signal. It controls the routing of data into the AY-5-9100. (See Function Description for further details.)
13-16	C_1 C_2 C_3 C_4	Data Input/Outputs. These four lines are connected to the system. Address and dialled digit information is input on these pins and dialling information is fed out from these pins to the Push-Button Dialler. The standard keyboard code accepted by the AY-5-9200 is shown below. When outputting information, the output is normally at a logic '1' and goes to a logic '0' for a data bit.

NOTE:
Chip Select, Retrieve, Control Logic Enable and an address can all be applied simultaneously to the Store Chip. Also Store and Control Logic Enable signals can be applied simultaneously.

KEYBOARD CODE

Digit	No. of Impulses	Code			
		C_1	C_2	C_3	C_4
1	1	1	1	1	1
2	2	1	1	1	0
3	3	1	1	0	1
4	4	1	0	1	1
5	5	1	0	1	0
6	6	1	0	0	1
7	7	0	1	1	1
8	8	0	1	1	0
9	9	0	1	0	1
0	10	1	1	0	0
Access Pause		0	0	1	1

FUNCTION DESCRIPTION

The following description applies to a Push Button Repertory Dialler using the AY-5-9100 and AY-5-9200 circuits. The system provides normal push button telephone facilities with access pause and redialling, together with a repertory dialling store expandable in blocks of 10 numbers.

The AY-5-9100 is a standard Push Button Dialler circuit with normal dialling and redialling facilities. It also has the capability of storing access pauses and waiting until a dial tone is detected by external circuitry before dialling is recommenced. This chip can operate by itself when a storage facility is not required. A detailed description of this device is contained in the AY-5-9100 data sheet.

The AY-5-9200 contains all the control logic and store facility required to store ten telephone numbers. Each number may be up to 22 characters in length, each character being either a digit or access pause; a dynamic memory technique being used for the data storage. Digits, access pauses and memory addresses are entered into the AY-5-9200 as 4-bit codes on 4 input/output pins which are also connected to the digit input pins of the AY-5-9100 as in Figs.4 and 5. While data is being transferred between the AY-5-9200 and the AY-5-9100, the keyboards are externally disabled by signals generated by the AY-5-9200, so that further key depressions have no effect until the transfer of data has been completed. Further address inputs are inhibited until the call is terminated.

The digit keyboard common key output is routed through the control logic and depending on the state of the logic, the Common Key output to the Push Button Dialler chip is enabled or disabled. This prevents digits to be stored and memory addresses from entering the Push Button Dialler.

The Common Key output from the AY-5-9200 is controlled as follows:

	C.S.	C.L.E.	
Logic Level	'0'	'0'	Common output is a direct replica of Common input and digits are dialled directly by the AY-5-9100
Logic Level	'1'	'1'	Common signals to the Push Button Dialler are generated only as a number is being retrieved (see Fig. 3). After a retrieve operation, Common signals are gated through, allowing further dialling unless externally inhibited.
Logic Level	'0'	'1'	No Common signals are generated and the output device goes off.

The control logic operates so that the first key depression at the beginning of an operation determines the subsequent sequence. Invalid key depressions at a later stage in a sequence are then ignored by the control logic.

The system is expanded by connecting further AY-5-9200 chips to the busses and using the Chip Select input to enable the required chip.

When a separate address keyboard is to be used an address keyboard strobe can be fed to the 'Retrieve' input, thus allowing a single button depression when retrieving a number from the store.

OPERATION MODES

1. STORE OPERATION

DEPRESS STORE

This sets the logic into a store mode. This signal must be present throughout the store operation. Thus, either electrical or mechanical bistable switching is required, or the 'Store' button must remain depressed during the sequence. The Control Logic Enable and Chip Select inputs should be activated at the same time. The Common Key output is inhibited and the address and digit codes are routed into the AY-5-9200 chip. The order of application of the signals is not important, they may be applied simultaneously with Address if required.

DEPRESS ADDRESS (one digit)

The address code, if valid, is latched and the memory location associated with this address is cleared to prevent corrupting the new number with old information. The Common Key output remains disabled. The Address Keyboard is also disabled for the remainder of the Store operation.

ENTER NUMBER DIGITS (and Access Pauses)

The number to be stored is then entered using the digit keyboard, and is stored in the addressed location. The maximum allowable number of digits or access pauses is 22. Chip select must be at logic '1' during digit entry.

RELEASE STORE, CONTROL LOGIC ENABLE AND CHIP SELECT

This is accomplished by re-setting the electrical or mechanical bistable or releasing the Store button. The control logic is then reset and disabled.

2. RETRIEVE OPERATION

DEPRESS RETRIEVE

For separate address keyboard systems, this signal can be generated automatically with the address. The control logic is set in a retrieve mode and the address inputs are enabled. Control Logic Enable and Chip Select must be at logic '1' for the whole of the Retrieve operation, including the data transfer period. The Retrieve input must be returned to logic '0' before the end of data transfer to prevent a repeat operation.

DEPRESS ADDRESS (Digit)

The address is decoded and latched, both keyboard disable outputs go active, disabling the keyboards. After a minimum period of 60ms, the first digit code is transmitted to the Push Button Dial chip together with a Common signal. The Common is stable for a minimum period of 60ms, the Common only being present while the code is stable. The data transmission continues at 60ms on, 60ms off until the whole number has been transferred after which the chip is reset, the keyboard disable signals are removed and the Common signal is enabled to the Push Button Dialler chip. (See Fig. 3.)

3. ERASE OPERATION

This operation is basically a Store operation with no digits being input.

DEPRESS STORE

This sets up the logic as in the Store operation.

DEPRESS ADDRESS (Digit)

This then clears the decoded address.

RELEASE STORE

This is accomplished either by releasing 'Store' input, or resetting the mechanical or electrical 'Store' bistable.

4. RECALL AND NORMAL DIALLING

These are performed as for the Push Button Dialler on its own. See AY-5-9100 data sheet for full description.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} . . . . . −20V to +0.3V
Storage temperature range. . . . . −65°C to +150°C
Ambient operating temperature range . . . . −55°C to +80°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
$V\phi$ = −15±1.5V (see Fig. 1 for waveform)
Clock frequency = 18kHz
Operating Temperature (T_A) = −55°C to +80°C
Negative logic conventions are followed for this data sheet.

Characteristic	Min.	Typ.**	Max.	Units	Conditions
Clock					
Logic '0' level	+0.3	—	−1	V	Note 1
Logic '1' level	−13.5	—	−16.5	V	
Frequency	10	18	30	kHz	
Rise Time (Tr)	0.1	—	4	μs	
Fall Time (Tf)	0.1	—	8	μs	
Width (Tw)	5	—	40	μs	At logic '1' min. level
Separation (Ts)	5	—	40	μs	At logic '0' max. level
Capacitance	—	70		pF	Per phase $V\phi$ = 0V, f = 1MHz(Note 2)
Leakage	—	—	10	μA	$V\phi$ = 16.5V, T_A = 25°C
Inputs					
Logic '0' level	+0.3	—	−1	V	
Logic '1' level	−5	—	−16.5	V	
Capacitance	—	—	5	pF	V_{IN} = 0V, f = 1MHz
Leakage	—	—	1	μA	V_{IN} = −16.5V, T_A = 25°C
Common Key Input					
Pulse Width (Tc)	10	—	—	ms	At logic '0' max level see fig. 2
Reset Input					
Pluse Width (Td)	3	—		ms	After clocks reach full amplitude
Fall Time (Te)	—	—	100	μs	Fig.2
Anti-bounce on all Inputs except Chip Select & Reset	4.2	—	—	ms	
Outputs					
All outputs including C_1 to C_4 when acting as outputs					
Logic '0' output current	0.6	—	—	mA	V_0 = −1V
Logic '1' output leakage	—	—	10	μA	V_0 = −10V
Digit Output Rate	—	8.35	—	Hz	
Power	—	2.25	—	mW	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. Clock logic '0' levels should be within 0.5V of each other.
2. The effective dynamic clock capacitance while operating is 260pF.

TIMING DIAGRAMS

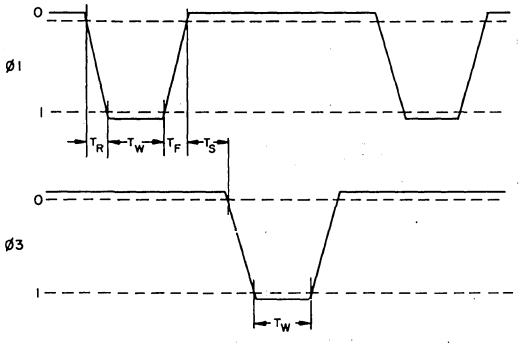


Fig.1 CLOCK WAVEFORMS

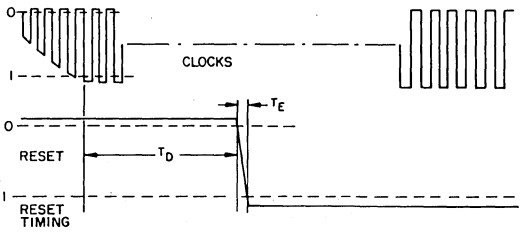


Fig. 2 CLOCK WAVEFORMS WITH RESET TIMING

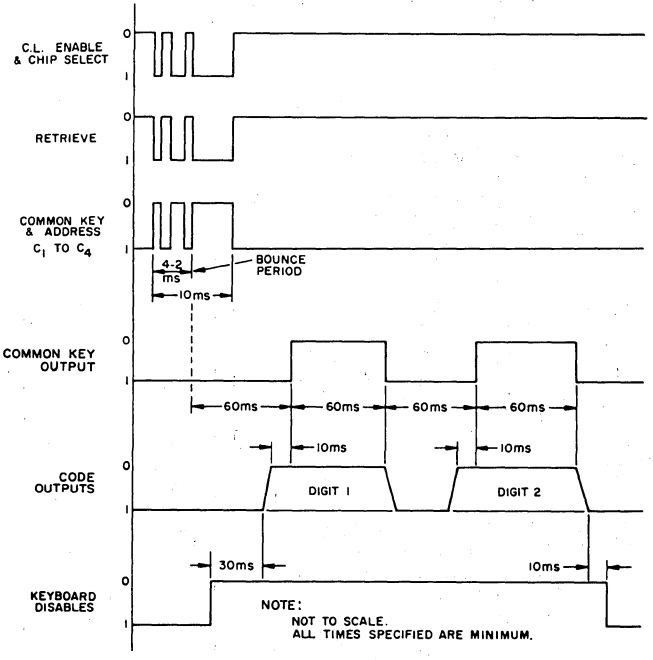


Fig. 3 "RETRIEVE" WAVEFORMS

TELECOM

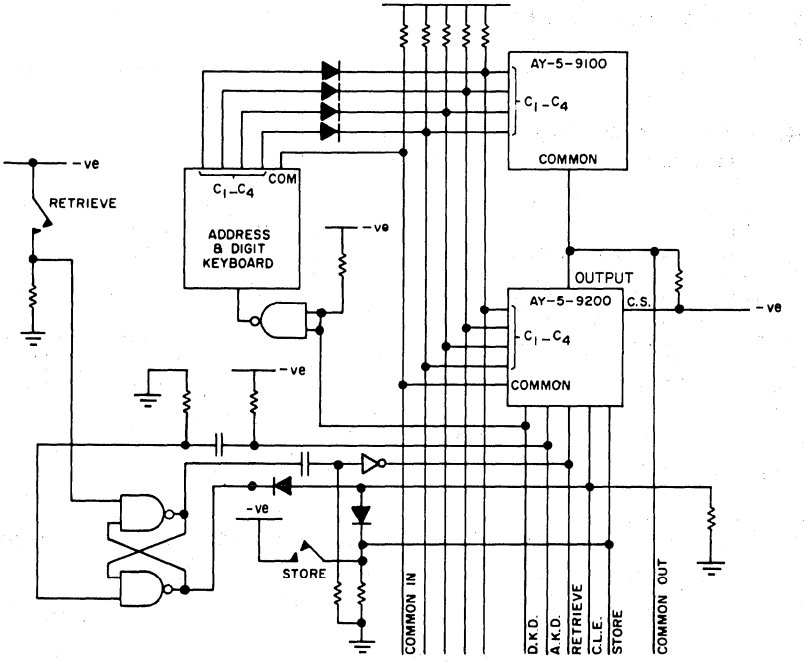


Fig.4 SINGLE KEYBOARD SYSTEM FOR REPERTORY DIALLER

Note for Figs.4 and 5
Logic: CD4011A (C-MOS)
Resistors: 100K
Capacitors: 0.1uF
Diodes: 1N914

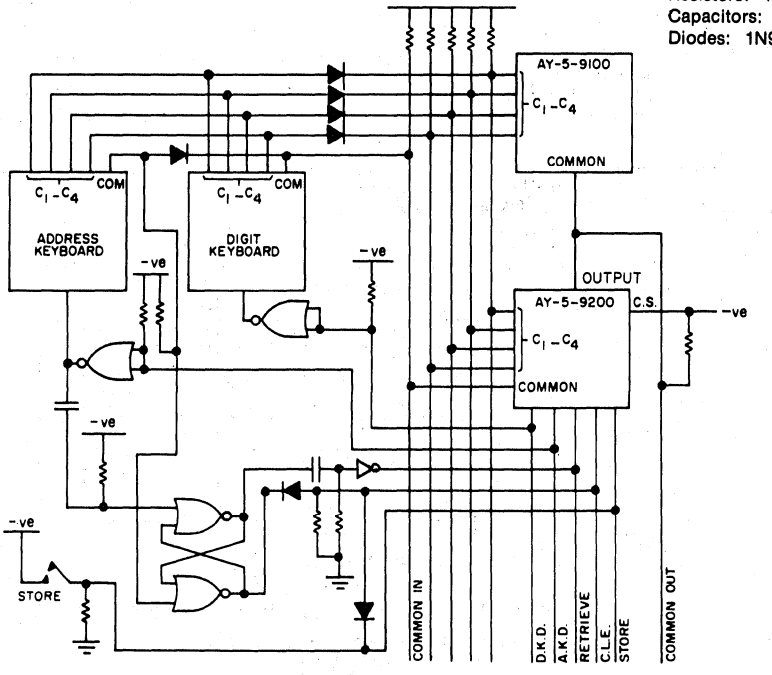


Fig.5 DUAL KEYBOARD SYSTEM FOR REPERTORY DIALLER

Dual Tone Multi-Frequency Generators

FEATURES

- No tuning required, inherent accuracy ± 0.25%
- Uses low cost ceramic resonator
- 12 tone pairs (16 tone pairs with AY-3-9401/9410 and choice of high group pre-emphasis with AY-3-9410)
- Total harmonic distortion less than 8% (but dependent on external filter)
- Instant generation of tone outputs
- Low voltage drop
- Low power consumption (less than 35mW)
- Good thermal and voltage stability
- Keyboard lock out inhibits output if more than one key depressed
- N-channel ion implant construction
- High group pre-emphasis fixed at 3.52dB (AY-3-9400), 2dB (AY-3-9401), 3/6dB (AY-3-9410)
- Pre-emphasis can be varied by simple component adjustment.

DESCRIPTION

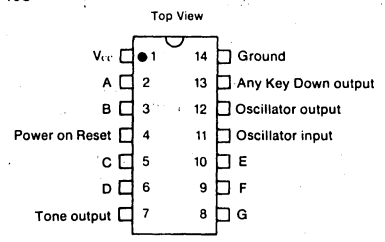
The AY-3-9400/9401/9410 DTMF circuits generate all the tone pairs required for multifrequency tone dialing. The tones are generated from a single ceramic controlled master oscillator, ensuring high accuracy and stability of the output frequencies and eliminating the need for any adjustments. The digitally synthesized tones give precisely controlled characteristics.

The AY-3-9400/9401/9410 is fabricated using the ion implant N-channel low voltage process, and employs novel logic techniques to minimize power consumption and voltage drops. The circuit is suitable for operation direct from telephone line power, or it can be used with main power or battery supplies.

PIN CONFIGURATION

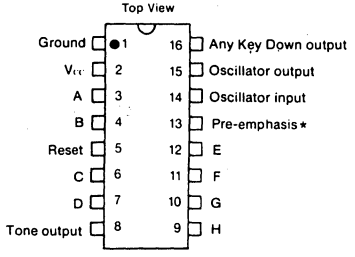
14 LEAD DUAL IN LINE
AY-3-9400

Top View



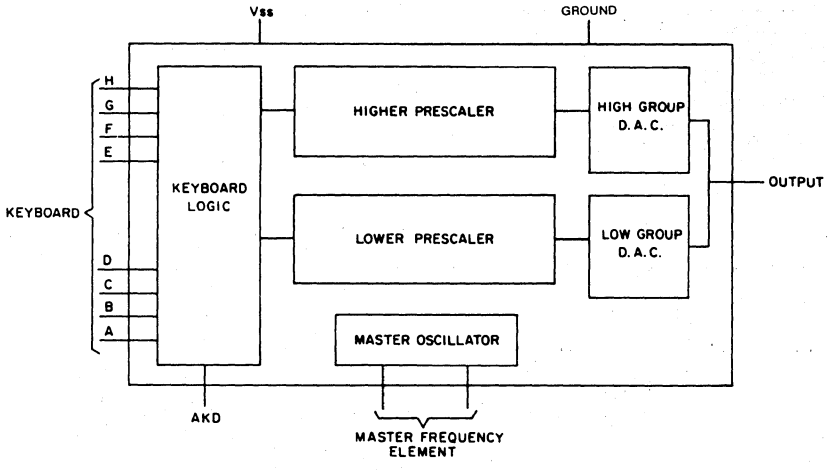
16 LEAD DUAL IN LINE
AY-3-9401/AY-3-9410

Top View



*2dB on AY-3-9401, 3/6dB on AY-3-9410.

BLOCK DIAGRAM



AY-3-9401/9410

TELECOM

OPERATION

When a key is pressed the chip will immediately start operating, the output tones both starting from zero on the first negative half cycle. The first cycle will be of full amplitude assuming the power supply is at the correct level. If power is applied at the same time as a key is pressed, the power on reset circuit will operate, preventing spurious outputs.

When two or more keys are pressed together, one or both tones will be switched off. The tones will start from zero as soon as the extra keys have been released. When all keys are released, the tone outputs will immediately cease.

If only one key contact is made, a single tone corresponding to the closed contact will be output. The "Any Key Down" output, which requires a pull-up resistor (typ. 47K), goes to logic '0' as soon as a key depression is recognized.

The tones are output on a single pin, as a mixture of pulse width modulated, constant amplitude square waves. This output signal is constructed into resultant sine waves in the external low pass filter. The approximation chosen yields a total harmonic distortion of less than 8%.

The amplitude of the output signal is directly proportional to the V_{CC} supply voltage.

A low pass filter buffer amplifier is used to remove switching noise and interface the tones to the line. There is an option of either a low impedance or a high impedance output for interfacing to telephone lines. The low impedance circuit is shown in Fig. 1; the high impedance circuit is shown in Fig. 2.

NOTES:

1. Pre-emphasis selection for the AY-3-9401: Connect pin 13 to ground for 2dB pre-emphasis, Pre-emphasis selection for the AY-3-9410: Connect pin 13 to Vcc for 3dB high group pre-emphasis, or to ground for 6dB pre-emphasis. The circuits are otherwise identical in operation to the AY-3-9400.
2. See MFO2 specification for the resonator (for reference, the MFO2 specification is reproduced in Fig. 4).

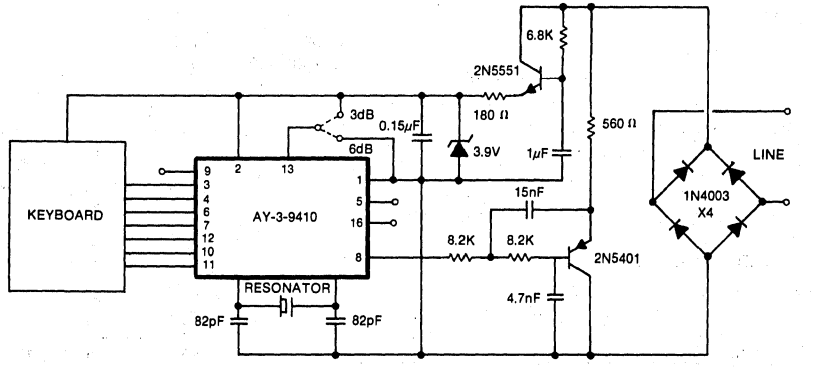


Fig. 1 LOW IMPEDANCE INTERFACE CIRCUIT

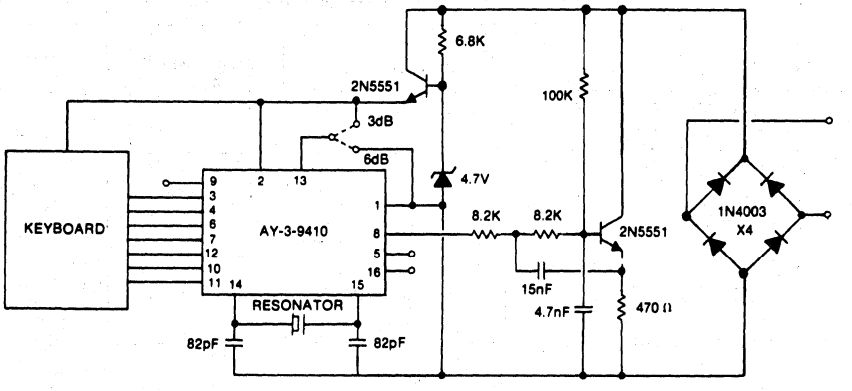


Fig. 2 HIGH IMPEDANCE INTERFACE CIRCUIT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to ground pin . . . . +10V to —0.3V
Storage temperature range . . . . . —65°C to +150°C
Ambient operating temperature range. . . . . -25°C to -70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +3.5 to +8V
F Clock=559.7kHz
Operating Temperature (T_A) -25°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Input Logic '1'	+3.3	—	+8	Volts	Logic '1' activates tone
Input Logic '0'	—0.3	—	+0.4	Volts	
Input pull down resistance	20	—	100	kΩ	Resistor to ground
Input capacitance	—	—	10	pF	
Tone output Low Group	—	0.312	—	V_{peak}	V_{CC} = 4V, Note 1, Note 4
Tone output High Group	—	0.486	—	V_{peak}	V_{CC} = 4V, Note 1, Note 4
High group pre-emphasis	—	3.52	—	dB	1.6dB typ. for AY-3-9401.
Output impedance	—	—	500	Ω	Note 2, Note 3
Any Key Down output					
On resistance	—	—	1	kΩ	Vout = +1V
Off Leakage	—	—	10	μA	Vout = +8V
Total Distortion	—	—	—23	dB	Note 4
Harmonic component	—	—	—30	dB	Note 4
Supply current	—	—	8	mA	V_{CC} = +3.5V
	—	—	10	mA	V_{CC} = +8V

**Typical values are at +25°C and nominal voltages.

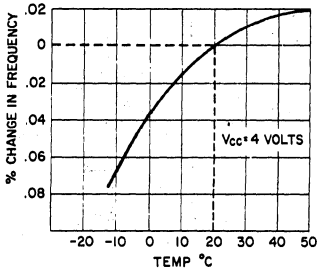
NOTE:
1. The amplitudes of the output signals are directly related to the V_{CC} supply voltage.
2. The chip output is intended to drive a low pass filter having an input impedance of greater than 8K.
3. The output would be buffered to drive the line, the buffer can be arranged to have either a high impedance current output or a low impedance voltage output (See Fig. 1).
4. Output parameters determined by Test Circuit (See Fig. 2).

FREQUENCY OUTPUTS

All output frequencies are derived from a 559.7kHz master oscillator.
The output frequencies are as follows:

	Nominal frequency Hz	Actual Frequency Hz	Error %	Key
Low Group	697	695.28	-0.25	A
	770	768.82	-0.15	B
	852	850.61	-0.16	C
	941	940.68	-0.03	D
High Group	1209	1211.48	+0.21	E
	1336	1332.62	-0.25	F
	1477	1480.69	+0.25	G
	1633	1631.78	-0.07	H

TYPICAL CHARACTERISTIC CURVES



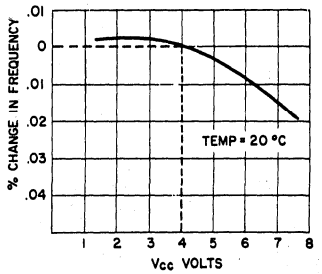


Fig.3 OSCILLATOR CHARACTERISTICS

C-MOS Clock Generator

FEATURES

- Generates 2 phase clock from single power supply
- Operates with AY-5-9100 Push Button Dialler and AY-5-9200 Repertory Dialler
- Very Low power consumption, allowing use of line powered telephones
- Minimizes external components in Push Button Telephones
- Stable generation of clock frequencies

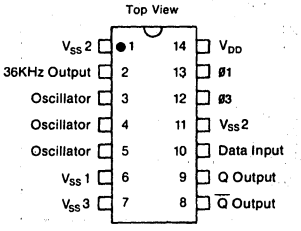
DESCRIPTION

The AY-5-9500 is a C-MOS circuit designed to generate the 2 phase clock required by the AY-5-9100 series of Push Button Telephone Diallers and the AY-5-9200 Repertory Dialler circuit.

It consists of an RC oscillator, a level shifter, a 2 phase clock generator and driver, and a clocked D-type bistable. The RC oscillator is set by external components to run at 36kHz and is normally operated from a −4 Volt supply to minimize power consumption. The oscillator output is shifted and used to drive the 2 phase clock generator. The D-type bistable is either used as a Reset generator for the AY-5-9100 or AY-5-9200 or it is used to drive a Cockroft-Walton voltage multiplier to generate the nominal 15 Volt supply for the AY-5-9100 and AY-5-9200.

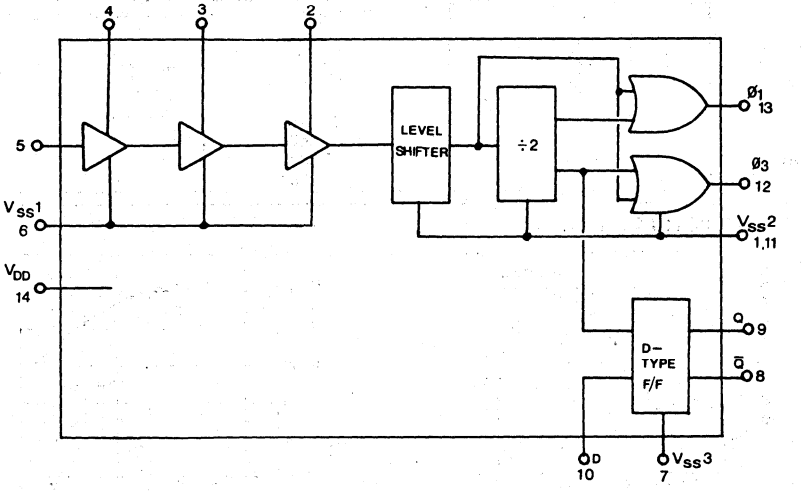
PIN CONFIGURATION

14 LEAD DUAL IN LINE



TELECOM

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{DD} pin .....−15V to +0.3V
Storage temperature range ..... −65°C to +150°C
Ambient operating temperature range .....−25°C to +70°C
Output Current .....7mA per output

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

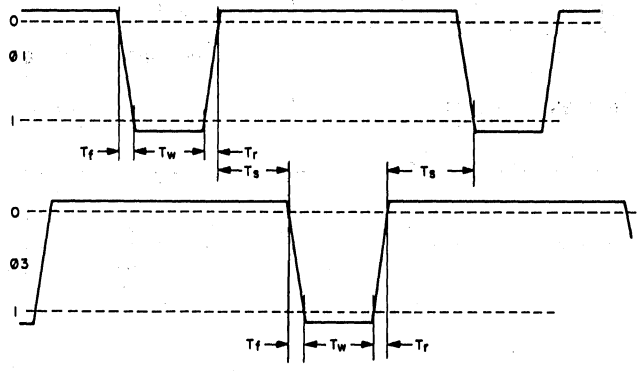
$V_{DD} = 0V$
$V_{SS}1 = -3.8V$ to $-8.5V$
$V_{SS}2 = -3.8V$ to $-15.0V$
$V_{SS}3 = -3.8V$ to $-15.0V$
F Clock = 36kHz ± 10%
Operating Temperature (T_A) = +25°C

Characteristic	Min.	Typ.**	Max.	Units	Conditions
Clock Outputs					
Frequency at pin 12	15.8	18.0	20.2	kHz	$V_{SS} = 4.0V$, $T_A = +25°C$, Note 1, Fig 1.
Frequency stability	−5		+8	%	$V_{SS}1 = -4.0V$, $T_A = +25°C$, Fig. 2.
Rise Time (T_R)	–	–	700	ns	$V_{SS}2 = -3.8V$
	–	120	250	ns	$V_{SS}2 = -15V$ } At 360 pF
Fall Time (T_F)	–	–	600	ns	$V_{SS}2 = -3.8V$ } load/phase
	–	90	200	ns	$V_{SS}2 = -15V$
Width (T_W)	10	–	–	μs	} Fig. 1
Separation (T_S)	10	–	–	μs	
Input Leakage	–	–	20	nA	$T_A = +25°C$, Fig. 3
Output Current-Logic "0" (High)					
Pin 2	0.5	–	–	mA	
ϕ 1, ϕ 3	0.5	–	–	mA	} $V_{OUT} = -0.5V$
Q, $\overline{Q}$	0.8	–	–	mA	
Output Current-Logic "1" (Low)					
Pin 2	0.5	–	–	mA	
ϕ 1, ϕ 3	0.5	–	–	mA	} $V_{OUT} = +0.5V$
Q, $\overline{Q}$	0.8	–	–	mA	
Power Supply Current					
I_{SS1}	–	200	250	μA	$V_{SS1} = -4.0V$
I_{SS2}	–	–	50	μA	$V_{SS2} = -4.0V$
	–	200	250	μA	$V_{SS2} = -15V$
I_{SS3}	–	–	15	μA	$V_{SS3} = -4.0V$
	–	50	60	μA	$V_{SS3} = -15V$

** Typical values are at +25°C and nominal voltages.

NOTES: 1. In practice, it is recommended that the capacitor at pin 3, or the resistor at pin 4, be adjusted to set the frequency to 18 kHz with a nominal supply voltage at an ambient temperature of +25°C.

TIMING DIAGRAM



TELECOM

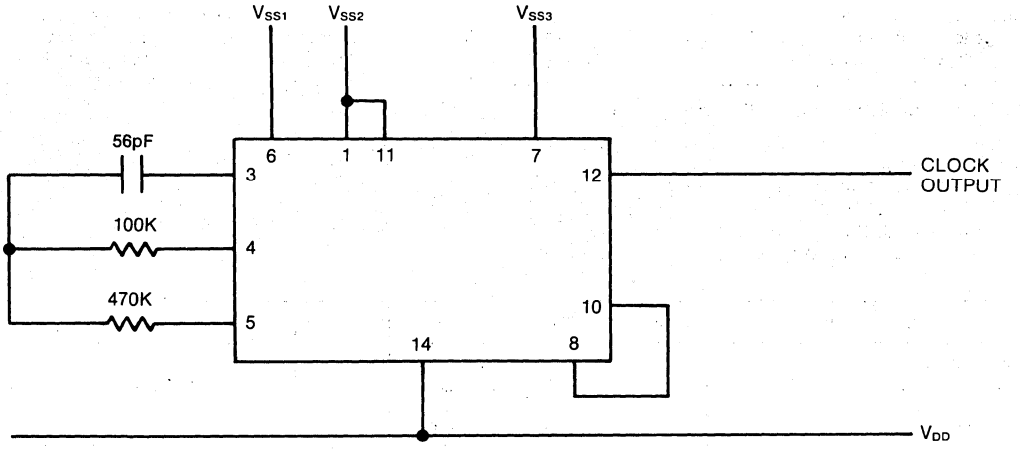


Fig. 1

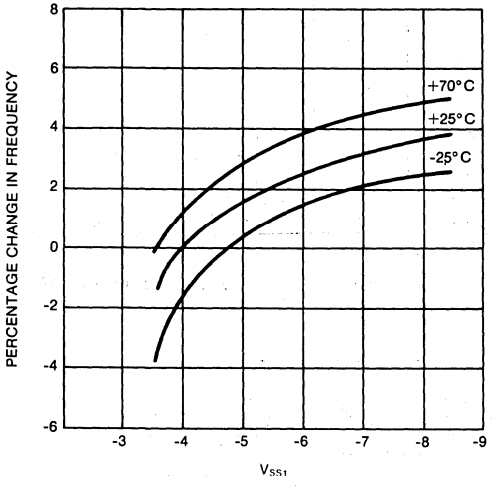


Fig. 2 TYPICAL FREQUENCY STABILITY

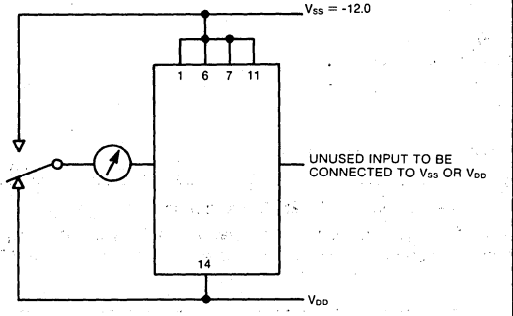


Fig.3 INPUT LEAKAGE CURRENT TEST

TELECOM

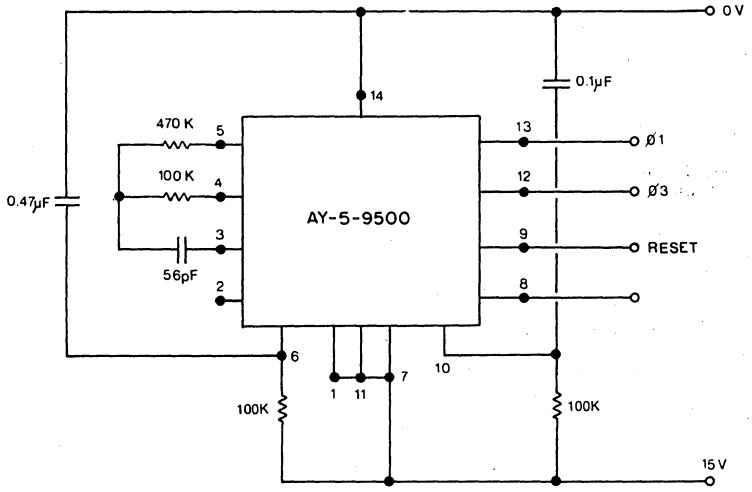


Fig.4 SINGLE SUPPLY OPERATION

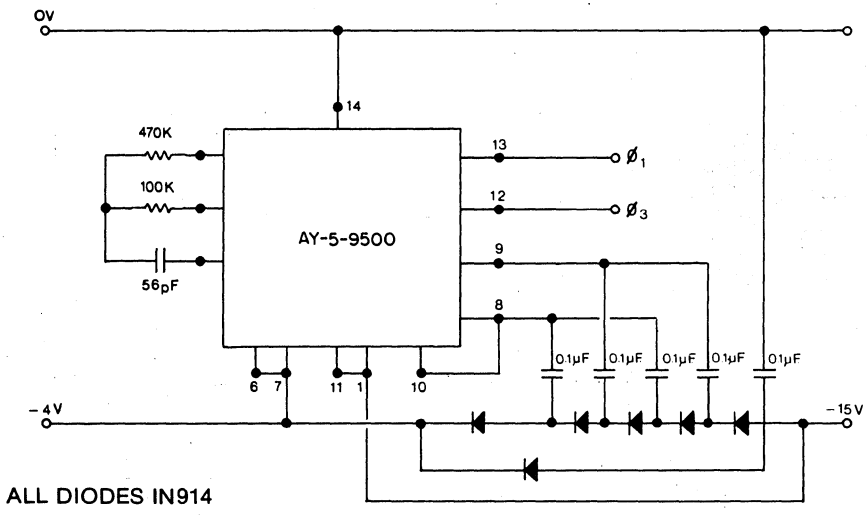


Fig. 5 DC-DC CONVERTER CONNECTION

Dual Tone Multi-Frequency Receivers

FEATURES

- No tuning required; inherent discrimination better than ±0.1%
- Digitally defined bandwidths with no inherent voltage or temperature drift
- Fast acquisition of tones
- Frequency correlation provides good S/N performance
- Inter-tone separation checked for correct IDP period
- Many programmable features provide wide applications
- High reliability and low cost using P-channel process
- On-chip analog amplifiers for analog preprocessing
- Interfaces directly with the AY-5-9100 for M.F.—Strowger converters (AY-5-9801/9805)
- Handshaking facility to interface directly with CP1600 microprocessor
- Three-State code outputs

AY-5-9800 SERIES

Part Number*	Output Code	On-Chip OP Amps	Pins
AY-5-9801	4-Bit	Yes	28
AY-5-9802	1 of 16	Yes	40
AY-5-9803	2 of 8	Yes	40
AY-5-9804	Binary	Yes	28
AY-5-9805	4-Bit	No	24
AY-5-9807	2 of 8	No	24
AY-5-9808	Binary	No	24

*Part numbers AY-5-9801 through 9808 are supplied in ceramic packages.

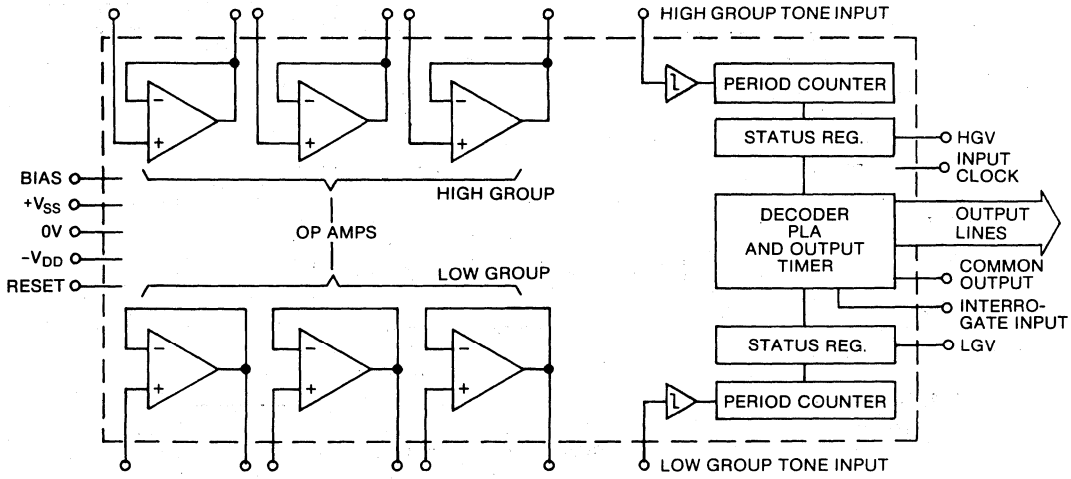
PROGRAMMABLE OPTIONS

These options can all be provided by a single layer mask change.

- Programmable center frequencies
- Programmable accuracies
- Variable "Acquire" criteria (1 out of 5 to 5 out of 5)
  Variable "Release" criteria (1 out of 5 to 5 out of 5)
- Normally arranged for 2 of 8 detection, but can be reprogrammed for single tone (1 of 8) detection
- Common output can be delayed by 1-32 ms after tones are detected valid
  Note: IDP period = common delay + common width
- Common output pulse can be programmed from 1-31 ms.
- Output code can be any 4 bit code in 24/28 lead DIP or any 16-bit code in 40 lead DIP (e.g. 2 of 7, 1 of 12 etc.)

TELECOM

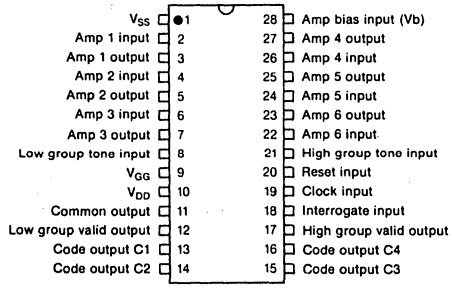
BLOCK DIAGRAM



PIN CONFIGURATIONS

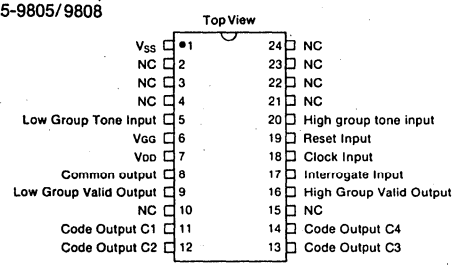
28 LEAD DUAL IN LINE
AY-5-9801/9804

Top View



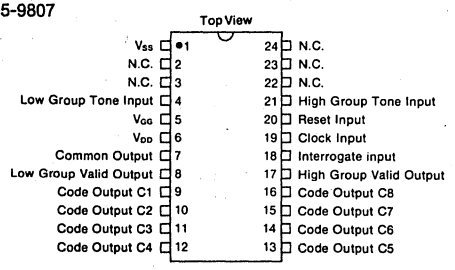
24 LEAD DUAL IN LINE
AY-5-9805/9808

Top View



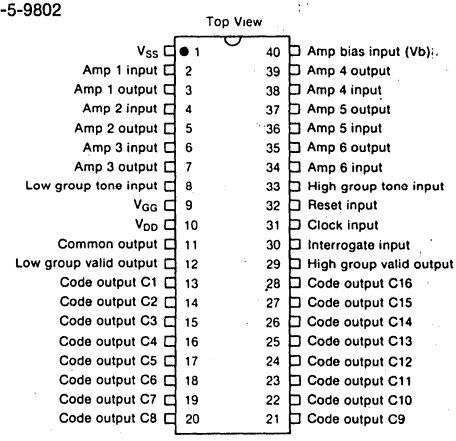
24 LEAD IN DUAL LINE
AY-5-9807

Top View



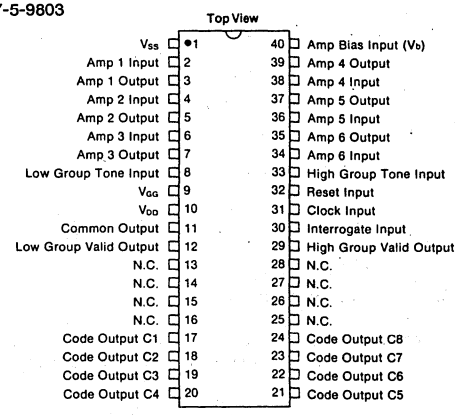
40 LEAD DUAL IN LINE
AY-5-9802

Top View

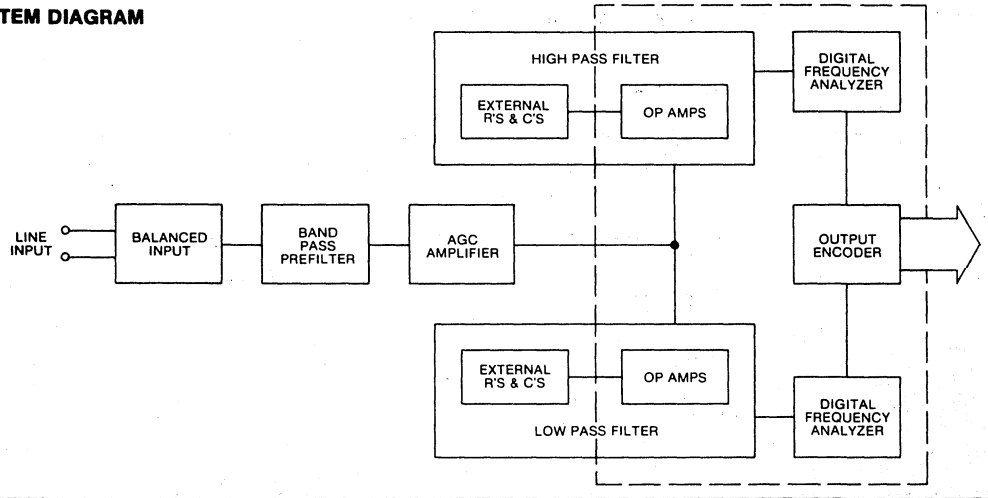


40 LEAD DUAL IN LINE
AY-5-9803

Top View



SYSTEM DIAGRAM



TELECOM

DESCRIPTION

The AY-5-9800 series circuits are fabricated in P channel MTNS process thus minimizing cost and providing high reliability. The basic chip block diagram is shown on the previous page. For analog preprocessing six amplifiers are included on-chip, external components being used to determine the filter characteristics. The major functions are mask programmable thus giving a flexible system at a low cost.

The tone pair is separated into two individual tones using the analog circuitry, the separated tones being applied to the Schmidt triggers to square incoming signals which are then processed by the digital circuitry. The high and low group logic is similar; only the decode values for frequency recognition are different. The incoming signal is divided by two or three to eliminate the effects of changing mark/space ratio and its period counted by a timer which is clocked by the accurate 1MHz clock. If the period value is within encoded limits, the result is stored. Five cycles of incoming signal are stored and a decision is made with this information as to whether the tone is valid. A programmable logic array scans the five cycle store for both an "Acquire" criteria and "Release" criteria. If the "Acquire" criteria is exceeded (e.g. 4 out of 5), and the "Release" criteria is not reached (e.g. less than 2 out of 5), the frequency is deemed to be valid. If both high and low frequencies are detected, a time-out timer is started. This timer is mask programmable and will normally require 25ms of valid tone pair signal. Once this period has elapsed the Common Output pulses high, again for a preprogrammed period. After this pulse, the system will not respond again until an IDP of a preprogrammed duration occurs, after which a new input tone pair can be applied.

The Code Outputs and Common Output can be configured for a wide variety of systems. A typical device, AY-5-9801/9821, provides four Three-State Code outputs suitable for microprocessor controlled systems and direct interfacing to the AY-5-9100 for DTMF-Strowger converters. A handshaking interface is provided using the Interrogate input thus allowing very simple microprocessor interfacing.The outputs will directly drive low power TTL, CMOS or MOS and, being Three-State, can be bussed in large systems.

Input Clock — The recommended clock frequency is 1MHz which will then give a frequency detect range of 620—3400Hz with a discrimination of ± 1μs. The discrimination of 1633Hz using a 1MHz clock will be better than ± 0.1%. Any deviation of the 1MHz clock will result in a proportional deviation of the tone recognition bands.

Power-On-Reset—An external power-on reset is required which is used to reset all counters, etc. An on-chip resistor pulls this input to V_{DD}; a 0.1μF capacitor connected from the P.O.R. input to V_{SS} will provide automatic power-on-reset. This input can be used as a chip select putting all Three-State outputs into their high impedance state when held high.

Input Amplifiers—Input amplifiers are suitable for use in band-pass and general buffer amplifiers. They have an open loop gain of approximately 250 and are trimmed by a single 'Bias Input'.

Period Counters—The input frequency, which must be A.C. coupled, is interrogated by the period counter. Each counter has eight values decoded, these representing F1 low limit, F1 high limit etc. Once a positive going edge is detected, the period counter is started and if the next positive going edge occurs during a time slot decode, the circuit deems the tone to be valid and a bistable indicating the tone decoded is set. Special logic is incorporated to prevent the counter from being continuously triggered in the presence of noise.

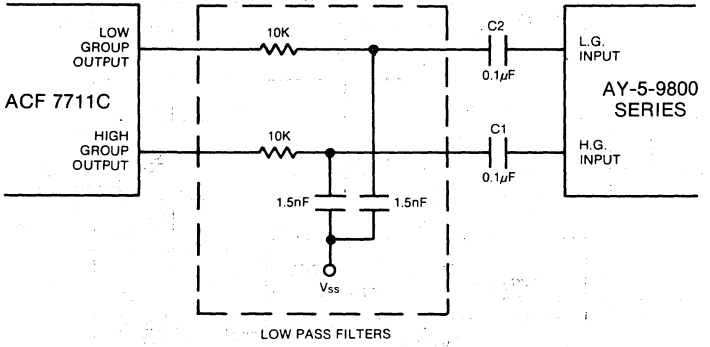
Status Word Register—The Status Word Register is a five bit register which is filled with 1's for an in-band signal but filled with 0's for out-of-band signals. With the data in this register a decision is performed which sets a bistable (Acquires the signal) or resets a bistable (Releases the signal). Thus by changing the preprogrammed acceptance standard, a direct trade-off between S/N ratio and stimulation rate can be obtained for different systems.

Output Logic—Two outputs, HGV and LGV, indicate the current state of the correlator for each group. A valid high group frequency, if present for longer than the correlation time, will cause the HGV (high group valid) output to go high. Similarly with the LGV (low group valid) output. Once both high and low group tones have been detected valid, a preprogrammed timer is started. If the tone pair is still valid after the timer has counted out, the Common Output goes high for a preprogrammed period and the Code Outputs present the programmed outputs corresponding to the tone pair input.

If the interrogate input is used for handshaking, the Code Outputs are only presented after the interrogate input goes low, the interrogate input going high removes both the Codes and the Common Output.

TELECOM

AY-5-9800 SERIES SYSTEM IMPROVEMENT NOTE



Leakage of the 1MHz Clock signal onto the High or Low Group inputs can cause intermittent High or Low Group Valid outputs, and reduction of the system sensitivity.

To remedy this, the low pass filters shown below are inserted between the ACF 7711 Band Separation Filter and the input decoupling capacitors (C1 and C2) of the AY-5-9800 series Multi-Frequency Receivers. This restores proper operation of the MFR while attenuating stray clock signals more than 39 db.

OUTPUT CODE CHART

Input Tone Pair		Normal Digit Representation	AY-5-9801 AY-5-9805 Output Code*				AY-5-9802 AY-5-9806 Output Code	AY-5-9803 AY-5-9807 Output Code	AY-5-9804 AY-5-9808 Output Code**			
Low Group (Hz)	High Group (Hz)	C1	C1	C2	C3	C4	1 of 16	2 of 8	C1	C2	C3	C4
697	1209	1	1	1	1	1	C1	C1,C5	1	1	1	0
697	1336	2	1	1	1	0	C2	C1,C6	1	1	0	1
697	1477	3	1	1	0	1	C3	C1,C7	1	1	0	0
697	1633	(A)	0	0	0	1	C4	C1,C8	0	0	0	1
770	1209	4	1	0	1	1	C5	C2,C5	1	0	1	1
770	1336	5	1	0	1	0	C6	C2,C6	1	0	1	0
770	1477	6	1	0	0	1	C7	C2,C7	1	0	0	1
770	1633	(B)	0	0	1	0	C8	C2,C8	0	0	1	0
852	1209	7	0	1	1	1	C9	C3,C5	1	0	0	0
852	1336	8	0	1	1	0	C10	C3,C6	0	1	1	1
852	1477	9	0	1	0	1	C11	C3,C7	0	1	1	0
852	1633	(C)	0	1	0	0	C12	C3,C8	0	0	1	1
941	1209	*	0	0	1	1	C13	C4,C5	0	1	0	0
941	1336	0	1	1	0	0	C14	C4,C6	0	1	0	1
941	1477	#	0	0	0	0	C15	C4,C7	0	0	0	0
941	1633	(D)	1	0	0	0	C16	C4,C8	1	1	1	1

*Compatible with AY-5-9100 **Compatible with AY-5-9120.

FREQUENCY MEASUREMENT TOLERANCES

NOMINAL CENTER FREQUENCY (Hz)		BANDWIDTH (Hz)	% TOLERANCE
Low Group	697	683.3- 711.2	−1.97 to +2.04
	770	755.0- 785.9	−1.95 to +2.06
	852	835.4- 869.6	−1.97 to +2.07
	941	922.5- 960.2	−1.97 to +2.04
High Group	1209	1185.5-1233.8	−1.94 to +2.05
	1336	1309.8-1363.3	−1.96 to +2.04
	1477	1448.2-1507.2	−1.95 to +2.04
	1633	1601.3-1666.7	−1.94 to +2.06

NOTE:
The figures quoted are as programmed. Any variation in master clock frequency will cause additional errors.

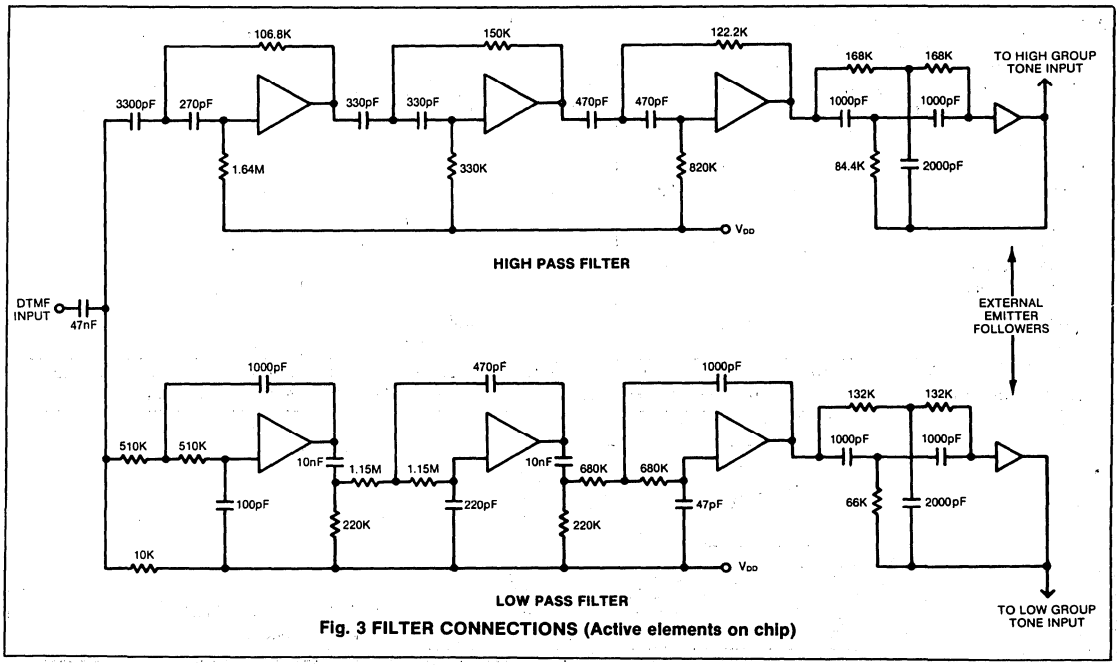


Fig. 3 FILTER CONNECTIONS (Active elements on chip)

TELECOM

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... -20V to +0.3V
Storage Temperature Range ..... -65°C to +150°C
Ambient operating temperature ..... -25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = -8.5 ±0.5V
V_{GG} = -17V ±1V
Clock frequency = 1MHz
Operating Temperature (T_A) = +25°C

Characteristics	Min	Typ	Max	Units	Conditions
Clock					
Logic '0' level	+0.3	—	-1.0	V	
Logic '1' level	-6.5	-8.5	-18	V	
Frequency (see NOTE below)	0.01	1.0	1.1	MHz	
Rise Time	10	—	50	ns	
Fall Time	10	—	50	ns	
Width	450	500	550	ns	
Capacitance	—	—	20	pF	
Leakage	—	—	10	μA	
Logic Inputs					
Logic '0' level	+0.3	—	-1.0	V	
Logic '1' level	-3.7	-5	-18	V	
Capacitance	—	—	10	pF	
Leakage	—	—	10	μA	
Logic Outputs					
(i) Code outputs					
Logic '0' output current	1	—	—	mA	V_O = -1V
Logic '1' output current	460	—	—	μA	V_O = -5V
(ii) Common output					
Logic '0' output current	1	—	—	mA	V_O = -1V
Logic '1' output current	620	—	—	μA	V_O = -5V
Pulse delay	1	—	31	ms	
Pulse width	1	32	32	ms	
(iii) Group valid outputs (HGV & LGV)					
Logic '0' output current	500	—	—	μA	V_O = -1V (External pull-down resistors to V_{DD} required).
Signal Input	.5	—	2	V	Peak to peak sine wave
"Handshake" Routine					
(See Fig. 1 for timing diagram). T1, T2	—	—	2.5	μs	
Pull-down resistor (to V_{DD})	50	150	500	kΩ	
Power-on Reset					
Pull-down resistor (to V_{DD})	50	150	500	kΩ	
Pulse Width	10	—	—	μs	
Amplifiers					
Open loop gain	—	500	—	—	Fin = 1kHz
Open loop bandwidth	—	1	—	MHz	
Output Impedance	—	—	6	kΩ	Fin = 1kHz
Power Dissipation	—	—	350	mW	V_{DD} = -9V V_{GG} = -18V

NOTE: Any deviation from the nominal 1MHz clock frequency will result in a corresponding deviation of the frequency detection bands. Other frequencies than 1MHz clock can be preprogrammed in, but circuit characteristics will be modified.

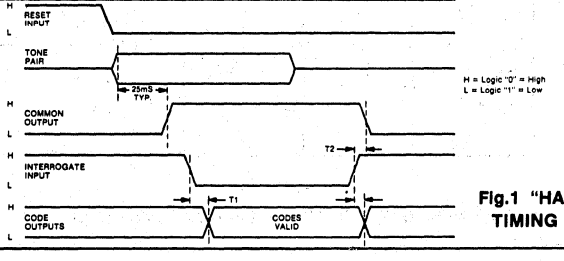


Fig.1 "HANDSHAKING" TIMING DIAGRAM

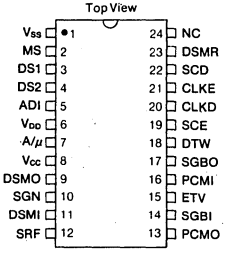
PCM Code Converter (CODEC)

FEATURES

- Converts a delta-sigma modulated pulse stream at 2048 kbit/sec into 8 ksample/sec companded PCM
- Converts 8 ksample/sec companded PCM into a delta-sigma modulated pulse stream at 2048 kbit/sec
- Enables the realization of a single channel PCM Codec using a minimum of external components
- Serial PCM input/output interface can operate in a single channel mode at 64 kbit/sec, or at up to 2048 kbit/sec for a multi-channel burst format
- All digital technique uses no on-chip precision components
- Pin-selectable A-law/μ-law companding characteristic
- Optional alternate digit inversion provided
- Direct interface with standard TTL or CMOS
- Encoder and Decoder can be clocked asynchronously (useful for PCM multiplex applications)

PIN CONFIGURATION

24 LEAD DUAL IN LINE



DESCRIPTION

The AY-3-9900 is a PCM Code Converter containing all the logic necessary to realize a high performance low cost single channel PCM Codec according to the system block schematic, Fig. 1. It contains no analog components and is fabricated with General Instruments' N-Channel Ion-Implant GIANT II process, ensuring high performance with proven reliability and production history.

Together with the chip, an external delta-sigma modulator and demodulator using a small number of easily obtainable components, is required to construct the Codec, which uses delta-sigma modulation as an intermediate stage in the conversion of an analog signal into PCM and vice-versa. A pin-selectable companding characteristic which meets the CCITT recommendations G711/G712 for both. A law and μ law with good safety margins is included, together with a very flexible serial PCM input/output interface to allow the Codec to be readily used in a wide number of applications.

TELECOM

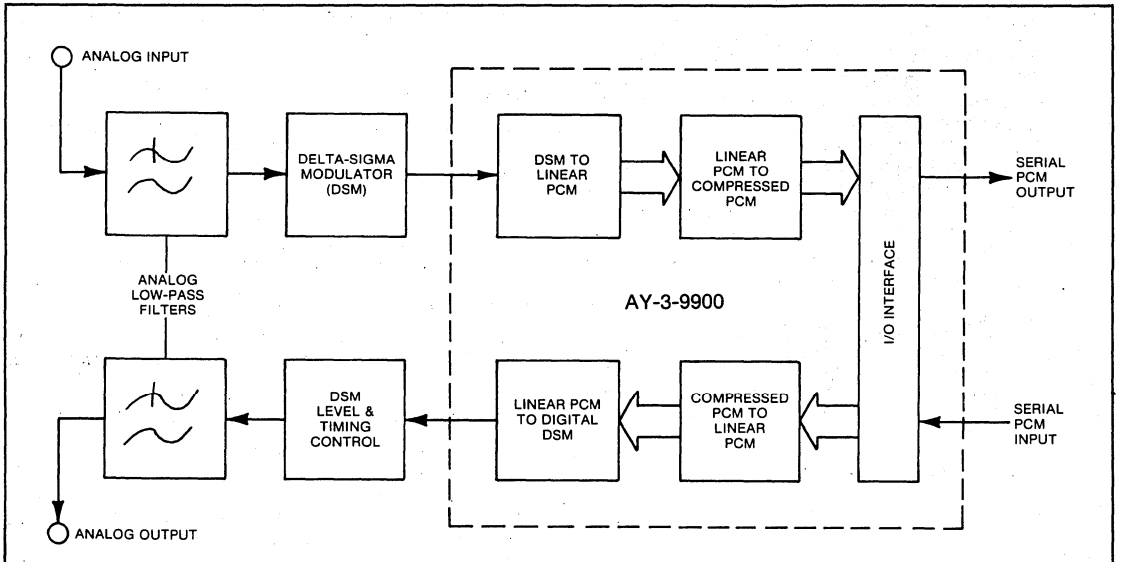


Fig.1 BLOCK DIAGRAM OF A COMPLETE CODEC

CIRCUIT DESCRIPTION

The AY-3-9900 consists of two autonomous logic systems, designated in this specification as encoder and decoder. The encoder provides the necessary logic for the digital conversion of a delta-sigma encoded pulse density signal at 2048 kbit/sec into standard 8 ksample/sec 8 bit compressed PCM codewords. The decoder provides the necessary logic for the digital conversion of standard 8 bit compressed PCM characters at 8ksample/sec into a delta-sigma encoded pulse density signal at 2048 kbit/sec. Serial PCM input/output interfaces are also provided with facilities for a data rate of 64 to 2048 kbit/sec to enable its use in either a single channel system or a standard 30 channel TDM environment. For the necessary timing information to clarify this section reference should be made to the waveform diagrams, Figs. 5a, 5b, and 5e.

The encoder logic, operating continuously on the delta-sigma input pulse train, will generate a corresponding compressed PCM codeword every 125μs; with alternate digit inversion being provided if required by appropriate use of the ADI control input. A timing vector pulse (ETV) of nominal width equal to one encoder clock period, will define the required frame start time and should be repeated every 125μs to ensure correct synchronization.

If the mode select (MS) input is connected high then the 8 bit PCM codeword will be transmitted serially at a rate of 64 kbit/sec at which speed each codeword will occupy the full 125μs frame period for transmission, with the leading edge of the first bit occurring at a time defined by the ETV pulse.

Alternatively, if the MS input is left open circuit or connected low, the serial PCM transmission will be under the control of an externally generated shift clock (SCE) which can vary in frequency from 64kHz to 2048kHz. The timing of this input function allows the insertion of a number of signalling bits into the PCM stream via the SGBI input.

With the MS input connected high, an input PCM bit stream at 64 kbit/sec will be accepted by the decoder logic under the control of internal clocks generated from the CLKD signal. Because of delays through the transmission network, normally under the control of transmission switches, the input pulse stream may be delayed in time by number of digit periods from the original pulse stream as transmitted. To allow for this, a discrete delay of 0 to 3 digit periods can be selected by the control inputs DS1 and DS2 which results in a controlled shift of decoder timing in order to re-align bit 1 in its correct position in the input register. Alternatively, if the MS input is left open circuit or connected low, the decoder input interface will be under the control of externally generated waveforms in which case it requires an input shift clock (SCD) and timing waveform (DTW) to define the time when bit 1 of the input codeword occupies its correct position in the input register. In this mode, the device will accept an input PCM stream at up to 2048 kbit/sec, with any signalling bits present in this signal being extracted via the SGBO output.

Upon receipt of a compressed PCM codeword, the decoder logic will first remove alternate digit inversions if necessary (under the control of the ADI input) after which the codeword will be linearized. A digital delta-sigma modulator will then generate a delta-sigma bit stream at 2048 kbit/sec for external decoding to produce the required analog signal.

All inputs and outputs of the AY-3-9900 are directly compatible with standard TTL (driving capacitive loads) or CMOS.

INPUT/OUTPUT FUNCTIONS

Supplies:

V_{SS}	GND
V_{CC}	+5V
V_{DD}	+9V

DC Control Signals:

MS — Mode Select — Selects between internal and external PCM I/O interface timing
Logic 0 = external
Logic 1 = internal
A resistor is connected internally between this input and V_{SS}.

ADI — Alternate-digit-inversion control – Selects ADI or no ADI
Logic 0 = no ADI
Logic 1 = ADI
A resistor is connected internally between this input and V_{SS}.

DS1, DS2 — Decoder delay select — A two bit binary word to select the required digit delay between encoder and decoder.

DS1	DS2	Digit Delay
0	0	0
0	1	1
1	0	2
1	1	3

A resistor is connected internally between each input and V_{SS}.

A/μ — Companding characteristic select-selects either A law or μ law
Logic 0 = A law
Logic 1 = μ law
A resistor is connected internally between this unput and V_{SS}.

CLOCKS & AC CONTROL SIGNALS

CLKE — Encoder main clock — 2.048MHz clock signal

CLKD — Decoder main clock — 2.048MHz clock signal

SCE — Encoder shift clock — Used to control the output of serial PCM data from the encoder (when MS=0)

SCD — Decoder shift clock — Used to control the input of serial PCM data to the decoder (when MS=0)

ETV — Encoder timing vector — A pulse defining the beginning of each frame, used to maintain encoder timing.

DTW — Decoder timing waveform — A pulse used to indicate to the decoder when the input PCM stream is in the input register (only required when external shift clocks are used).

DSMR — Delta-sigma reset — a pulse used to reset the digital delta-sigma modulator during testing only. Should be tied to ground during normal operation.

ENCODER OPERATIONAL INPUTS & OUTPUTS

DSMI — Delta-Sigma modulated input signal — Input to the encoder from the delta-sigma modulator.

SRF — Spectral redistribution function — 8kHz Output signal used to operate on the delta-sigma modulator to reduce low frequency quantization noise.

SGN — Sign bit output — Sign bit from the encoder, used to operate on the delta-sigma modulator for DC alignment.

SGBI — Signalling bit input — facility for adding signalling bit(s) to the output PCM stream. (MS = 0).

PCMO — PCM output — Serial PCM output under the control of the encoder shift clock (MS = 0) or the encoder main clock (MS=1).

DECODER OPERATIONAL INPUTS AND OUTPUTS

PCMI — PCM input — Serial PCM input under the control of the decoder shift clock (MS = 0) or the decoder main clock (MS=1).

SGBO — Signalling bit output — Serial output for extracting signalling bit(s) from the incoming PCM stream.

DSMO — Delta-sigma modulated output signal — Output pulse stream from the decoder.

A SINGLE CHANNEL PCM CODEC

The block schematic of a single channel Codec using the AY-3-9900 is shown in Fig. 1. It consists of a band limiting low pass filter followed by a delta-sigma modulator which, by sampling at a rate of 2048kHz provides a highly over-sampled, waveform-tracking A/D conversion. The bit stream produced by this modulator at 2048 kbits, is then converted into 8 bit compressed PCM code words at the standard rate of 8 ksample/sec; which, after conversion into serial format is transmitted serially at a bit rate of 64 kbit/sec. By the application of external timing signals, the PCM output transmission rate can be increased to allow for multiplexing in a burst format, with a maximum bit rate of 2048 kbit/sec.

The PCM input interface will accept either a 64 kbit/sec bit stream or, by the application of external timing signals, a bit rate of up to 2048 kbit/sec in a burst format. This input PCM stream will be converted into a delta-sigma modulated pulse stream at 2048 kbit/sec, from which the original analog signal can be recovered by the use of a low pass filter,cutting off just above the highest signal frequency to be recovered (3.4kHz).

The transition times and voltage levels of the delta-sigma modulated pulse streams are critical to the performance of the system. The delta-sigma modulator should therefore be constructed using TTL D-Types; with the delta-sigma modulated output pulse stream from the AY-3-9900 being clocked through a similar D-type before the analog signal is recovered.

Fig. 2 shows a more detailed diagram of the necessary external components (including component tolerances) required to realize a complete PCM Codec using the AY-3-9900. The response of such a Codec is shown graphically in Figs. 3 and 4.

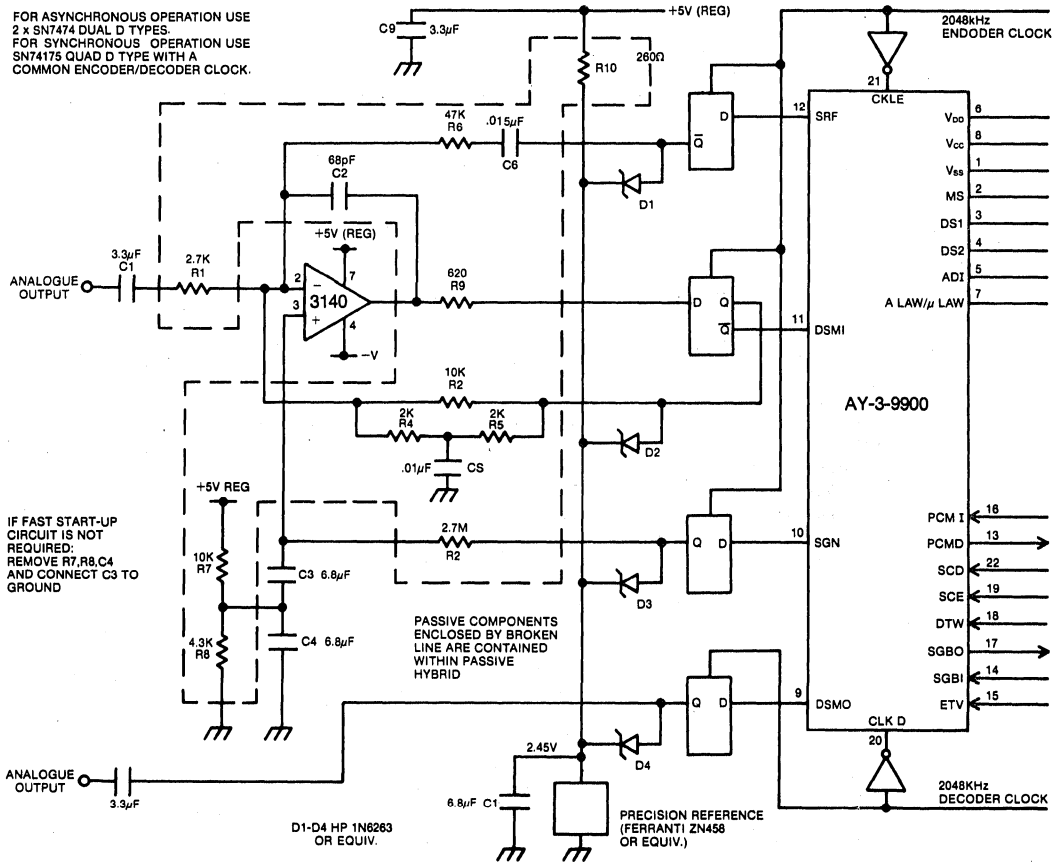
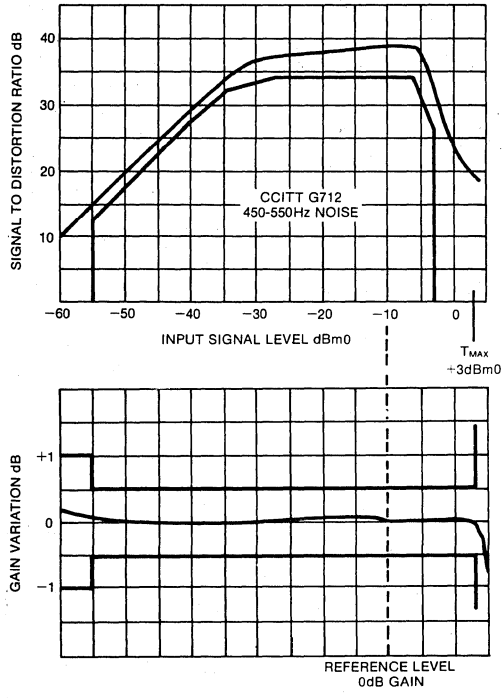


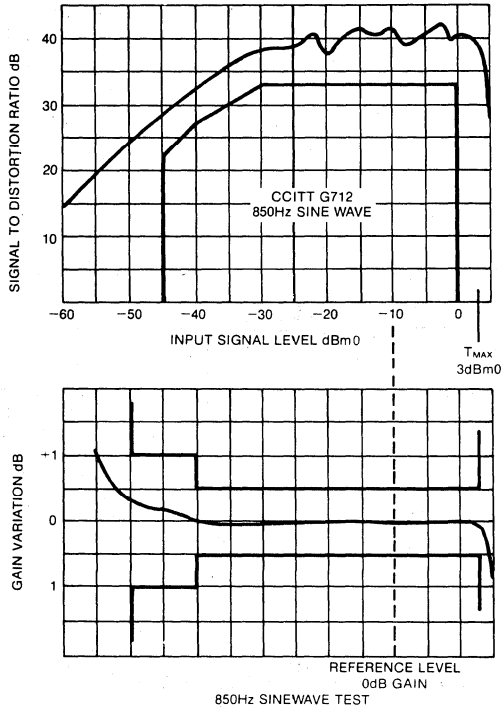
Fig.2 DETAILS OF DELTA-SIGMA MODULATOR, WITH DEMODULATOR LEVEL GENERATOR

TYPICAL PERFORMANCE MEASUREMENTS: A-LAW



450-550Hz NOISE TEST FOR LEVEL < −10dBm0
850Hz SINEWAVE TEST FOR LEVEL > −10dbm0

TYPICAL PERFORMANCE MEASUREMENTS: μ-LAW



850Hz SINEWAVE TEST

TELECOM

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... −0.3V to +15V
Storage temperature range ..... −55°C to +150°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V (substrate voltage)
V_{CC} = +5V ± 5%
V_{DD} = +8.5V to +12.5V
Operating temperature (T_A) = −25°C to +75°C

Characteristic	Min.	Typ.**	Max.	Units	Conditions
DC Control Inputs					
Logic 1	4.75	5	10	V	Connect to V_{CC} or V_{DD}
Logic 0	0	–	0.4	V	Connect to V_{SS}
Pull down resistor	200	–	1000	kΩ	Resistor to V_{SS}
CLOCKS (CLKD & CLKE)					
Logic 1	3	–	10	V	
Logic 0	−0.2	0	0.4	V	
Rise & Fall Times	5	–	40	ns	0.4V-3V transition
Frequency	–	2.048	–	MHz	
Pulse Width	200	–	–	ns	Between 1.5V levels (Fig. 4c)
Input Capacitance	–	–	10	pF	
Other A.C. Control Signals					
Logic 1	3	–	10	V	
Logic 0	−0.2	0	0.4	V	
Rise & Fall times	5	–	40	ns	0.4-3V transition
SCE/SCD pulse width	200	–	–	ns	between 1.5V levels
ETV width (tvw)	–	488	–	ns	See Fig. 4c.
edge variation (tvv)	–	–	100	ns	
DTW width	10	–	–	μs	One digit period (see Fig. 4c)
Input Capacitance	–	–	10	pF	
Operational Inputs					
Logic 1	3	–	10	V	
Logic 0	−0.2	0	0.4	V	
Rise & Fall Times	5	–	40	ns	0.4-3V transition
Pulse Width	200	–	–	ns	between 1.5V levels
Input capacitance	–	–	10	pF	
Operational Outputs					
Logic 1	4	5	5.25	V	
Logic 0	0	–	0.4		
Logic 1 source current	100	–	–	μA	at V_O = 3V
Logic 0 sink current	1.6	–	–	mA	at V_O = 0.4V
Rise & Fall times	–	–	40	ns	0.4-3V transition (driving 15pF)
PCMO delay (from SCE edge)	40	100	140	ns	between 1.5V levels
Power Consumption	–	–	450	mW	at V_{CC}=5V, V_{DD}=9V

**Typical values are at +25°C and nominal voltages.

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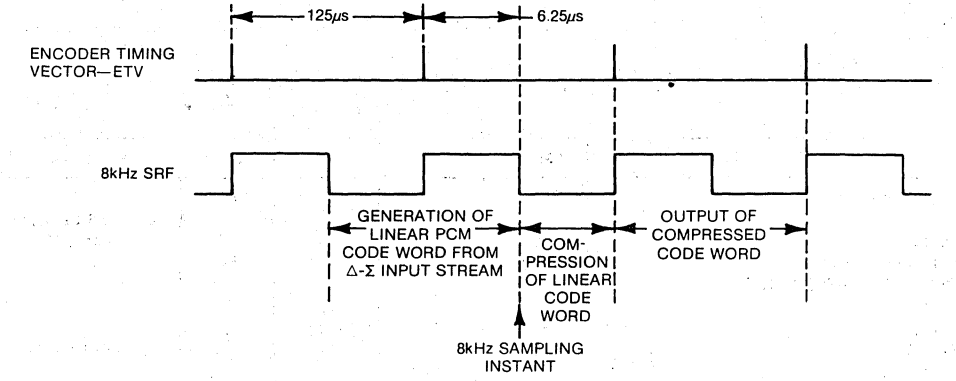
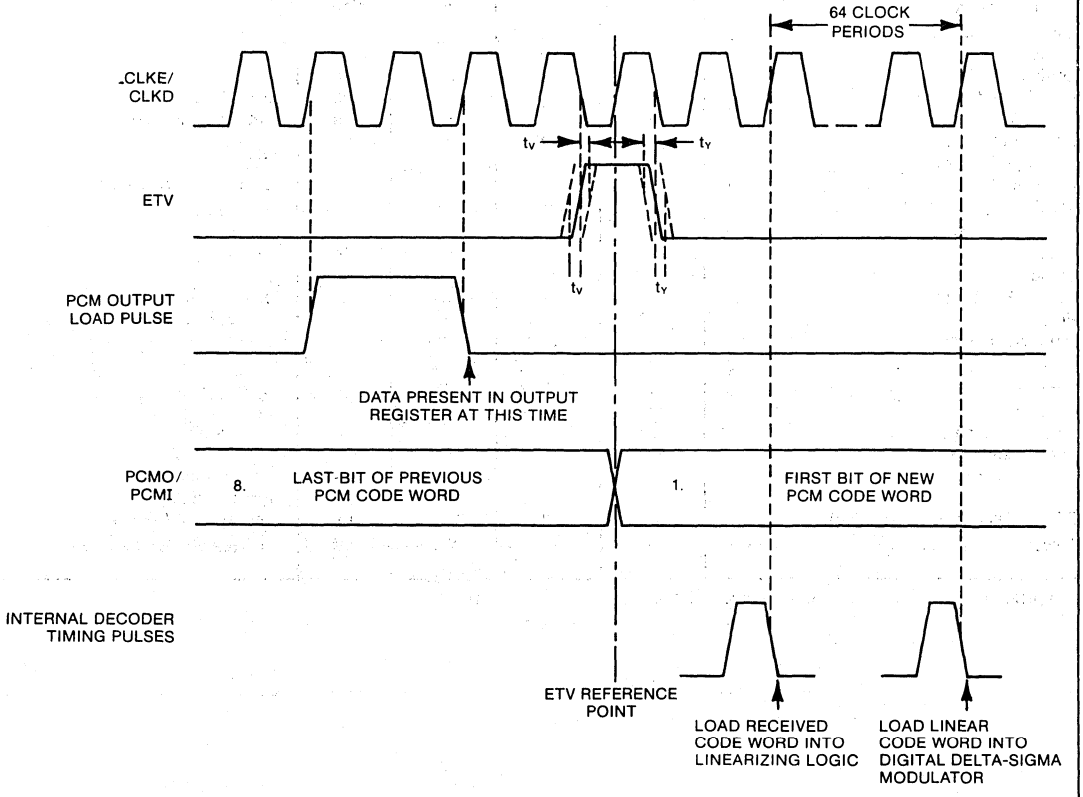
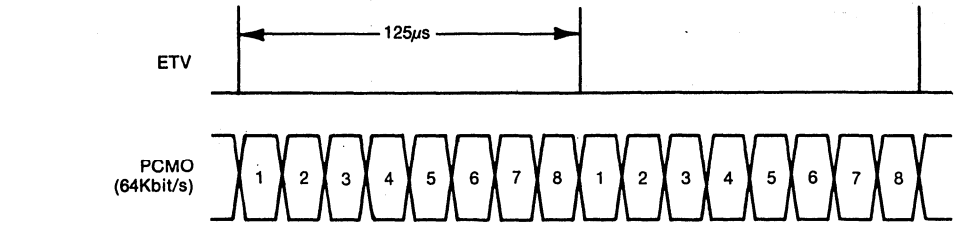


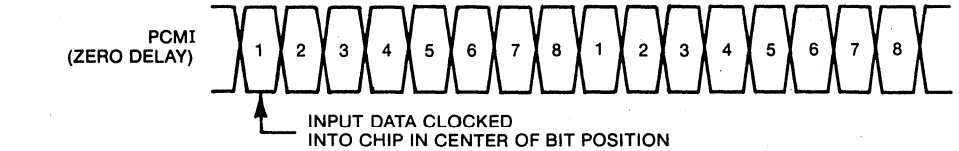
(a) TIMING OF ENCODER OPERATION

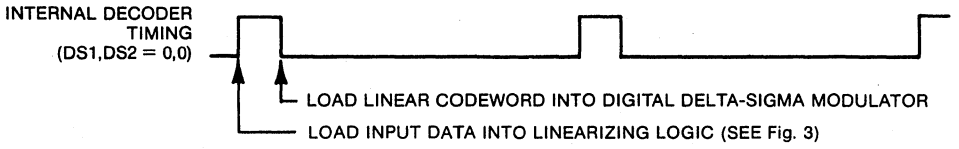


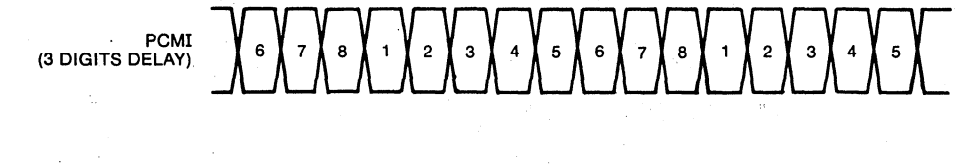
(b) DETAIL OF ETV TIMING AND INTERNAL CLOCK MODE INPUT/OUTPUT TIMING



(a) PCM OUTPUT DATA STREAM (INTERNAL CLOCKS)







(b) PCM INPUT DATA STREAM (INTERNAL CLOCKS)

Programmable Microcomputer Telephone Diallers

FEATURES

- Microcomputer based dialler
- On board keyboard debounce circuitry
- Single button redial of last number dialled
- Program can be customized by single mask change

STANDARD PROGRAMMED DEVICE FEATURES

TZ-2001 — Pulse Dialler

- Outputs for 12 digit time multiplexed display
- 16 numbers by 12 digit repertory storage via 1 button recall
- Real time clock (hrs., min., sec.)
- Elapsed time timer/stopwatch
- Optional calculator interface with C-59X series

TZ-2002 — Dual Tone Dialler

- Outputs for 12 digit time MUX display
- 16 numbers by 12 digit repertory storage via 1 button recall
- Real time clock (hrs., min., sec.)
- Prompting display for simple operation

TZ-2003 — Pulse or Dual Tone Dialler

- 32 numbers by 16 digit repertory storage
- Selectable pulse dialling rates
- Selectable tone duration lengths
- Indicators for auto redial, hold and store modes

DESCRIPTION

The TZ-2000 series telephone diallers are from the General Instrument PIC series microcomputers. They are programmed to function as dialler circuits to produce either dual tone or pulse dialling functions. As with the PIC microcomputers, the TZ-2000 series are fabricated in N-channel Ion Implant technology and contain RAM, I/O parts, C.P.U. and pre-programmed ROM.

The TZ-2001 is a pulse dialler that simulates the outputs of a rotary telephone dial. It also displays and stores up to 16 12-digit telephone numbers, keeps real time displaying hours, minutes, and seconds, and can act as a stopwatch to enable the telephone user to time a call.

The TZ-2002 is a dual-tone dialler that produces the tone codes for the General Instrument AY-3-9400 Dual Tone Multifrequency Generator to generate the tonal outputs in a telephone set. It also displays and stores up to 16 12-digit telephone numbers and keeps real time displaying hours, minutes, and seconds.

The TZ-2003 is a pulse or dual tone dialler with the ability to store 32 16-digit telephone numbers. It also has selectable pulse duration rates and selectable tone duration rates plus LED function indicator drivers.

The logic timing is provided by an on-chip oscillator using an external R-C network. The use of an external 32.768kHz crystal is implemented for real time events.

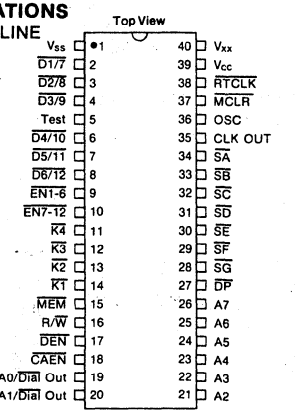
The repertory storage is achieved through the use of external RAM devices. The TZ-2001 and TZ-2002 use a 256 x 4 bit RAM device.

The Keyboards required for these devices consist of single key depression switches arranged in matrixes. The TZ-2001 and TZ-2002 devices require an 8 x 4 matrix and the TZ-2003 requires a 4 x 4 matrix.

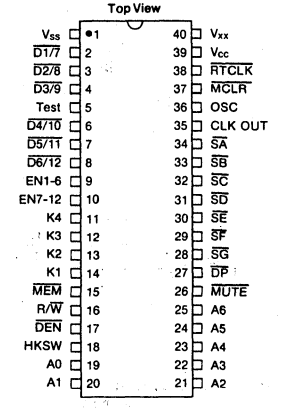
PIN CONFIGURATIONS

40 LEAD DUAL IN LINE

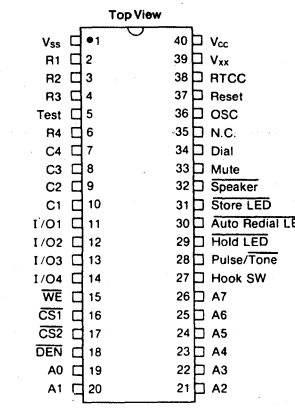
TZ-2001



TZ-2002



TZ-2003



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TZ-2000 SERIES OPERATION

Dial Mode

The TZ-2001 simulates a rotary dial telephone in that the output produces a series of pulses. The TZ-2001 may be dialled by consecutive numerical entries from the keyboard after depressing the Dial Key.

The number depressed will appear in the right hand side of the display. As consecutive numbers are entered the numbers will shift left on the display. The minimum time interval between number entries is 80 msec.

The "PA" key allows a pause in access or break within the dialled sequence. The "RE" key allows a redial of the number entered. A double depression of the "DIAL" key erases the number displayed.

The TZ-2002 drives the AY-3-9400 to generate a dual tone frequency. Depression of the "DIAL" key prompts the user with the words "DIAL PLEASE" on the display.

Consecutive digit entries with a minimum of 80 nsec between entries will be displayed and dialled.

A double depression of the "DIAL" Key enables the complete number to be redialled. A display of "NONE" indicates no number in storage or an erasure of a number. The "P" Key enables the user to pause or break the dial out sequence for 2 seconds. To dial from the repertory storage, depress one of the 16 storage keys L1 to L16 after a "DIAL PLEASE" prompt display.

Store Mode

Depression of the "Store" key enables numbers to be entered into the storage memory. Both the TZ-2001 and TZ-2002 have prompting messages displayed after the store mode is entered.

The TZ-2001 prompts with a "ST" displayed and the TZ-2002 prompts with "STORE INTO" displayed after entering the "STORE" mode with the given prompting, the location must be selected by depressing one of the L1 to L16 keys. After the location is determined the TZ-2001 prompts with "STORE PLEASE" displayed. Then the telephone number can be entered as in the dial mode.

Time Mode

Depression of the "TIME" key puts the TZ-2001 and TZ-2002 circuits into the time display mode. They both indicate real time in a hours, minutes and seconds format. To set the time of day on the TZ-2001 depress the "TIME SET" key on the TZ-2002 depress the "P" key. Then enter the correct time starting with tens of hours, hours, tens of minutes then minutes. The real time starts with the fourth digit entry of the time.

The stop watch on the TZ-2001 starts with a double depression of the "TIME" key and can count up to 12 hours of elapsed time. Another depression of the "TIME" key stops the elapsed time and a final depression of the "TIME" reverts back to real time.

TZ-2003 OPERATION

The TZ-2003 has four modes of operation:

1. Dial
2. Automatic redial
3. Store
4. Hold mode

Dialling

Dialling can be operated in either the pulse or tone functions. Consecutive digit and pause entries cause the dialling to occur. Dialling may be made with either the hardset on hook or off hook. A redial of the same number can be made by depressing the redial key.

Automatic Redial

Automatic redialling of the same number consecutively at 40 sec intervals can be augmented by depressing the redial key twice. This makes the n.

Store

Depression of store key enters circuit into the store mode indicated by LED store indicator. Next two digits enters the storage location number from 01 to 32.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +70°C
V_{CC}, V_{XX}, all other I/O voltages ..... −0.3V to 12.0V (with respect to V_{SS})

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5.0V ±5%
V_{XX} = 4.75V to 10.0V

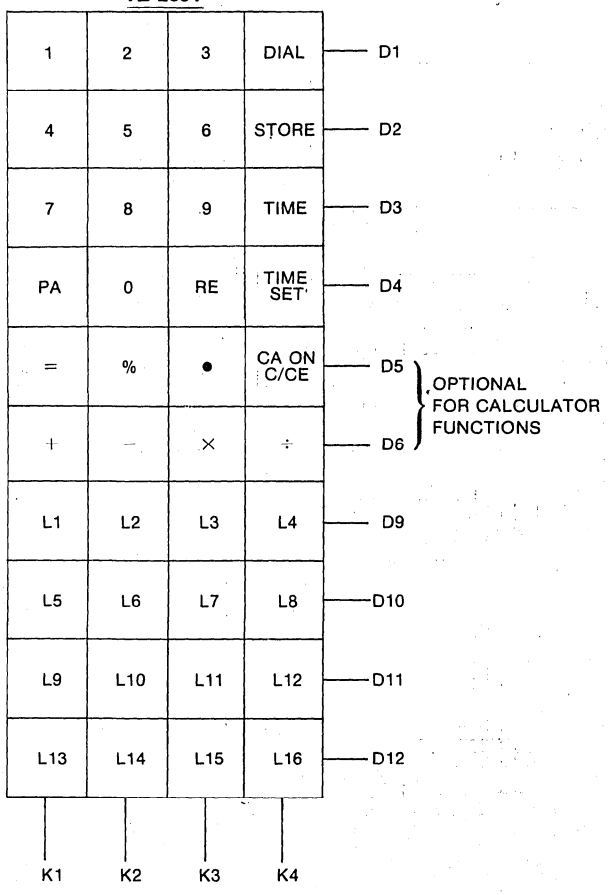
Characteristic	Sym	Min	Typ	Max	Units	Conditions
Power Supply Currents	I_{CC}	—	35	50	mA	
	I_{XX}	—	1	5	mA	
Logic Inputs						
Low	V_{IL}	0	—	0.65	V	
	V_{IH}	2.4	—	V_{CC}	V	
Logic Outputs						
Low	V_{OL}	—	—	0.45	V	V_{XX} = 5V @ I_{OL} = 1.6mA
High	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 100μA
Osc Frequency	f_{in}	0.8	—	1.0	MHz	
Rt Clk Frequency	f_{rt}	—	32.768	—	kHz	Crystal Generated
CLK OUT Frequency	—	0.25 f_{in}	—	—	—	
Key Debounce Time	t_{db}	15.6	—	23.4	ms	
Interdigit Pause	IDP	—	125	—	ms	
Tone Duration	—	—	125	—	ms	

TABLE 3: DUAL TONE FREQUENCY OUTPUTS

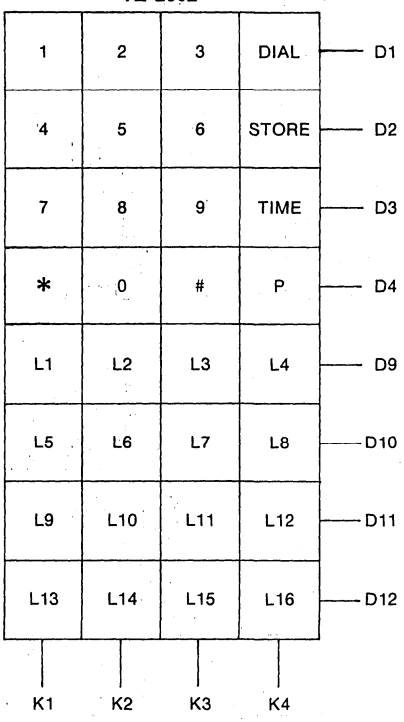
DIGIT	LOW FREQUENCY (Hz)	HIGH FREQUENCY
1	697	1209
2	697	1336
3	697	1477
4	770	1209
5	770	1336
6	770	1477
7	852	1209
8	852	1336
9	852	1477
0	941	1336
A (*)	941	1209
n (#)	941	1477

KEYBOARD LAYOUT

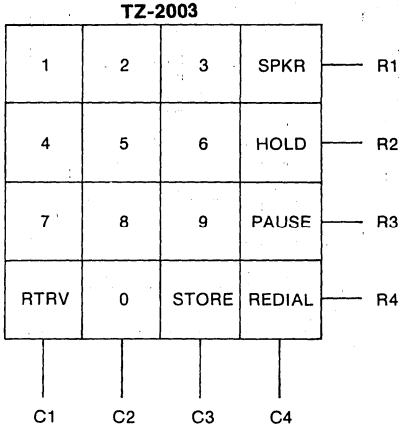
TZ-2001



TZ-2002



TZ-2003



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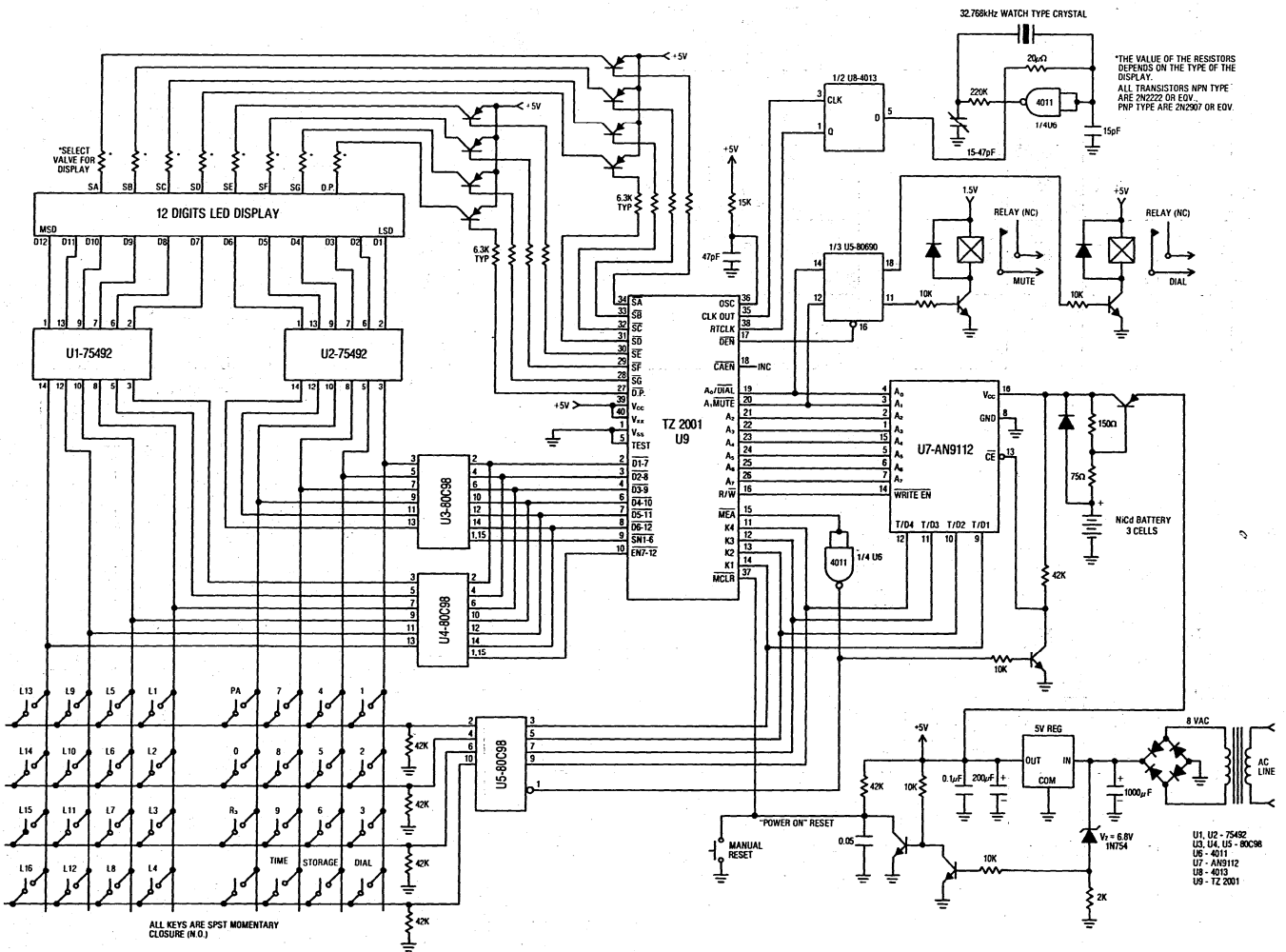
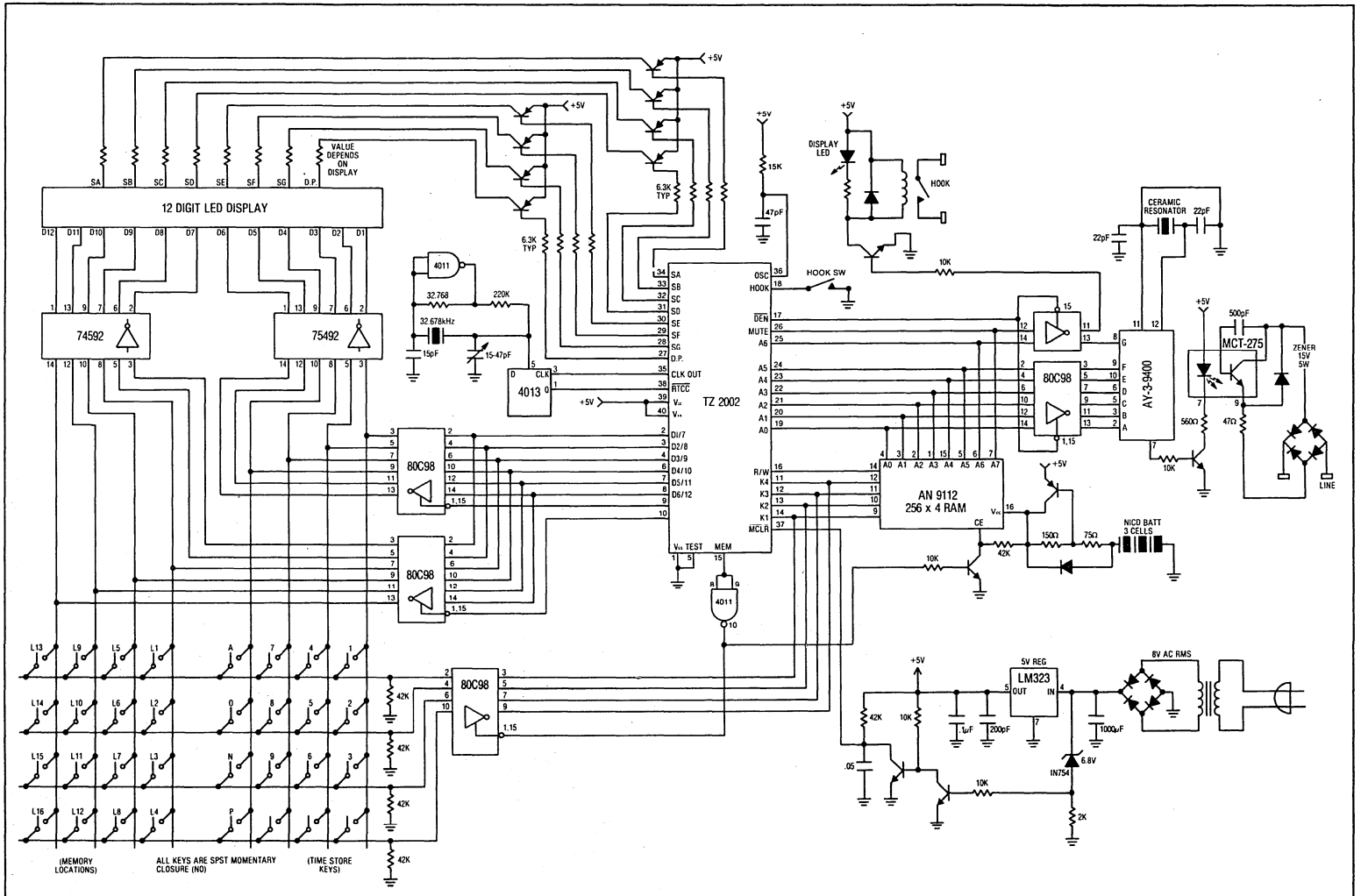
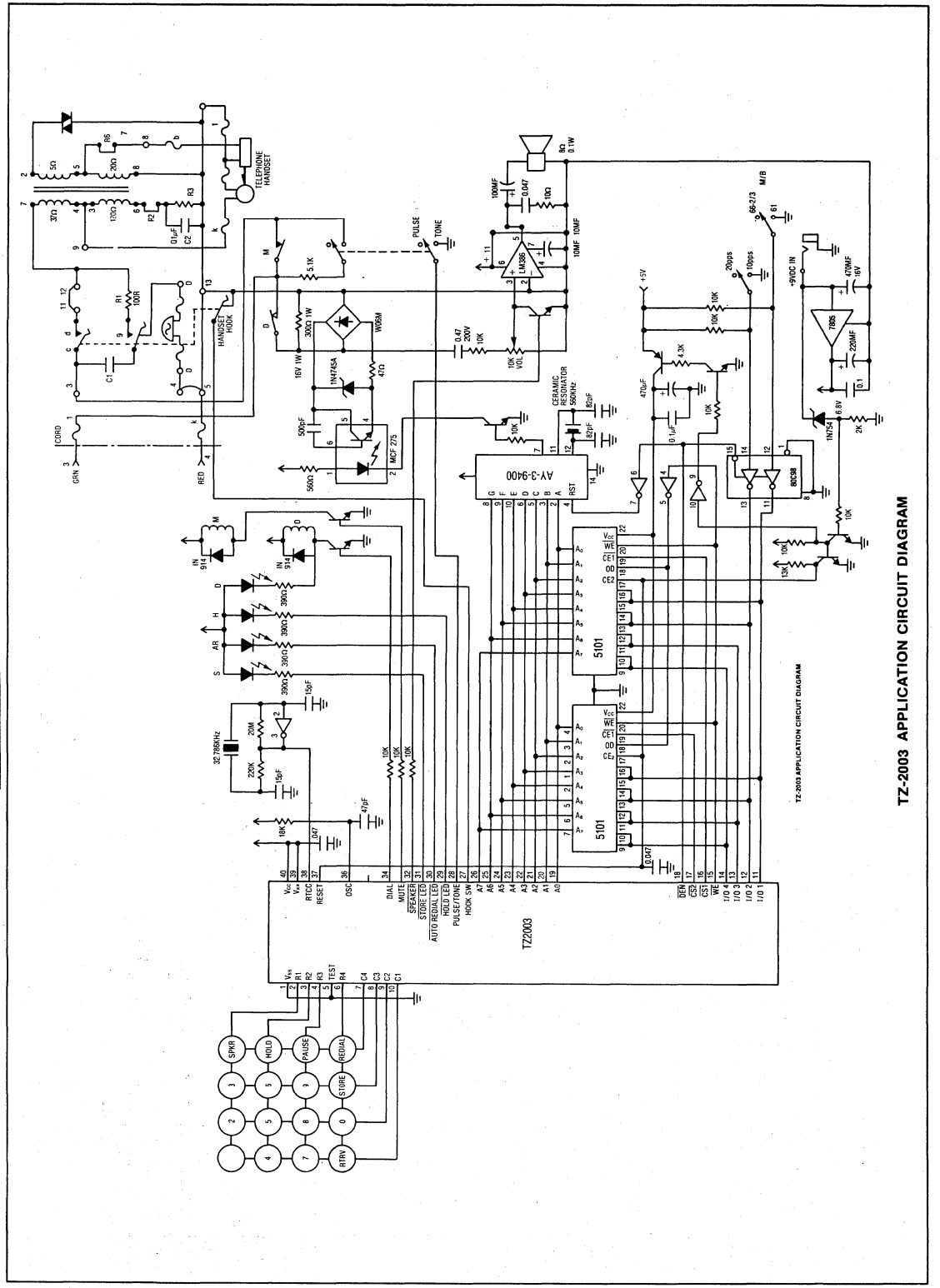


TZ-2001 APPLICATION CIRCUIT DIAGRAM (16 NUMBER REPERTORY STORAGE) WITH BATTERY BACK UP



TZ-2002 APPLICATION DIAGRAM



TZ-2003 APPLICATION CIRCUIT DIAGRAM

Telecom Hybrids

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
UNIVERSAL ACTIVE FILTERS	Generate any filter response by means of external connections.	ACF 7092C	6-52
LOW PASS FILTERS	PCM transmit filter.	ACF 7270C	6-56
	PCM receive filter.	ACF 7271C	6-58
BAND PASS FILTERS	Full wave detector and a factory tunable four pole fixed bandwidth band pass filter.	ACF 7300C ACF 7301C ACF 7302C	6-60 6-62 6-63
	Detects and passes the 2600Hz signalling frequency.	ACF 7310C	6-66
	DTMF/tone detection band pass filters.	ACF 7323C	6-68
		ACF 7363C	6-68
		ACF 7383C	6-68
	Detects and passes the 2800Hz signalling frequency.	ACF 7328C	6-70
BAND REJECTION FILTERS	Rejects the 2600Hz signalling frequency.	ACF 7410C	6-72
		ACF 7412C	6-73
		NCS 2061	6-74
	Rejects the 2800Hz signalling frequency.	NCS 2062	6-74
BAND SEPARATION FILTERS	Isolates low and high groups of DTMF frequencies.	ACF 7711C	6-75
	DTMF Low Group Band Splitting Filter	ACF 7720C	6-77
	DTMF High Group	ACF 7721C	6-78

Universal Active Filter

FEATURES

- Low Pass, High Pass, Band Pass, and Band Reject responses from the same unit
- Independent control of Frequency, Q and Amplifier Gain
- External resistors need not temperature track internal NPO capacitors
- 10Hz to 10kHz operating frequency range
- 0.5 to 50 adjustable Q range

DESCRIPTION

The schematic diagram for the ACF 7092C is shown in Figure 1. The filter is composed of 4 operational amplifiers. The first three form the basic state variable configuration (triad) and the fourth can be utilized for increased gain or in the biquadratic configuration with the addition of external components. Two filter inputs are provided; a non-inverting input and an inverting input.

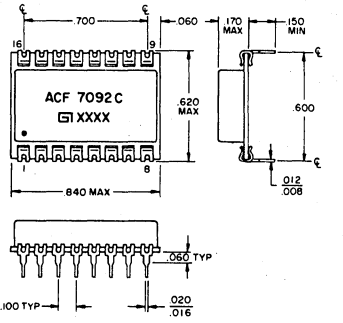
In the Triad configuration, amplifier A_1 is a summing amplifier providing the high pass output, amplifiers A_2 and A_3 are integrators providing band pass and low pass outputs. The external resistors establish the operating parameters for each filter mode. R_1 and R_2 determine the resonant frequency (Fn). R_7 and R_3 or R_7 and R_8 determine the values for gain and Q.

APPLICATIONS

General Instrument Hybrid universal active filters are low cost units that can be used to generate any filter response. Some common applications for these filters are found in sonar systems, telephone and paging systems, navigation systems, modems, transducers, biomedical measuring systems, process control equipment, data acquisition systems, radar systems, audio signal processing equipment and seismology.

PACKAGE INFORMATION
PIN CONFIGURATION

16 LEAD DUAL IN LINE
ACF 7092C



PIN	FUNCTION
1	A1(+IN)
2	A1 (—IN)
3	VHP
4	V+
5	VLP
6	A4 (+IN)
7	A3 (—IN)
8	NC
9	GND
10	A4 (—IN)
11	VO
12	V—
13	VBP
14	A2 (—IN)
15	NC
16	NC

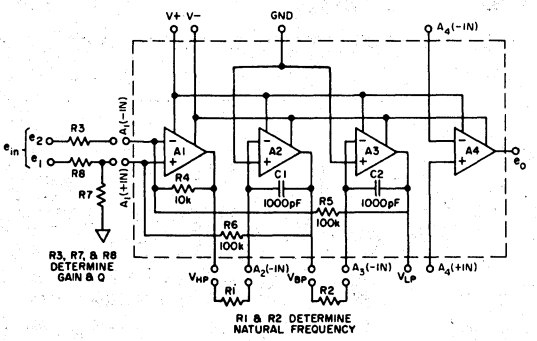


Fig. 1 SCHEMATIC

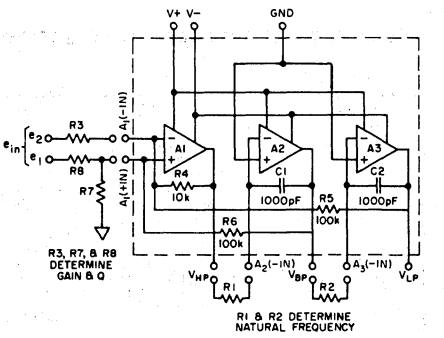


Fig. 2 TRIAD CONFIGURATION

TELECOM

ACTIVE FILTER DESIGN WITH UNIVERSAL FILTERS

TRIAD TRANSFER FUNCTIONS

The Triad configuration illustrated in Figure 2 gives transfer functions at the various points, HP, BP, and LP as shown in Table 1 for infinite gain band width operational amplifiers.

Table I TRANSFER FUNCTIONS

$$G_{HP}(s) = \frac{V_{HP}}{e_{IN}} = \frac{G_\infty S^2}{S^2 + \frac{Wn}{Q}S + Wn^2} \quad \text{HIGH PASS}$$

$$G_{BP}(s) = \frac{V_{BP}}{e_{IN}} = \frac{G_o \frac{Wn}{Q} S}{S^2 + \frac{Wn}{Q}S + Wn^2} \quad \text{BAND PASS}$$

$$G_{LP} = \frac{V_{LP}}{e_{IN}} = \frac{G(O)Wn^2}{S^2 + \frac{Wn}{Q}S + Wn^2} \quad \text{LOW PASS}$$

Fn = Wn/2π = Natural or corner frequency for low or high pass outputs. Center frequency for band pass output.

S = Transform variable

G_∞ = Gain at infinite frequency (high pass)

G_o = Gain at center frequency (band pass)

G(0) = Gain at zero frequency (low pass)

$$Q = \frac{\text{Center frequency}}{\text{Bandwidth}} \quad \text{BAND PASS}$$

$$Q = \frac{\text{Gain at Natural Frequency}}{\text{Gain at infinite Frequency}} \quad \text{HIGH PASS}$$

$$Q = \frac{\text{Gain at Natural Frequency}}{\text{Gain at DC}} \quad \text{LOW PASS}$$

DESIGN EQUATIONS

The design equations for the transfer functions listed in Table 1 are:

$$Wn = \sqrt{a_3 W_1 W_2} \qquad W_1 = \frac{1}{R_1 C_1} \quad W_2 = \frac{1}{R_2 C_2}$$

$$Q = \left[\frac{1}{a_2 (1 + a_4 + a_3)}\right]\sqrt{\frac{a_3 W_2}{W_1}} \qquad a_1 = \frac{1}{1 + \frac{R_8}{R_6} + \frac{R_8}{R_7}}$$

$$a_2 = \frac{1}{1 + \frac{R_6}{R_7} + \frac{R_6}{R_8}} \qquad a_3 = \frac{R_4}{R_5} \qquad a_4 = \frac{R_4}{R_3}$$

	Non-Inverting Figure 3	Inverting Figure 4
G_∞	$a_1 (1 + a_3 + a_4)$	$-a_4$
G_o	$-a_1/a_2$	$\frac{a_4}{a_2 (1 + a_4 + a_3)}$
G(O)	$\frac{a_1 (1 + a_3 + a_4)}{a_3}$	$-a_4/a_3$

Note:
Since operational amplifiers have finite gain-bandwidths, the Q will be greater than calculated. A correction factor will be required and will operate on the desired Fn Q product. See Step #1 of Triad tuning procedure.

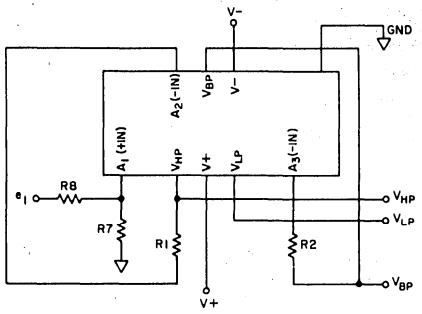


Fig. 3 NON-INVERTING CONFIGURATION

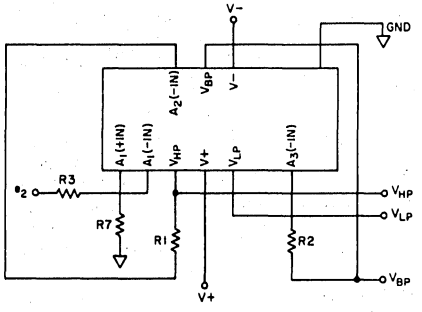


Fig. 4 INVERTING CONFIGURATION

TRIAD TUNING PROCEDURE

The following four step tuning procedure allows the selection of the external resistors R_1, R_2, R_7 and R_3 or R_8. The procedure is based on first selecting an output function (low-pass, band-pass or high-pass) and the inverting or non-inverting configuration. If other gains are desired the uncommitted operational amplifier can be used.

Step #1: Determine Design Q

Calculate the product of the desired Fn and Q. If this product exceeds 10,000 refer to Figure 5 to obtain the corresponding design FnQ. Divide the design FnQ product by Fn to determine the design Q for all subsequent calculations. The design Q now includes the effects of operational amplifier finite gain bandwidths.

If the desired FnQ product is less than 10,000, use the desired Q as the design Q for all subsequent calculations. The operational amplifier's finite gain-bandwidth in this lower FnQ region has a second order effect on the Q and can be ignored.

Step #2: Calculate R_3 or R_8 as a Function of Design Q

R_3 or R_8 can be calculated from the equations listed in Table II.

TELECOM

Table II R_8 OR R_3 CALCULATION

Configuration	Non-Inverting Figure 3	Inverting Figure 4
Low-Pass	$R_8 = \frac{316k\Omega}{Q\ design}$	$R_3 = 100k\Omega$
Band-Pass	$R_8 = \frac{Q\ desired\ (100k)}{Q\ design}$	$R_3 = Q\ design\ (31.6k\Omega)$
High-Pass	$R_8 = \frac{31.6k\Omega}{Q\ design}$	$R_3 = 10k\Omega$

Step #3: Calculate R_1 and R_2 as a Function of Fn

For basic unity gain configuration, $R_1 = R_2$.

$$R_1 = R_2 = \frac{5.04 \times 10^7}{Fn}$$

LOW FREQUENCY OPERATION

For very low frequencies (fn $\leq$ 50Hz) additional capacitance can be used to shunt the internal integrating capacitors from pins 5 to 7 and 13 to 14. R_1 and R_2 are then calculated as follows:

$$R_1 = R_2 = \frac{1}{2\pi Fn}\sqrt{\frac{R_4}{R_5 C_1 C_2}}$$

Step #4: Calculate R_7 as a Function of Design Q

R_7 can be calculated from the equations listed in Table III

Table III R_7 CALCULATIONS

Configuration	Non-Inverting Figure 3	Inverting Figure 4
Low-Pass	$R_7 = \frac{100k\Omega}{3.16\ (Q\ design) - 1}$	$R_7 = \frac{100k\Omega}{3.8\ (Q\ design) - 1}$
Band-Pass	$R_7 = \frac{100k\Omega}{3.48\ (Q\ design) - 2}$	$R_7 = \frac{100k\Omega}{3.48\ (Q\ design)}$
High-Pass	$R_7 = \frac{100k\Omega}{0.32\ (Q\ design) - 1}$	$R_7 = \frac{100k\Omega}{6.64\ (Q\ design) - 1}$

BIQUAD TRANSFER FUNCTION

The BIQUAD configuration for generating Cauer or Band Reject responses is shown in Figure 6.

The transfer function is:

$$\frac{e_o}{e_{IN}} = A\left[\frac{S^2 + aWnS + bWn^2}{S^2 + \frac{Wn}{Q}S + Wn^2}\right]$$

The parameters for the Transmission Zeros (numerator) are given by:

$$a = \frac{R_{13}}{R_{14}}\sqrt{\frac{R_5}{R_4}} \qquad A = -\left(\frac{R_{14}}{R_{13}}\right) \times \left(\frac{R_4}{R_5}\right) \times G(O)$$

$$b = \frac{R_{13}}{R11} \times \frac{R5}{R_4}$$

provided that $R_{12}R_{14} = R_{15}\left(\frac{R_{11}R_{13}}{R_{11} + R_{13}}\right)$

The tuning procedure for Wn and Q is the same as in the TRIAD configuration.

A Band Reject filter can be obtained by making Constant (b) = 1 and R_{12} infinite which makes the Constant (a) = zero. The transfer function then becomes:

$$\frac{e_o}{e_{IN}} = \frac{S^2 + Wn^2}{S^2 + \frac{WnS}{Q} + Wn^2}$$

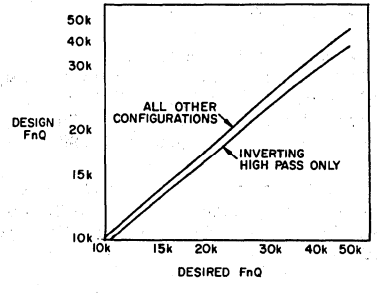


Fig. 5 FnQ CORRECTION

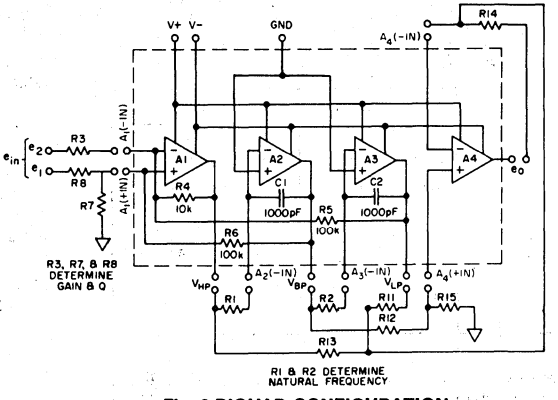


Fig. 6 BIQUAD CONFIGURATION

PERFORMANCE SPECIFICATIONS

MAXIMUM RATINGS *

Supply Voltages ..... ±18V
Supply Current (±15 Volt Supplies) ..... ±7.5mA
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -55°C to +125°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

ELECTRICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, these parameters apply over a temperature range of 0°C to +70°C with ± 15 VDC supplies

Characteristic	Min	Typ	Max.	Units	Conditions
FnQ Product	5	—	50,000	—	
Fn Range	10	—	10,000	Hz	Self Resonant Frequency
Fn Accuracy	—	± 1.5	±2.5	%	Note 1, T_A = 25°C
Fn Temp. Coeff.	—	± 40	±75	ppm/°C	Note 2
Q Range	0.5	—	50	—	
Q Accuracy	—	± 7	—	%	
Q Temp. Stability	—	± FnQ×10^{-6}	—	%	0°C ≤ T_A ≤ 70°C
Pass band gain	1	—	10	—	Note 3
Input offset voltage	—	2	10	mV	T_A =25°C
	—	—	15	mV	0°C ≤ T_A ≤ 70°C
Input offset current	—	5	200	nA	T_A = 25°C
	—	—	300	nA	0°C ≤ T_A ≤ 70°C
Input bias current	—	40	500	nA	T_A = 25°C
	—	—	800	nA	0°C ≤ T_A ≤ 70°C
Input voltage range	± 12	± 14	—	V	
Input Resistance	0.3	5	—	MΩ	
Large Signal Voltage Gain	20,000	300,000	—	—	RL ≥ 2K, Vo = ± 10V, T_A = 25°C
	15,000	—	—	—	RL ≥ 2K, Vo = ± 10V, 0°C < T_A < 70°C
Supply Voltage Rejection Ratio	—	30	300	μV/V	
Output Resistance	—	—	100	Ω	
Load Resistance	1,000	—	—	Ω	
Output Voltage Swing	—	—	20	V P-P	
	—	—	8	V P-P	Fn = 10Hz to 1kHz, Band pass
	—	—	2	V P-P	Fn = 10Hz to 1kHz, High pass
	—	—	8	V P-P	Fn = 10kHz, Low pass
	—	—	3	V P-P	Fn = 10kHz, Band pass
	—	—	0.8	V P-P	Fn = 10kHz, High pass
Common mode rejection ratio	70	90	—	dB	

Note 1: The 25°C Fn accuracy is determined by the internal capacitor tolerance (± 1%), and the R_4/R_5 tolerance (±2%) and does not include the tolerance of the external resistors R1 and R2.

Note 2: The internal capacitors have a temperature coefficient of ±30ppm/°C. The remaining portion of the temperature coefficient is due to the change of the operational gain band width products over temperature.

Note 3: Gain greater than 1 can be provided with the uncommitted amplifier.

PCM Transmit Low Pass Filter

FEATURES

- Pass band ripple: ±0.125dB, from 300 to 3kHz, 0° to 70°C
- Stop band attenuation: 32dB, 4.2kHz to 100kHz
- Insertion Loss: 0dB
- Wide power supply range: ±12VDC to ±15VDC

DESCRIPTION

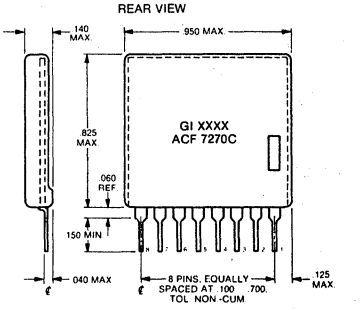
The ACF 7270C is a linear hybrid low pass active filter with a Cauer type response (transfer function based on elliptic functions). The hybrid will pass a signal in the pass band with ±.125 dB ripple to 3kHz and be 32 dB down at 4.2kHz with equal rejection out to 100kHz. The filter is designed to be used in PCM transmit applications.

MAXIMUM RATINGS

V_{CC} ..... ±18VDC
Input Voltage ..... ±15VDC
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... 0°C to +70°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	Input	5	N.C.
2	N.C.	6	V_{CC}
3	GND	7	$-V_{CC}$
4	N.C.	8	Output

ELECTRICAL CHARACTERISTICS

$0°C \leq T_A \leq 70°C$
$V_{CC} = +12$ to $+15$VDC
$-V_{CC} = -12$ to -15VDC

Characteristic	Min	Typ	Max	Units	Conditions
Gain	−.125	0	+.125	dB	f = 1kHz
Passband ripple	−.125	0	+.125	dB	f = 300-3kHz, ref 1kHz
Passband response	−.5	0	+.2	dB	f = 3kHz-3.4kHz, ref 1kHz
Transition atten.	15	18	—	dB	f = 4kHz, ref 1kHz
Stop band atten.	32	35	—	dB	f = 4.2kHz
Low freq 3dB pt	20	40	50	Hz	ref. 1kHz
Differential delay	—	78	90	μs	1kHz, 2.6kHz
Output noise	—	0	6	dBrnc	input grounded
Distortion	—	0.1	0.25	%	1kHz
Output swing	10	12	—	Vp-p	RL = 2K, $V_{CC} = +15$VDC, $-V_{CC} = -15$VDC
Input impedance	100k	1meg	—	Ω	DC to 10kHz
Output impedance	—	1	5	Ω	DC to 10kHz
Supply current	—	10	15	mA	

NOTES:

1. Specifications apply with an input of 0dBm Ref 600Ω.
2. To obtain the full signal range, the filter should be driven from a source with a nominal DC voltage of 0V.
3. The source must provide a DC path to ground of not more than 10K.

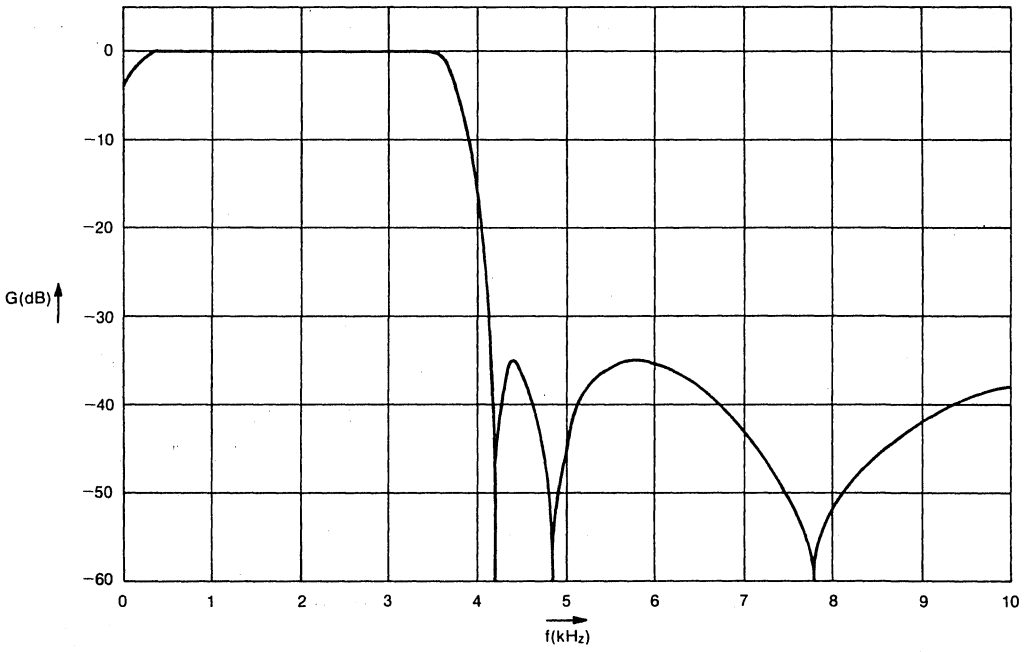


Fig.1 TYPICAL FREQUENCY RESPONSE

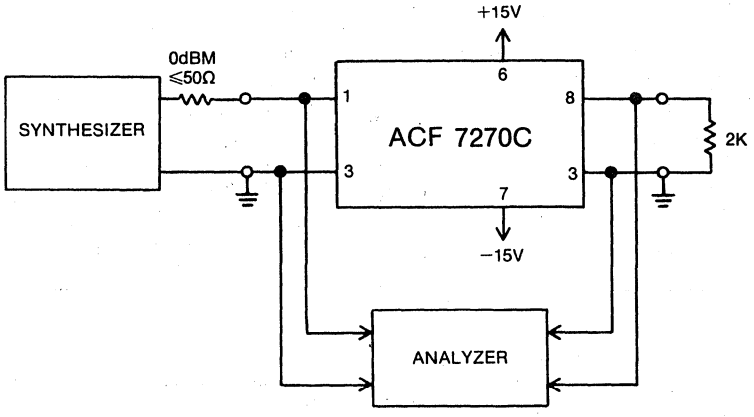


Fig. 2 TEST CIRCUIT

PCM Receive Low Pass Filter

FEATURES

- Pass band ripple: ±0.125dB, from 300 to 3kHz, 0° to 70°C
- Stop band attenuation: 32dB, 4.2kHz to 100kHz
- Insertion Loss: 0 dB
- Wide power supply range: ±12VDC to ±15VDC

DESCRIPTION

The ACF 7271C is a linear hybrid low pass active filter with a Cauer type response (transfer function based on elliptic functions). The hybrid will pass a signal in the pass band with ±.125dB ripple to 3kHz and be 32dB down at 4.2kHz with equal rejection out to 100kHz. The filter is designed to be used in PCM receive applications.

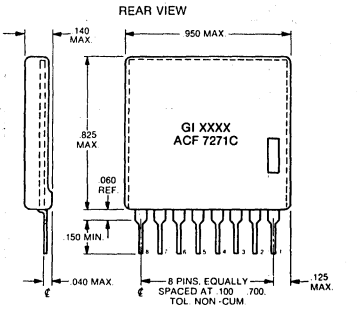
MAXIMUM RATINGS *

V_{CC}	±18VDC
Input Voltage	±15VDC
Storage Temperature	−55°C to +125°C
Operating Temperature	0°C to +70°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

PACKAGE INFORMATION

PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	Internal Connection	5	V_{CC}
2	Input	6	N.C.
3	GND	7	$-V_{CC}$
4	N.C.	8	Output

ELECTRICAL CHARACTERISTICS

$0°C \leq T_A \leq 70°C$
$V_{CC} = +12$ to $+15$VDC
$-V_{CC} = -12$ to -15VDC

Characteristic	Min	Typ	Max	Units	Conditions
Gain	−.125	0	+.125	dB	f = 1kHz
Passband ripple	−.125	0	+.125	dB	f = 300-3kHz, ref 1kHz
Passband response	−.5	0	+.2	dB	f = 3kHz-3.4kHz, ref 1kHz
Transition atten.	15	18	—	dB	f = 4kHz, ref 1kHz
Stop band atten.	32	35	—	dB	f = 4.2kHz
Differential delay	—	85	95	μs	1kHz, 2.6kHz
Output noise	—	0	6	dBrnc	input grounded
Distortion	—	0.1	0.25	%	1kHz
Output swing	10	12	—	Vp-p	RL = 2K, $V_{CC} = +15$VDC, $-V_{CC} = -15$VDC
Input impedance	130	140	—	kΩ	DC to 10kHz
Output impedance	—	1	5	Ω	DC to 10kHz
Supply current	—	10	15	mA	

NOTES:

1. Specifications apply with an input of 0dBm Ref 600Ω.
2. To obtain the full signal range, the filter should be driven from a source with a nominal DC voltage of 0V.
3. The source must provide a DC path to ground of not more than 10K.
4. Frequency response data is multiplied by sin x/x response.

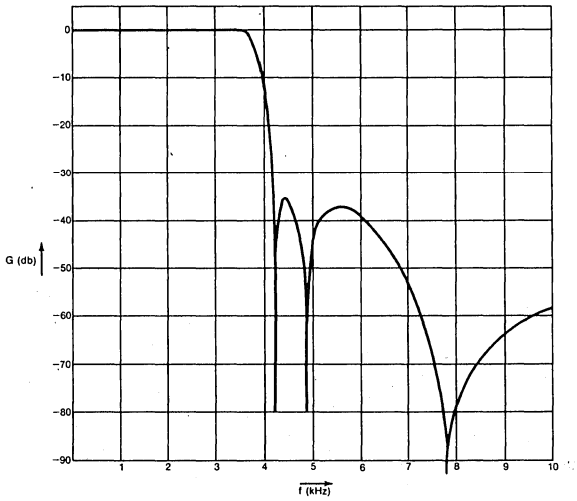


Fig. 1 TYPICAL FREQUENCY RESPONSE MULTIPLIED BY SIN X/X

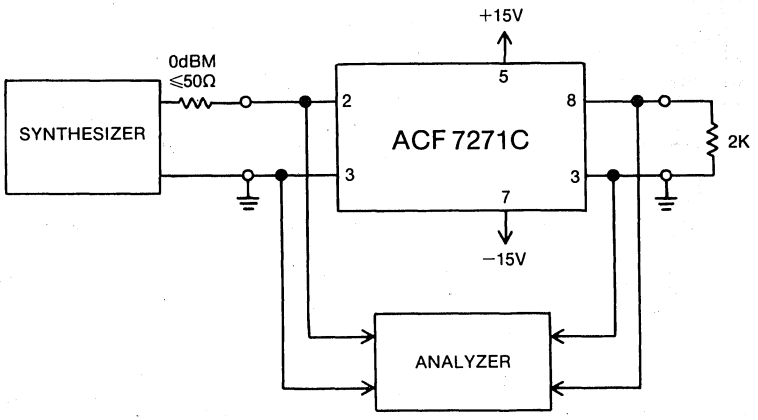


Fig. 2 TEST CIRCUIT

Band Pass Filter and Full Wave Detector

FEATURES

- Low Power Dissipation
- Can be operated from a single ended power system
- 20dB minimum attenuation at stop band frequencies
- 0dB Insertion loss in pass band
- Fixed band width filter
- Internal full wave detector

DESCRIPTION

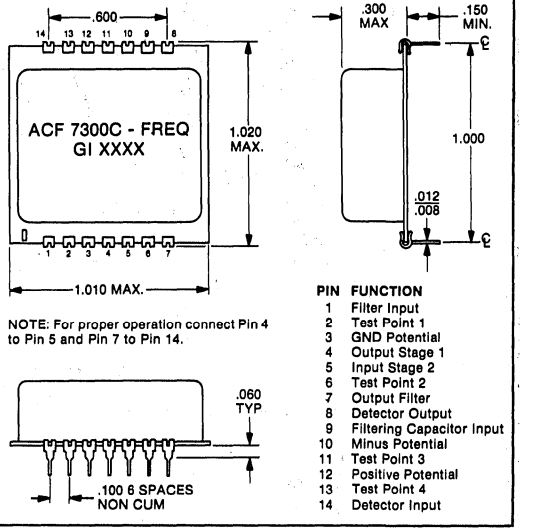
The ACF 7300C consists of a four (4) pole, fixed band width, band pass filter, factory tunable over a center frequency (F_O) range of 540Hz to 1980Hz, and a full wave detector. This RC active filter and detector is packaged in a dual in line package. Only one external capacitor is required for filtering the detector output, the balance of the circuitry is self contained requiring no additional components for proper operation.

MAXIMUM RATINGS *

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

PACKAGE INFORMATION
PIN CONFIGURATION



NOTE: For proper operation connect Pin 4 to Pin 5 and Pin 7 to Pin 14.

PIN	FUNCTION
1	Filter Input
2	Test Point 1
3	GND Potential
4	Output Stage 1
5	Input Stage 2
6	Test Point 2
7	Output Filter
8	Detector Output
9	Filtering Capacitor Input
10	Minus Potential
11	Test Point 3
12	Positive Potential
13	Test Point 4
14	Detector Input

ELECTRICAL CHARACTERISTICS (unless otherwise specified)

V_{CC} = ±12 Volts
0°C to +70°C
Filter Load Resistance = 5kΩ
Detector Load Resistance = 5kΩ
Source Impedance, Filter or Detector = 50Ω

Characteristic	Min.	Typ.	Max.	Units	Conditions
Filter					
Input Impedance	—	2	—	kΩ	
Voltage Gain					See Figure 1.
	—	0	1.5	±dB	Ideal Center Frequency (F_O)
	—	0	1.5	±dB	Pass Band (±10Hz from F_O)*
	-20	—	—	dB	Stop Band (±110Hz from F_O)*
Input Voltage	5	—	—	V_{RMS}	
Output Impedance	—	—	25	Ω	
Detector					
Input Impedance	25	—	—	kΩ	
Input Voltage	5	—	—	V_{RMS}	
Voltage Gain	0.95	1.0	1.05	VDC/V_{RMS}	See Figure 2.
Output Impedance	—	—	25	Ω	
Output Offset Voltage	—	—	20	mVolts	
Power Supply Current	—	1.5	3.0	mA	

*Referenced to Gain at F_O.
Standard factory tuned filters available with the following ideal center frequencies:
540Hz, 660Hz, 780Hz, 900Hz, 1020Hz, 1140Hz, 1380Hz, 1500Hz, 1620Hz, 1740Hz, 1860Hz, and 1980Hz. To order one of the above tuned filters, specify the device as follows; ACF 7300C - Frequency. e.g. ACF 7300C - 0540
Other factory tuned frequencies are available upon request and nominal set up charge.

TELECOM

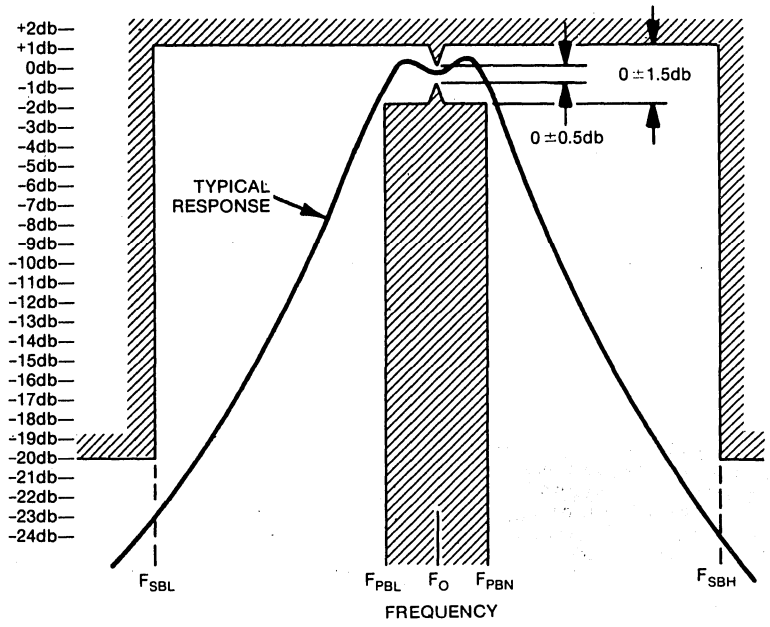


Fig.1 FREQUENCY RESPONSE

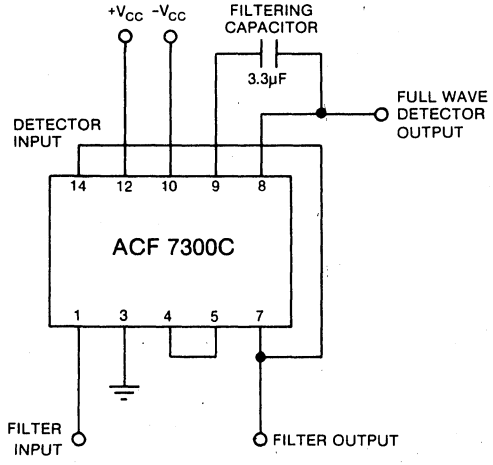


Fig.2 TYPICAL APPLICATION

Table I

Center Frequency (FO)(Hz)	Low Stop Band Frequency (FSBL)(Hz)	Low Pass Band Frequency (FPBL)(Hz)	High Pass Band Frequency (FPBH)(Hz)	High Stop Band Frequency (FSBH)(Hz)
540	430	530	550	650
660	550	650	670	770
780	670	770	790	890
900	790	890	910	1010
1020	910	1010	1030	1130
1140	1030	1130	1150	1250
1380	1270	1370	1390	1490
1500	1390	1490	1510	1610
1620	1510	1610	1630	1730
1740	1630	1730	1750	1850
1860	1750	1850	1870	1970
1980	1870	1970	1990	2090

Band Pass Filter and Full Wave Detector

FEATURES

- Low Power Dissipation
- Can be operated from a single ended power system
- 0db Insertion loss in pass band
- 20dB minimum attenuation at stop band frequencies
- Fixed band width filter
- Internal full wave detector

DESCRIPTION

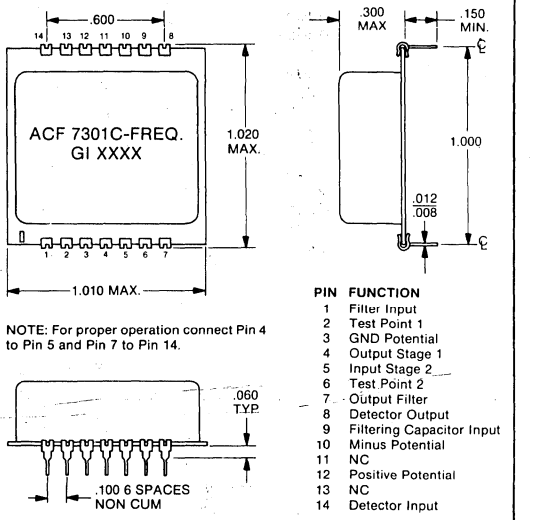
The ACF 7301C consists of a four (4) pole, fixed band width, band pass filter, factory tunable over a center frequency (F_o) range of 700Hz to 1700Hz, and a full wave detector. This RC active filter and detector is packaged in a dual in line package. Only one external capacitor is required for filtering the detector output, the balance of the circuitry is self contained requiring no additional components for proper operation.

MAXIMUM RATINGS *

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70° C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

PACKAGE INFORMATION
PIN CONFIGURATION



NOTE: For proper operation connect Pin 4 to Pin 5 and Pin 7 to Pin 14.

PIN	FUNCTION
1	Filter Input
2	Test Point 1
3	GND Potential
4	Output Stage 1
5	Input Stage 2
6	Test Point 2
7	Output Filter
8	Detector Output
9	Filtering Capacitor Input
10	Minus Potential
11	NC
12	Positive Potential
13	NC
14	Detector Input

ELECTRICAL CHARACTERISTICS (unless otherwise specified)

V_{CC} = ±12 Volts
0°C to +70°C
Load Resistance, Filter Output or Detector Output = 5k ohms
Source Impedance, Filter Input or Detector Input = 50Ω

Characteristic	Min	Typ	Max	Units	Conditions
Filter					
Input Impedance	—	2	—	kΩ	
Voltage Gain					See Figure 1
	—	0	1.5	±dB	Ideal Center Frequency (F_O)
	—	0	2.5	±dB	Pass Band (±15Hz from F_O)*
	-20	—	—	dB	Stop Band (±185Hz from F_O)*
Input Voltage	5	—	—	V_{RMS}	
Output Impedance	—	—	25	Ω	
Detector					
Input Impedance	25	—	—	kΩ	
Input Voltage	5	—	—	V_{RMS}	
Voltage Gain	0.95	1.0	1.05	VDC/V_{RMS}	See Figure 2.
Output Impedance	—	—	25	Ω	
Output Offset Voltage	—	—	20	mVolts	
Power Supply Current	—	1.5	3.0	mA	

* Referenced to Gain at F_O.

Standard factory tuned filters available with the following ideal center frequencies: 700Hz, 900Hz, 1100Hz, 1300Hz, 1500Hz, and 1700Hz. To order one of the above tuned filters, specify the device as follows; ACF 7301C \ Frequency. e.g. ACF 7301C – 0700. Other factory tuned frequencies are available upon request and a nominal set up charge.

TELECOM

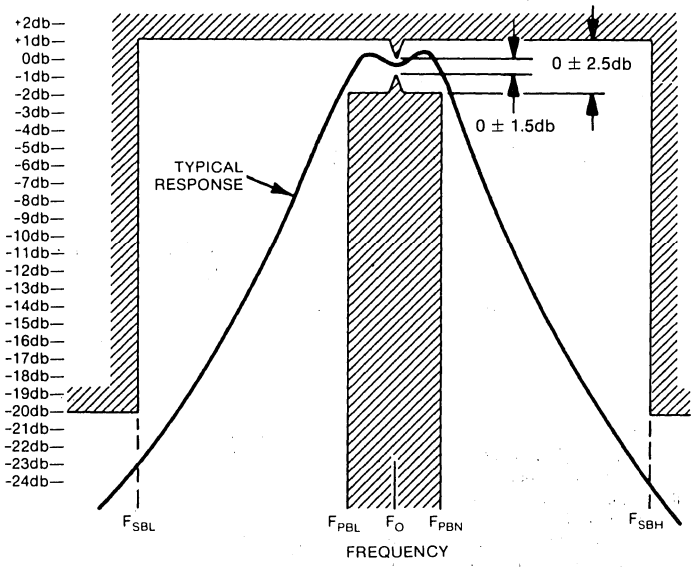


Fig.1 FREQUENCY RESPONSE

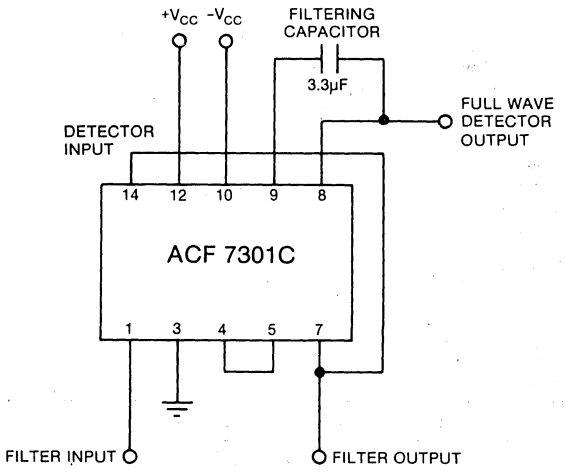


Fig.2 TYPICAL APPLICATION

TABLE 1

Center Frequency (FO) (Hz)	Low Stop Band Frequency (FSBL) (Hz)	Low Pass Band Frequency (FPBL) (Hz)	High Pass Band Frequency (FPBH) (Hz)	High Stop Band Frequency (FBBH) (Hz)
700	505	685	715	885
900	715	885	915	1085
1100	915	1085	1115	1285
1300	1115	1285	1315	1485
1500	1315	1485	1515	1685
1700	1515	1685	1715	1895

Band Pass Filter and Full Wave Detector

FEATURES

- Low Power Dissipation
- Can be operated from a single ended power system
- 22dB minimum attenuation at stop band frequencies
- 0dB Insertion loss in pass band
- Fixed band width filter
- Internal full wave detector

DESCRIPTION

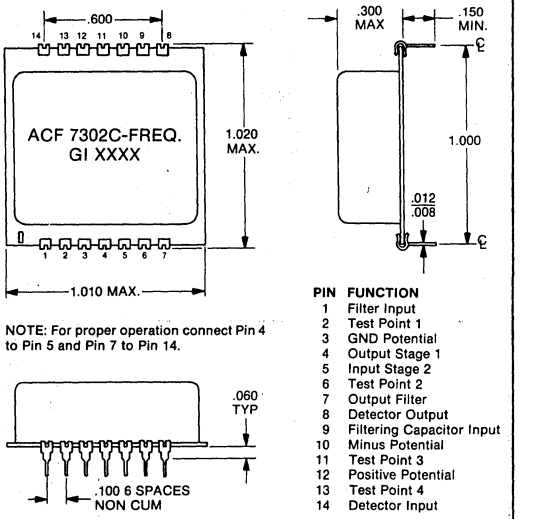
The ACF 7302C consists of six (6) pole, fixed band width, band pass filter, factory tunable over a center frequency (F_O) range of 2280Hz to 2600Hz, and a full wave detector. This RC active filter and detector is packaged in a dual in line package. Only one external capacitor is required for filtering the detector output, the balance of the circuitry is self contained requiring no additional components for proper operation.

MAXIMUM RATINGS *

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

PACKAGE INFORMATION
PIN CONFIGURATION



NOTE: For proper operation connect Pin 4 to Pin 5 and Pin 7 to Pin 14.

PIN	FUNCTION
1	Filter Input
2	Test Point 1
3	GND Potential
4	Output Stage 1
5	Input Stage 2
6	Test Point 2
7	Output Filter
8	Detector Output
9	Filtering Capacitor Input
10	Minus Potential
11	Test Point 3
12	Positive Potential
13	Test Point 4
14	Detector Input

TELECOM

ELECTRICAL CHARACTERISTICS (unless otherwise specified)

V_{CC} = ±12 Volts
0°C to +70°C
Filter and Detector Load Resistance = 5k ohms
Filter and Detector Source Impedance = 50Ω

Characteristic	Min	Typ	Max	Units	Conditions
Filter					
Input Impedance	—	2	—	kΩ	
Voltage Gain					See Figure 1.
	—	0	1.5	±dB	Ideal Center Frequency (F_O)
	—	0	1.5	±dB	Pass Band (±15Hz from F_O)*
	-22	—	—	dB	Stop Band (±120Hz from F_O)*
Input Voltage	5	—	—	V_{RMS}	
Output Impedance	—	—	25	Ω	
Detector					
Input Impedance	25	—	—	kΩ	
Input Voltage	5	—	—	V_{RMS}	
Voltage Gain	0.95	1.0	1.05	VDC/V_{RMS}	See Figure 2.
Output Impedance	—	—	25	Ω	
Output Offset Voltage	—	—	20	mVolts	
Power Supply Current	—	3.0	5.0	mA	

*Referenced to Gain at F_O.

Standard factory tuned filters available with the following ideal center frequencies: 2280Hz, 2400Hz, 2600Hz. To order one of the above tuned filters, specify the device as follows: ACF 7302 C - Frequency. e.g. ACF 7302C - 2280. Other factory tuned frequencies are available upon request and a nominal set up charge.

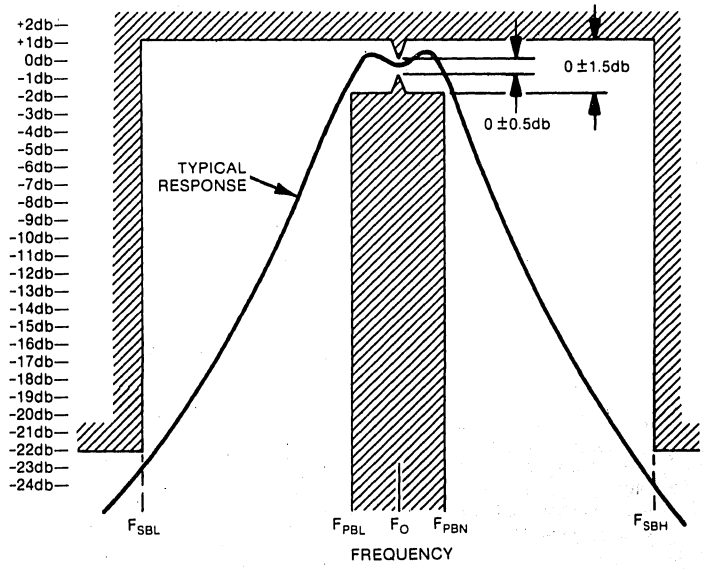


Fig.1 FREQUENCY RESPONSE

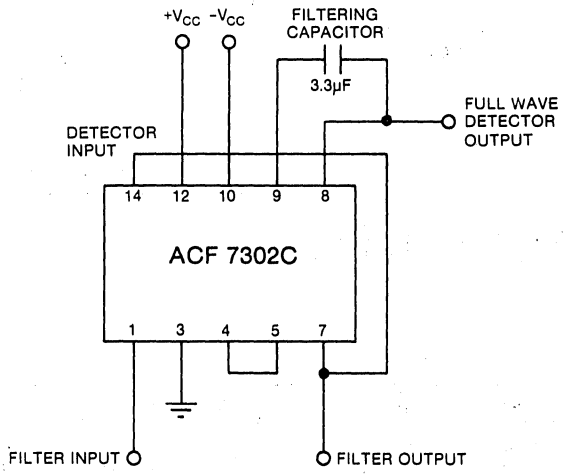


Fig.2 TYPICAL APPLICATION

Table I

Center Frequency (FO) (Hz)	Low Stop Band Frequency (FSBL) (Hz)	Low Pass Band Frequency (FPBL) (Hz)	High Pass Band Frequency (FPBH) (Hz)	High Stop Band Frequency (FBBH) (Hz)
2280	2160	2265	2295	2400
2400	2280	2385	2415	2520
2600	2480	2585	2615	2720

2600Hz Band Pass Filter

FEATURES

- 0dB Insertion Loss
- Narrow Band Width
- High Out of Band Attenuation
- Can be operated with single-ended power system

DESCRIPTION

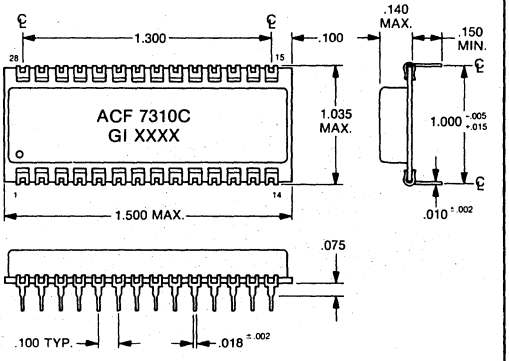
The ACF 7310C is a linear hybrid band pass RC active filter. The ACF 7310C is a sharply tuned filter designed to detect and pass the 2600Hz signaling frequency. This filter provides for a minimum attenuation of 30dB, plus and minus 200Hz from the ideal center frequency. The filter is self contained and requires no external components for proper operation. This filter is packaged in a dual in line configuration.

MAXIMUM RATINGS *

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±8 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1.	Input	10.	Stage 2 Input	20.	NC
2.	NC	11.	NC	21.	NC
3.	NC	12.	Stage 2 Output	22.	-12 VDC
4.	NC	13.	NC	23.	NC
5.	NC	14.	Output	24.	+12 VDC
6.	GND	15.	Stage 3 Input	25.	NC
7.	NC	16.	NC	26.	Stage 1 Output
8.	NC	17.	NC	27.	NC
9.	NC	18.	NC	28.	NC
		19.	NC		

NOTE: For proper operation connect Pin 26 to Pin 10, Pin 12 to Pin 15.

TELECOM

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

V_{CC} = ±12 Volts
T_A = 25°C
R_S = 50
R_L = 10K

Characteristic	Min	Typ	Max	Units	Conditions
Voltage Gain	−1.25	0	+1.75	dB	Ideal Center Frequency (F_O), 2600Hz
Frequency Response					Referenced from F_O Gain
	-70	—	—	dB	DC to 1600Hz
	-50	—	—	dB	2100Hz
	-30	—	—	dB	2400Hz
	-3	—	—	dB	2540Hz
	—	—	-3	dB	2560Hz
	—	—	-3	dB	2640Hz
	-3	—	—	dB	2660Hz
	-30	—	—	dB	2800Hz
	-50	—	—	dB	3100Hz
	-70	—	—	dB	3600Hz to 50kHz
Ripple	—	—	+0.5	dB	2541Hz to 2659Hz (Reference Fig. 1)
Input Impedance	25	—	—	kΩ	
Output Offset Voltage	—	—	20	mV	
Output Impedance	—	—	25	Ω	
Harmonic Distortion	—	—	1.0	%	V_{OUT} = 10 V_{PP}, Freq. = 2600Hz
Current Drain	—	8	15	mA	

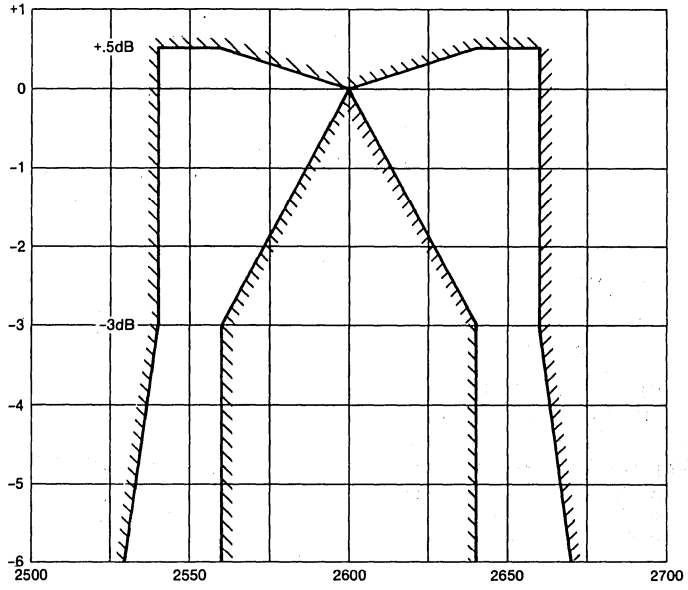


Fig.1 ACF 7310C PASS BAND ATTENUATION LIMITS EXPANDED

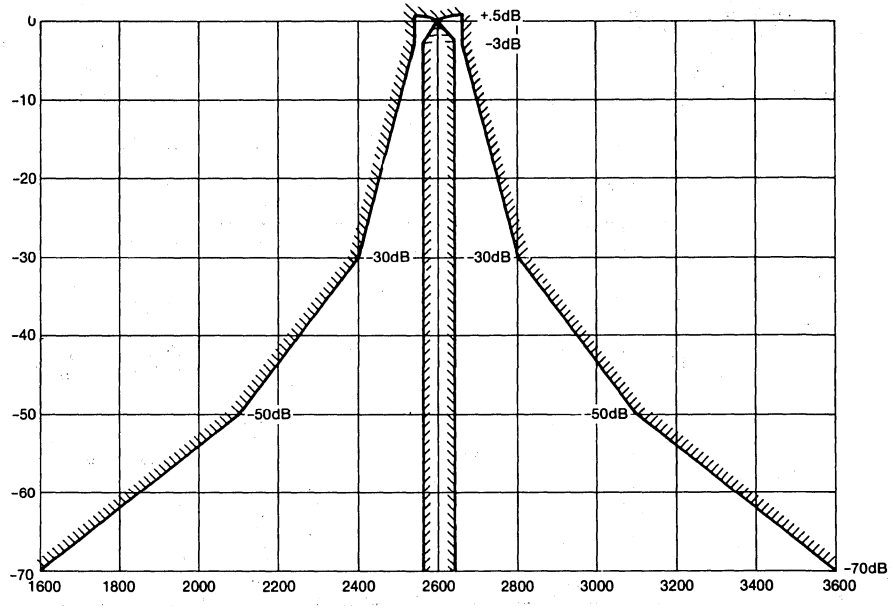


Fig.2 ACF 7310C PASS BAND ATTENUATION LIMITS

DTMF Tone Detection Band Pass Filter

FEATURES

- Standard model tone frequency settings of 697, 770, 852, 941, 1209, 1336, 1477 and 1633 and MF frequencies of 700, 900, 1100, 1300, 1500, 1700
- ± 0.3% F_O tolerance
- ± 0.0075%/°C F_O temperature coefficient
- ±0.1%/°C Q temperature coefficient
- Preset Q, 22 ±10% (4.5% B.W.)
- Filter design factory tunable over F_O range of 500 to 3kHz and Q range of 10 to 30
- Low power consumption 72mW max at ±12VDC
- Can be operated with single-ended power supplies

DESCRIPTION

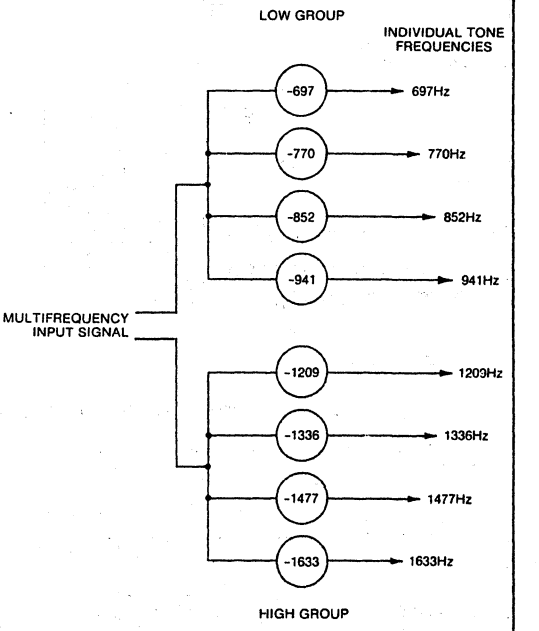
The General Instrument ACF 7323C/ACF 7363C/ACF 7383C Band Pass Active Filters are pre-tuned active filters designed specifically for tone receiver applications. These filters are available in hermetically sealed 12-lead TO-8, D.D.I.L., and S.I.L. packages.

Maximum Ratings *

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±8 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

TYPICAL APPLICATION
8-SECTION TONE FILTER



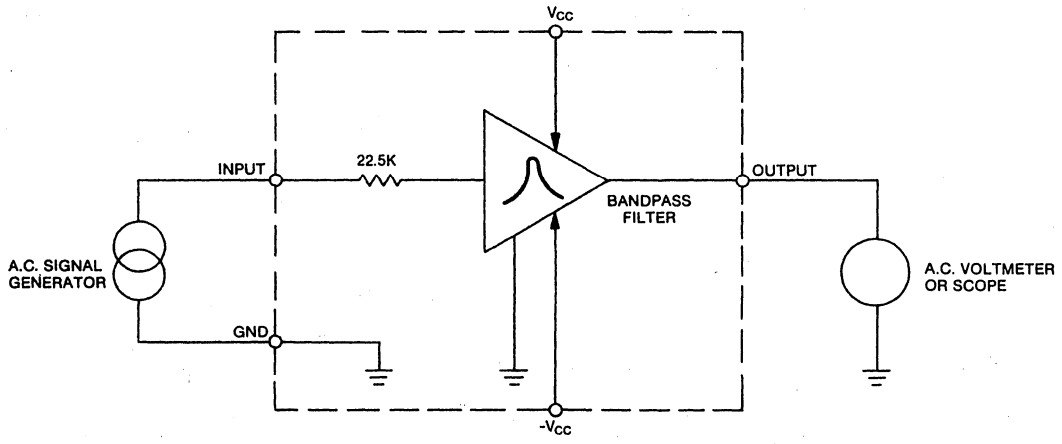
ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

$+V_{CC}$ = +12V,
$-V_{CC}$ = −12V

Characteristic	Min	Typ	Max.	Units	Conditions
Frequency Range	500	—	3000	Hz.	Note 1
Q Range	10	—	30	—	Note 1
F_O Accuracy	—	±0.2	±0.3	%	
F_O Temp Coef	—	± 35	± 75	ppm/°C	(0°C to 70°C)
Q Accuracy	—	—	±10	%	
Q Temp Coef	—	±500	±1000	ppm/°C	(0°C to 70°C)
Voltage Gain	-1	0	+1	dB	@F_O (0°C to 70°C)
Input Impedance	22.5	30	—	kΩ	
Output voltage	—	7	—	V_{RMS}	
Output Impedance	—	—	1	Ω	10 to 10kHz
Output Noise	—	0.25	0.75	mV_{RMS}	10 to 10kHz
Output Offset Voltage	—	±40	±60	mV	
Positive Supply Voltage	+5	+12	+18	V	
Negative Supply Voltage	-5	-12	-18	V	
Power Supply Current @±15V	—	1.5	3.0	mA	
Operating Temp Range	0	—	70	°C	
Storage Temp Range	-55	—	150	°C	

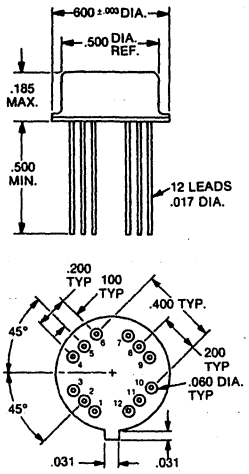
NOTE 1:
For the eight standard models, Q is preset to 22 and F_o is preset at the tone frequencies: 697, 770, 852, 941, 1209, 1336, 1477 and 1633. The model number designation is ACF 73XXC — F_o (e.g., ACF 7323C—0697). Other values of Q are indicated by a dash number (e.g., ACF 7323C—0697—18).

TEST CIRCUIT



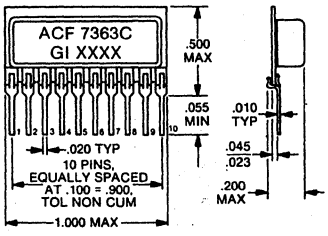
PACKAGE INFORMATION
PIN CONFIGURATION

ACF 7323C



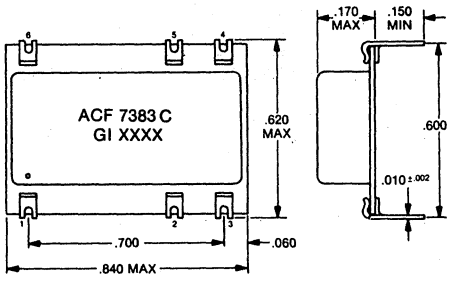
PIN FUNCTION
1. NC
2. NC
3. GND
4. Input Test Point
5. Input
6. NC
7. NC
8. NC
9. NC
10. Output
11. -Vcc
12. +Vcc

ACF 7363C



PIN FUNCTION
1. NC
2. Input
3. Test Point
4. NC
5. NC
6. -Vcc
7. GND
8. +Vcc
9. Output
10. NC

ACF 7383C



PIN FUNCTION
1. GND
2. Input Test Point
3. +Vcc
4. -Vcc
5. Output
6. Input

TELECOM

2800Hz Band Pass Filter

FEATURES

- 0dB Insertion Loss
- Low Power Dissipation
- Narrow Band Width
- High Out of Band Attenuation
- Can be operated with single-ended power system

DESCRIPTION

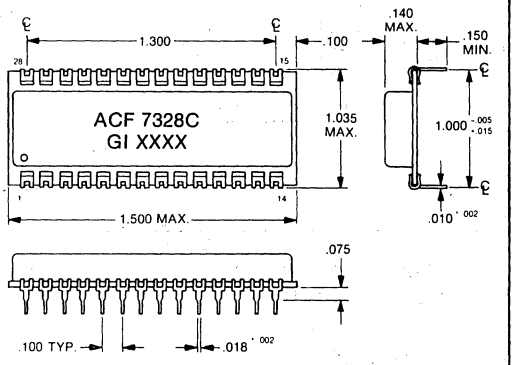
The ACF 7328C is a linear hybrid band pass RC active filter. The ACF 7328C is a sharply tuned filter designed to detect and pass the 2800Hz signaling frequency. This filter provides for a minimum attenuation of 30dB, plus and minus 200Hz from the ideal center frequency. The filter is self contained and requires no external components for proper operation. This filter is packaged in a dual in line configuration.

MAXIMUM RATINGS *

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±8 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1.	Input	10.	Stage 2 Input	20.	NC
2.	NC	11.	NC	21.	NC
3.	NC	12.	Stage 2 Output	22.	-12 VDC
4.	NC	13.	NC	23.	NC
5.	NC	14.	Output	24.	+12 VDC
6.	GND	15.	Stage 3 Input	25.	NC
7.	NC	16.	NC	26.	Stage 1 Output
8.	NC	17.	NC	27.	NC
9.	NC	18.	NC	28.	NC
		19.	NC		

NOTE: For proper operation connect Pin 26 to Pin 10, Pin 12 to Pin 15.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

V_{CC} = ±12 Volts
T_A = 25°C
R_S = 50
R_L = 10K

Characteristic	Min	Typ	Max	Units	Conditions
Voltage Gain	-1.5	0	1.5	dB	Ideal Center Frequency (F_O), 2800Hz
Frequency Response					Referenced from F_O Gain
	-70	—	—	dB	DC to 1800Hz
	-50	—	—	dB	2300Hz
	-30	—	—	dB	2600Hz
	-3	—	—	dB	2740Hz
	—	—	-3	dB	2760Hz
	—	—	-3	dB	2840Hz
	-3	—	—	dB	2860Hz
	-30	—	—	dB	3000Hz
	-50	—	—	dB	3300Hz
	-70	—	—	dB	3800Hz to 50kHz
Ripple	—	—	+0.5	dB	2741Hz to 2859Hz (Reference Fig. 1)
Input Impedance	25	—	—	kΩ	
Output Offset Voltage	—	—	20	mV	
Output Impedance	—	—	25	Ω	
Harmonic Distortion	—	—	1.0	%	V_{OUT} = 10V_{PP}, Freq. = 2800Hz
Current Drain	—	—	15	mA	

TELECOM

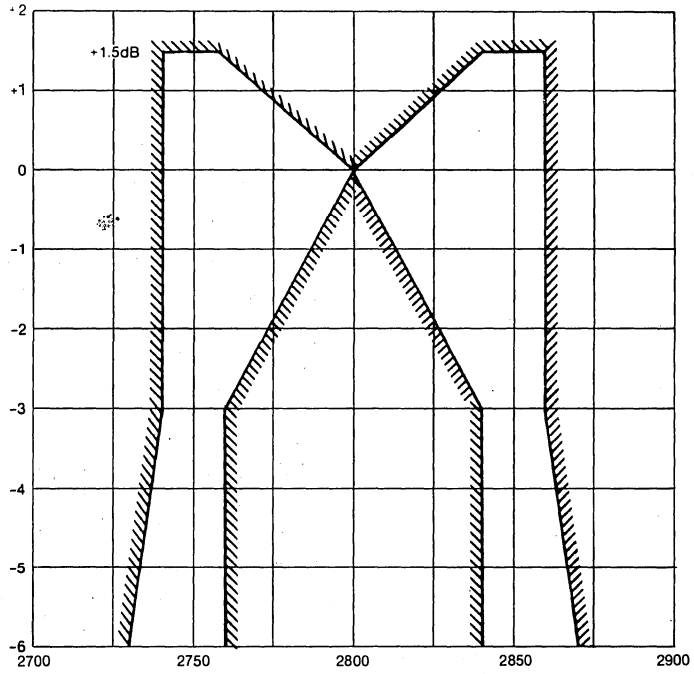


Fig. 1 ACF 7328C PASS BAND ATTENUATION LIMITS EXPANDED

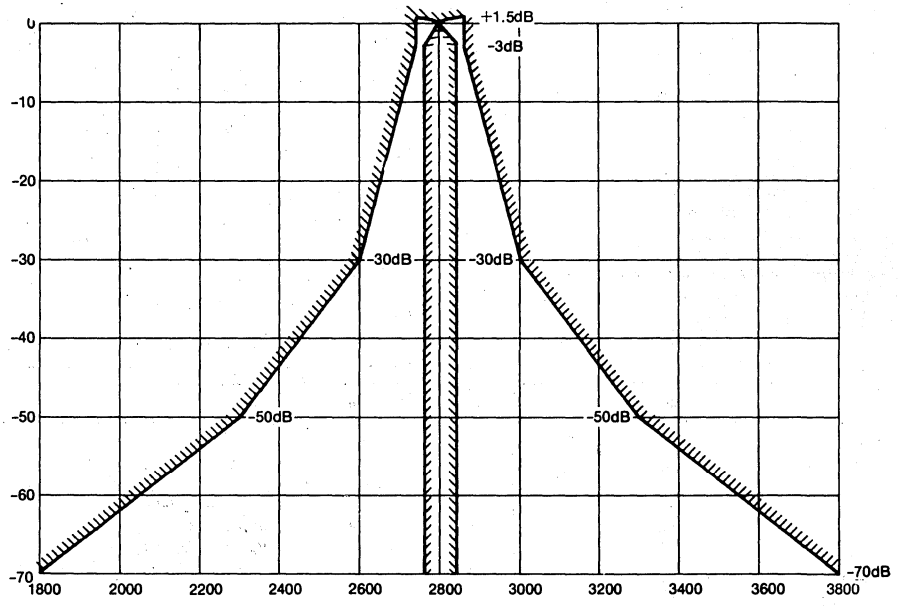


Fig. 2 ACF 7328C PASS BAND ATTENUATION LIMITS

2600Hz Band Suppression Filter

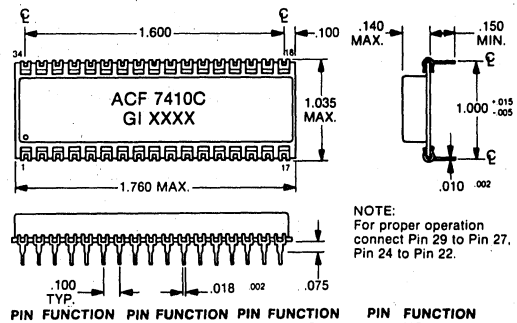
FEATURES

- 60dB attenuation from 2585Hz to 2615Hz
- Narrow Band Rejection
- Low Ripple
- Can be operated with single-ended power system

DESCRIPTION

The ACF 7410C is a linear hybrid band suppression RC Active Filter. The ACF 7410C is a sharply tuned filter designed to reject the 2600Hz signaling frequency. This filter provides for a 9dB attenuation to match the characteristics of a passive filter system. In addition, the filter provides a minimum attenuation of 60 dB, plus and minus 15Hz from the ideal center frequency of 2600Hz. This filter is packaged in a dual in line configuration.

PACKAGE INFORMATION
PIN CONFIGURATION



NOTE:
For proper operation connect Pin 29 to Pin 27, Pin 24 to Pin 22.

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1.	T.P.	9.	+12VCD	18.	-12VDC	26.	NC
2.	NC	10.	NC	19.	Output	27.	Stage 2 Input
3.	NC	11.	NC	20.	T.P.	28.	NC
4.	NC	12.	T.P.	21.	NC	29.	Stage 1 Output
5.	NC	13.	NC	22.	Stage 3 Input	30.	NC
6.	NC	14.	NC	23.	NC	31.	T.P.
7.	T.P.	15.	NC	24.	Stage 2 Output	32.	Input
8.	NC	16.	NC	25.	T.P.	33.	NC
		17.	GND			34.	NC

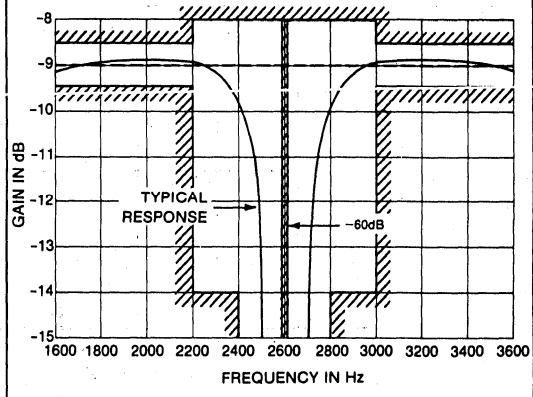


Fig. 1 FREQUENCY RESPONSE LIMITS ACF 7410C

ELECTRICAL CHARACTERISTICS

Maximum Ratings *

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±8 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)
at V_{CC} = ±12 Volts
T_A = 25°C
R_S = 50 Ω
R_L = 10K

Characteristic	Min	Typ	Max	Units	Conditions
Voltage Gain	-9.5	-9.0	-8.5	dB	1000Hz
Frequency Response					Referenced from the 1000Hz Gain as 0dB
	-0.5	0	+0.5	dB	250Hz to 2200Hz
	+1.0	—	-5.0	dB	2200Hz to 2400Hz
	-60	—	—	dB	2585Hz to 2615Hz
	+1.0	—	-5.0	dB	2800Hz to 3000Hz
	-0.5	0	+0.5	dB	3000Hz to 3400Hz
Input Impedance	25	—	—	kΩ	
Output Offset Voltage	—	—	100	mV	
Output Impedance	—	—	25	Ω	
Harmonic Distortion	—	—	0.5	%	V_{OUT} = 4.0 V_{PP}, Freq. = 1.0kHz
Current Drain	—	12	22.5	mA	

2600Hz Band Suppression Filter

FEATURES

- 30dB attenuation from 2585Hz to 2615Hz
- Low Power Dissipation
- Narrow Band Rejection
- Low Ripple
- Can be operated with single-ended power system

DESCRIPTION

The ACF 7412C is a linear hybrid band suppression RC Active Filter. The ACF 7412C is a sharply tuned filter designed to reject the 2600Hz signaling frequency. This filter provides for a 0dB attenuation to match the characteristics of a passive filter system. In addition, the filter provides a minimum attenuation of 30dB, plus and minus 15Hz from the ideal center frequency of 2300Hz. This filter is packaged in a dual in line configuration.

ELECTRICAL CHARACTERISTICS

Maximum Ratings *

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±8 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... −65° C to +150° C
Operating Temperature Range ..... 0° C to +70° C

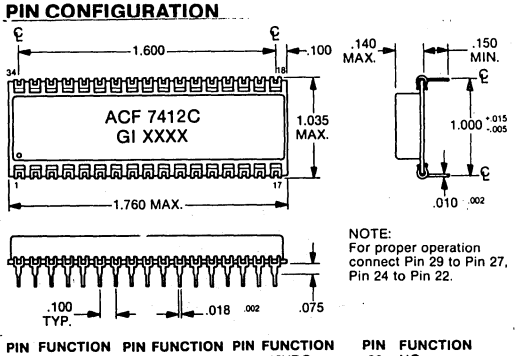
*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

at V_{CC} = ±12 Volts,
T_A = 25° C,
R_S = 50Ω,
R_L = 10K

PACKAGE INFORMATION

PIN CONFIGURATION



NOTE:
For proper operation connect Pin 29 to Pin 27, Pin 24 to Pin 22.

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1.	T.P.	9.	+12VCD	18.	-12VDC	26.	NC
2.	NC	10.	NC	19.	Output	27.	Stage 2 Input
3.	NC	11.	NC	20.	T.P.	28.	NC
4.	NC	12.	T.P.	21.	NC	29.	Stage 1 Output
5.	NC	13.	NC	22.	Stage 3 Input	30.	NC
6.	NC	14.	NC	23.	NC	31.	T.P.
7.	T.P.	15.	NC	24.	Stage 2 Output	32.	Input
8.	NC	16.	NC	25.	T.P.	33.	NC
		17.	GND			34.	NC

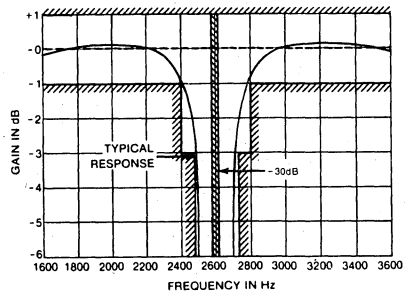


Fig. 1 FREQUENCY RESPONSE LIMITS ACF 7410C

Characteristic	Min	Typ	Max	Units	Conditions
Voltage Gain	−0.75	0	+0.75	dB	1000Hz
Frequency Response					Referenced from the 1000Hz Gain as 0dB
	−0.2	0	+0.3	dB	300Hz to 2300Hz
	−1.0	—	+1.0	dB	2300Hz to 2400Hz
	—	—	−30	dB	2585Hz to 2615Hz
	−3.0	—	+1.0	dB	2480Hz to 2720Hz
	−1.0	0	+1.0	dB	2800Hz to 3400Hz
Input Impedance	25	—	—	kΩ	
Output Offset Voltage	—	—	100	mV	
Output Impedance	—	—	25	Ω	
Harmonic Distortion	—	—	0.5	%	V_{OUT} = 4.0 V_{PP}, Freq. = 1.0kHz
Current Drain	—	—	22	mA	

2600Hz/2800Hz Band Suppression Filters

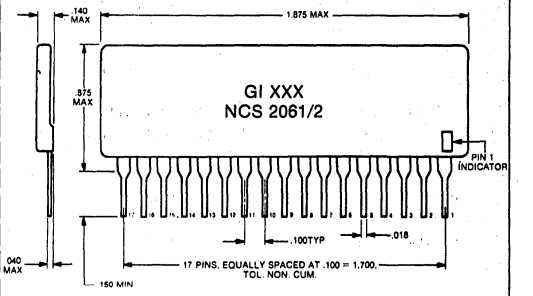
FEATURES

- 45dB attenuation from 2585Hz to 2615Hz and from 2785Hz to 2815Hz
- 0.875 inch high SIP configuration allows close board spacing.
- Low ripple

DESCRIPTION

The NCS 2061 and the NCS 2062 are linear hybrid band suppression RC Active Filters. They are a matched pair and combined to reject the 2600Hz and the 2800Hz signaling frequencies. These two filters are packaged in the dual in line configurations.

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1.	INPUT	7.	N.C.	13.	OUTPUT
2.	N.C.	8.	TP4	14.	TP7
3.	TP1	9.	N.C.	15.	−V
4.	N.C.	10.	TP5	16.	+V
5.	TP2	11.	TP6	17.	GND
6.	TP3	12.	N.C.		

ELECTRICAL CHARACTERISTICS

Maximum Ratings *

V_{CC} (Max) ..... ±18 Volts
Input Voltage Range ..... V_{CC}
Storage Temperature Range ..... −65° C to +150° C
Operating Temperature Range ..... 0° C to +70° C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

at $V_{CC} = \pm 12$ Volts,
$T_A = 25°$ C,
$R_S = 600\Omega$,
$R_L = 150K\Omega$

Characteristic	Min	Typ	Max	Units	Conditions
Voltage Gain	−.5	0	+.5	dB	1000Hz
Frequency Response*					Referenced from the 1000Hz Gain as 0dB
	−.5	0	+.5	dB	300Hz to 2000Hz
	−1.0	—	+.5	dB	2000Hz to 2200Hz
	−5.0	—	—	dB	2200Hz to 2400Hz
	—	—	−45	dB	2585Hz to 2615Hz
	—	—	−45	dB	2785Hz to 2815Hz
	−5.0	—	—	dB	3000Hz to 3200Hz
	−1.0	—	+.5	dB	3200Hz to 3400Hz
Input Impedance	10	—	—	KΩ	
Output Offset Voltage	—	—	±100	mV	
Output Impedance	—	—	5	KΩ	
Harmonic Distortion	—	—	0.5	%	$V_{OUT} = 4.0\ V_{PP}$, Freq. = 1.0kHz
Current Drain	—	—	30	mA	Both filters

*NOTE: Frequency response is for the 2061/62 pair.

DTMF Band Separation Filter

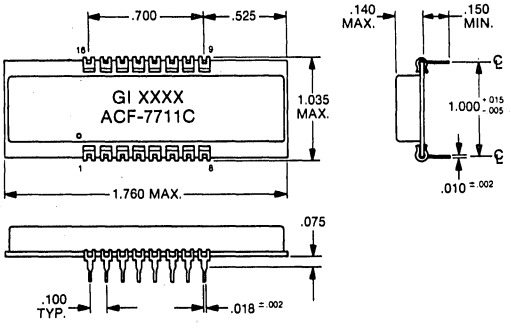
FEATURES

- Dual Filter in one package
- 24dB minimum out of band attenuation
- Low in band ripple
- 0dB insertion loss
- 30dB minimum out of band attenuation at 941Hz and 1209Hz respectively
- Low power dissipation
- Can be operated from a single-ended power system

DESCRIPTION

The ACF 7711C is a dual RC active filter which has been designed to provide channel isolation between the low frequency group of the Tone (DTMF) frequencies of 697Hz through 941Hz, and the high frequency group of the Tone (DTMF) frequencies of 1209Hz through 1633Hz. This dual filter is packaged in a dual in line package.

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	Low Group Output	9	Interstage Input #4
2	Plus V_{CC}	10	Test Point #3
3	Test Point #2	11	High Group Output
4	Low Group Input	12	High Group Input
5	Interstage Output #3	13	Test Point #1
6	GND #1	14	Minus V_{CC}
7	GND #2	15	Interstage Output #2
8	Test Point #4	16	Interstage Input #1

NOTE: An external connection is required between Pins; 3&13, 5&9, 6&7, 8&10, 15&16.

ELECTRICAL CHARACTERISTICS

Maximum Ratings *

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage (at V_{CC} max) ..... ±15 Volts
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

Standard Conditions (unless otherwise stated)

V_{CC} = ± 12V (Note 1)
R_L = 5kΩ
R_S = 50 Ω
0°C to 70°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Characteristic	Min	Typ	Max.	Units	Conditions
Low Group Filter Section					
Input Impedance	30	—	—	kΩ	
Input Voltage Range	—	—	±12	Volts	
Gain	—	0	±0.25	dB	941Hz
Frequency Response					Reference to 941Hz Gain
650Hz to 941Hz	-.75	0	+.75	dB	
1209Hz	-30	—	—	dB	
1209Hz to 1700Hz	-24	—	—	dB	
Output Voltage Range	±3.2	—	—	Volts	No Clipping
Output Impedance	—	—	10	Ω	
High Group Filter Section					
Input Impedance	60	—	—	kΩ	
Input Voltage Range	—	—	±12	Volts	
Gain	—	0	±0.25	dB	1209Hz
Frequency Response					Reference to 1209Hz Gain
1209Hz to 1700Hz	-.75	0	+1.5	dB	
941Hz	-30	—	—	dB	
941Hz to 650Hz	-24	—	—	dB	
Output Voltage Range	±3.2	—	—	Volts	No Clipping
Output Impedance	—	—	10	Ω	
Power Supply Current	—	4.0	5.0	mA	

NOTE:
1. Or equivalent single-ended power supplies.

TELECOM

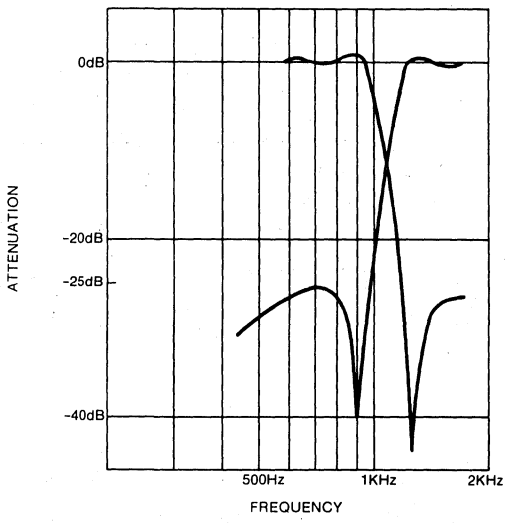


Fig.1 TYPICAL FREQ RESPONSE

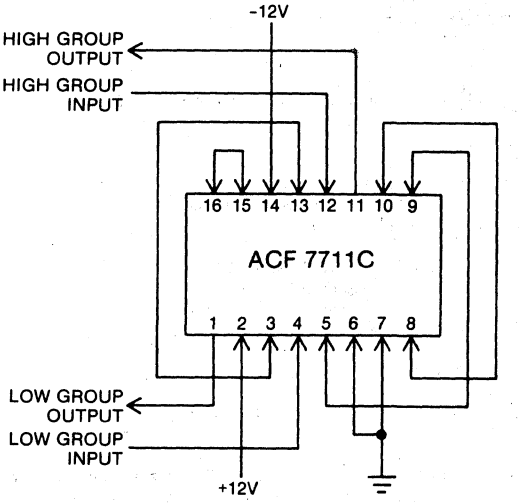


Fig.2 TONE SEPARATION FILTER TERMINATION

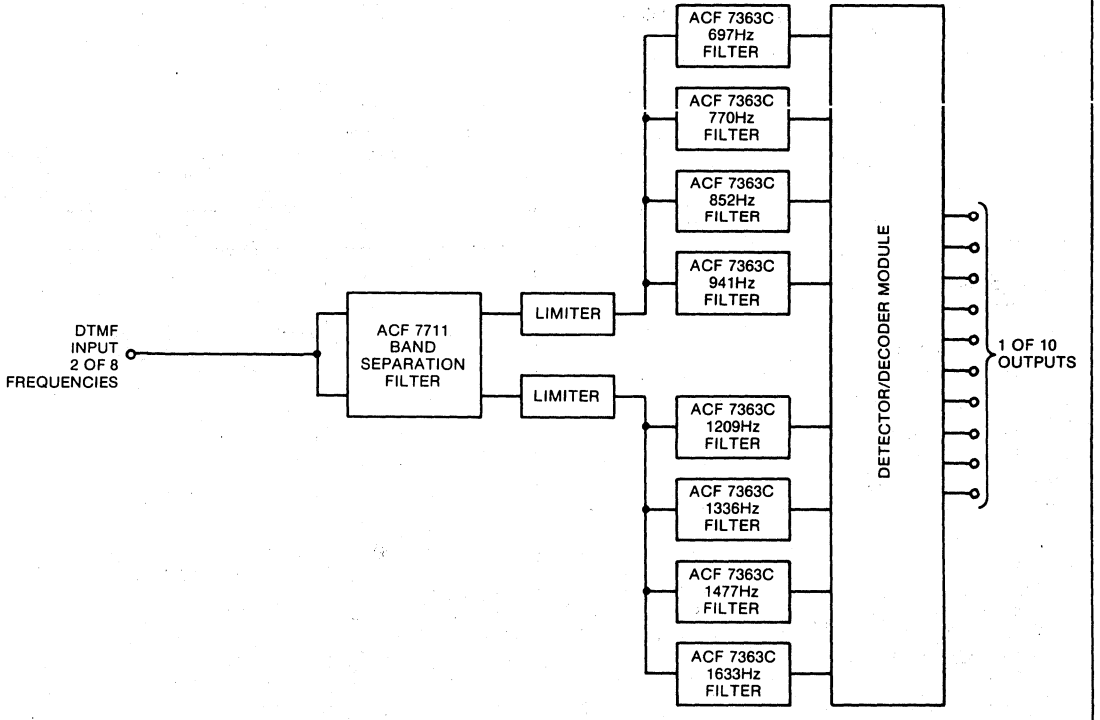


Fig.3 TYPICAL DTMF RECEIVER APPLICATION

DTMF Low Group Band Splitting Filter

FEATURES

- 0.73 inch high SIP configuration allows close board spacing
- Pass band ripple: ±1dB, from 686Hz to 955Hz
- Stop band attenuation: 30dB min, from 1190Hz to 1660Hz

DESCRIPTION

The ACF 7720C is a linear hybrid low pass active filter. The hybrid will pass a signal in the pass band with ±1dB ripple from 686Hz to 955Hz and be 30dB down from 1190Hz to 1660Hz. The filter is designed to be used in DTMF band splitting applications with the tone frequencies of 686Hz through 955Hz.

ELECTRICAL CHARACTERISTICS

Maximum Ratings *

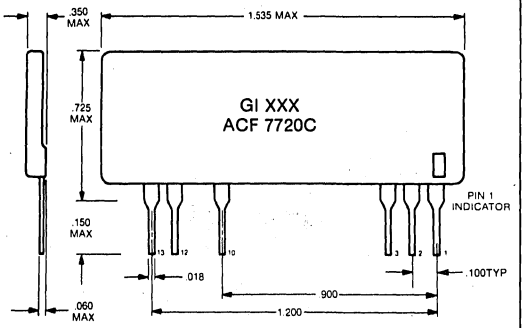
V_{CC}, V_{EE} ..... ±18VDC
Input Voltage .....Power Supply Potential
Storage Temperature .....−65° C to +150° C
Operating Temperature .....0° C to +70° C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

$V_{CC} = +12$ Volts
$V_{EE} = -12$ Volts
$T_A = 25° C$

PACKAGE INFORMATION
PIN CONFIGURATION



PIN FUNCTION		PIN FUNCTION	
1.	INPUT	8.	N.C.
2.	GND	9.	N.C.
3.	V_{CC}	10.	V_{EE}
4.	N.C.	11.	N.C.
5.	N.C.	12.	T.P.
6.	N.C.	13.	OUTPUT
7.	N.C.		

Characteristic	Min	Typ	Max	Units	Conditions
Passband Response	0	+1.5	+3.0	dB	f = 686Hz −955Hz
Passband Ripple	−1	0	+1	dB	f = 686Hz −955Hz
Stop Band Attenuation	30	—	—	dB	f = 1190Hz to 1660Hz
Output Noise	—	—	−50	dBm	input grounded
Distortion	—	—	1	%	
Input Impedance	10K	—	—	Ω	
Output Impedance	—	—	200	Ω	
Supply Current	—	—	15	mA	

PRELIMINARY INFORMATION

DTMF High Group Band Splitting Filter

FEATURES

- 0.73 inch high SIP configuration allows close board spacing
- Pass band ripple: ±1dB, from 1190Hz to 1660Hz
- Stop band attenuation: 30dB min, from 686Hz to 955Hz

DESCRIPTION

The ACF 7721C is a linear hybrid high pass active filter. The hybrid will pass a signal in the pass band with ±1dB ripple from 1190Hz to 1660Hz and be 30dB down from 686Hz to 955Hz. The filter is designed to be used in DTMF band splitting applications with the tone frequencies of 1190Hz through 1660Hz.

ELECTRICAL CHARACTERISTICS

Maximum Ratings *

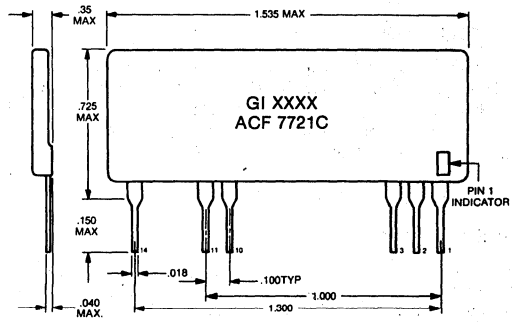
V_{CC} V_{EE} ..... ±18VDC
Input Voltage .....Power Supply Potential
Storage Temperature ..... −65° C to +150° C
Operating Temperature .....0° C to +70° C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

V_{CC} = +12 Volts
V_{EE} = −12 Volts
T_A = 25° C

PACKAGE INFORMATION
PIN CONFIGURATION



PIN FUNCTION		PIN FUNCTION	
1.	INPUT	8.	N.C.
2.	GND	9.	N.C.
3.	V_{CC}	10.	V_{EE}
4.	N.C.	11.	T.P.
5.	N.C.	12.	N.C.
6.	N.C.	13.	N.C.
7.	N.C.	14.	OUTPUT

Characteristic	Min	Typ	Max	Units	Conditions
Passband Response	0	+1.5	+3.0	dB	f = 1190Hz −1660Hz
Passband Ripple	−1	0	+1	dB	f = 1190Hz −1660Hz
Stop Band Attenuation	30	—	—	dB	f = 686Hz to 955Hz
Output Noise	—	—	−50	dBm	input grounded
Distortion	—	—	1	%	
Input Impedance	10K	—	—	Ω	
Output Impedance	—	—	200	Ω	
Supply Current	—	—	15	mA	

Data Communications

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
UAR/T	Complete 5-8 bit receiver/transmitter interface.	AY-5-1013A	6-80
		AY-6-1013	6-80
		AY-3-1014A	6-80
		AY-3-1015D	6-80
16 CHANNEL MULTIPLEXER	Multiplexes 16 analog channels with on-chip logic control.	AY-5-1016	6-93
		AY-6-4016	6-93

UAR/T: Universal Asynchronous Receiver/Transmitter

FEATURES

- DTL and TTL compatible—no interfacing circuits required—drives one TTL load
- Fully Double Buffered—eliminates need for system synchronization, facilitates high-speed operation
- Full Duplex Operation—can handle multiple bauds (receiving-transmitting) simultaneously
- Start Bit Verification—decreases error rate with center sampling
- Receiver center sampling of serial input; 46% distortion immunity
- High Speed Operation
- Three-State Outputs—bus structure capability
- Low Power—minimum power requirements
- Input Protected—eliminates handling problems

AY-5-1013A
- GIANT P-channel nitride process
- 0 to 40kbaud
- Pull up resistors to V_{CC} on all inputs

AY-6-1013
- GIANT P-channel nitride process
- 0 to 22.5kbaud
- Extended Operating Temperature Range:
  -40°C to +85°C (plastic package)
  -55°C to +125°C (ceramic package)
- Pull-up resistors to V_{CC} on all inputs

AY-3-1014A/1015D
- Single Supply Operation:
  +4.75V to +14V (AY-3-1014A)
  +4.75V to +5.25V (AY-3-1015D)
- CMOS compatible (AY-3-1014A)
- 1½ stop bit mode
- External reset of all registers except control bits register
- GIANT II N-channel Ion Implant Process
- 0 to 30k baud
- Pull-up resistors to V_{CC} on all inputs (AY-3-1015D)

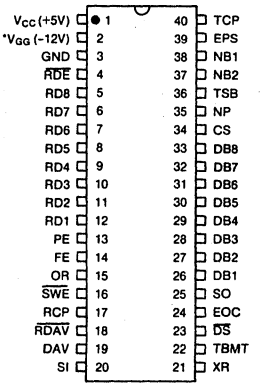
DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits (1½ stop bit capability with the AY-3-1014A/1015D), and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are three-state logic.

PIN CONFIGURATION

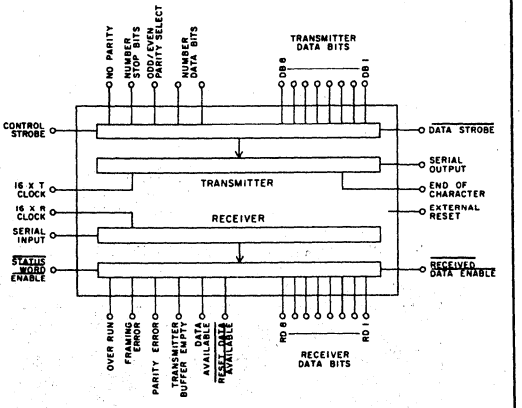
40 LEAD DUAL IN LINE

Top View



* Pin 2: AY-3-1014A/1015D — No Connection.

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	V_{CC} Power Supply (V_{CC})	+5V Supply
2	V_{GG} Power Supply (V_{GG})	−12V Supply (Not connected for AY-3- 1014A/1015)
3	Ground (V_{GI})	Ground
4	Received Data Enable (RDE)	A logic "0" on the receiver enable line places the received data onto the output lines.
5-12	Received Data Bits (RD8-RD1)	These are the 8 data output lines. Received characters are right justified: the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL ouput characteristics when RDE is "0" and a high impedance state when RDE is "1". Thus, the data output lines can be bus structure oriented.
13	Parity Error (PE)	This line goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state.
14	Framing Error (FE)	This line goes to a logic "1" if the received character has no valid stop bit. Tri-state.
15	Over-Run (OR)	This line goes to a logic "1" if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state.
16	Status Word Enable (SWE)	A logic "0" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tri-state.
17	Receiver Clock (RCP)	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud.
18	Reset Data Available (RDAV)	A logic "0" will reset the DAV line. The DAV F/F is only thing that is reset. Must be tied to logic '1' when not in use on the AY-3-1014A.
19	Data Available (DAV)	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state. Fig.12,34.
20	Serial Input (SI)	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception. Fig.11,12,33,34.
21	External Reset (XR)	Resets all registers except the control bits register (the received data register is not reset in the AY-5-1013A and AY-6-1013). Sets SO, EOC, and TBMT to a logic "1". Resets DAV, and error flags to "0". Clears input data buffer. Must be tied to logic "0" when not in use.
22	Transmitter Buffer Empty (TBMT)	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig.18,20,40,42.
23	Data Strobe (DS)	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS. Data must be stable during entire strobe.
24	End of Character (EOC)	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig.17,19,39,41.
25	Serial Output (SO)	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted. See Fig.16.
26-33	Data Bit Inputs (DB1-DB8)	There are up to 8 data bit input lines available.
34	Control Strobe (CS)	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level.
35	No Parity (NP)	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0".
36	Number of Stop Bits (TSB)	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits. For the AY-3-1014A/1015, the combined selection of 2 stop bits and 5 bits/character will produce 1½ stop bits.
37-38	Number of Bits/Character (NB2, NB1)	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character. NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select (EPS)	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock (TCP)	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud.

TRANSMITTER OPERATION

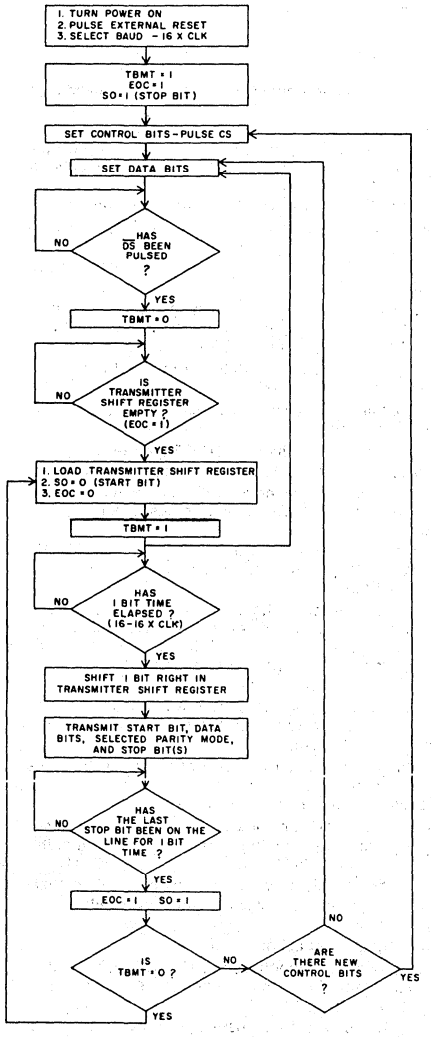


Fig.1

Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud. The above conditions will set TBMT, EOC, and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection normally occurring before data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once Data Strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will return to a logic "1". When transmitter shift register is empty, data bits in the holding register are immediately loaded into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit has been on line for one bit time, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously discussed.

RECEIVER OPERATION

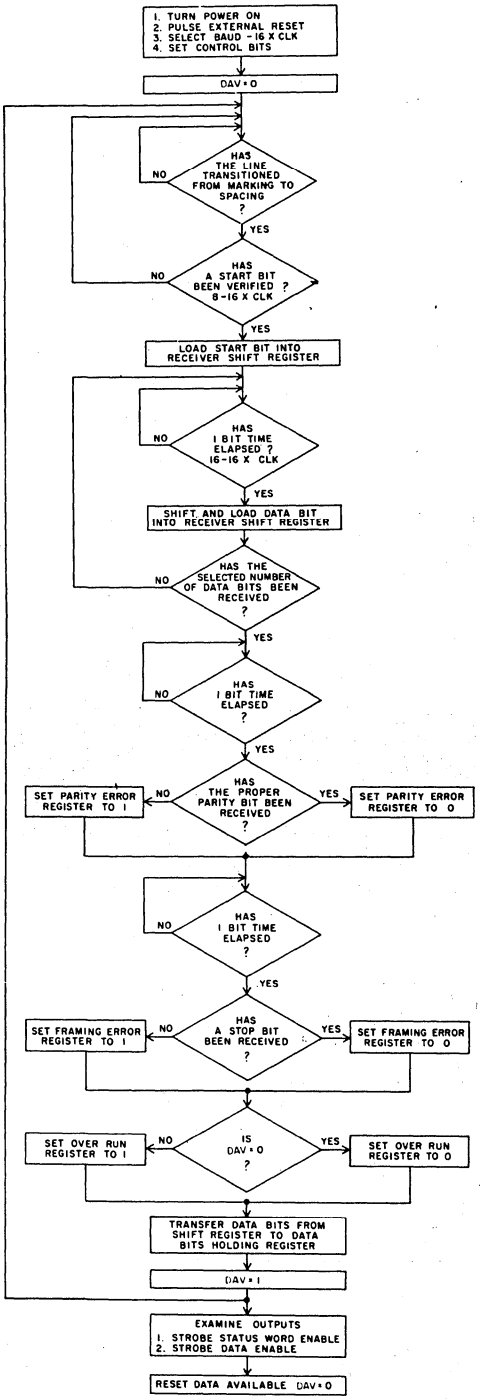


Fig.2

Initializing

Power is applied, external reset is enabled, and clock pulse is applied having a frequency of 16 times the desired baud. The previous conditions will set data available (DAV) to a logic "1".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs, the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time, for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditionally set to a logic "0".

Once a full character is received, internal logic looks at the data available (DAV) signal to determine if data has been the read out. If the DAV signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status word holding register will be set to a logic "1". If the DAV signal is at a logic "0" the receiver will assume that data has been read out. After DAV goes to a logic "1", the receiver shift register is now ready to accept the next character and has one full character time to remove the received character.

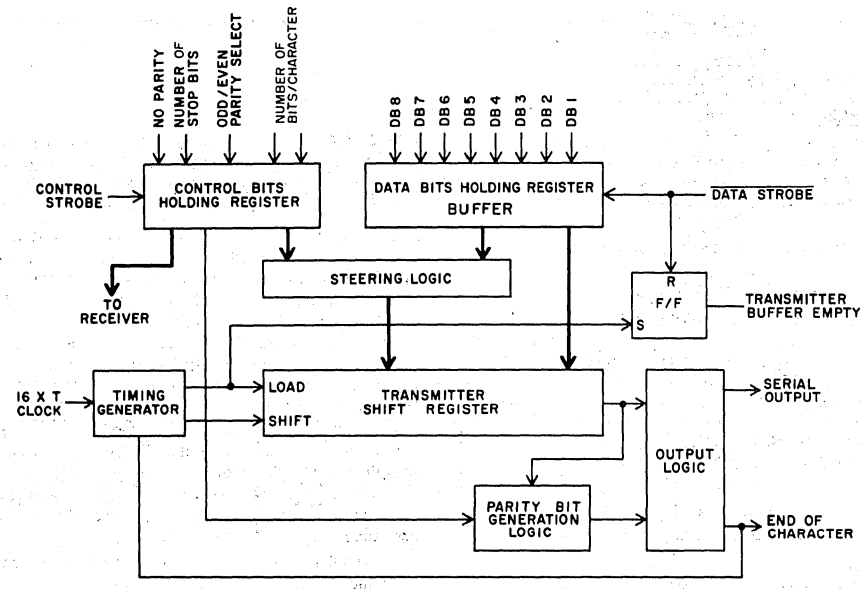


Fig.3 TRANSMITTER BLOCK DIAGRAM

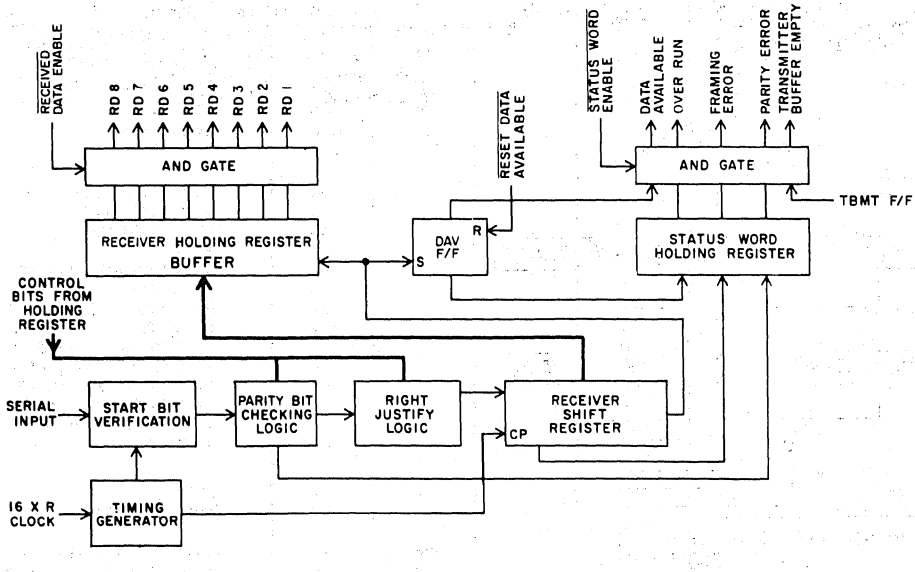


Fig.4 RECEIVER BLOCK DIAGRAM

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} (with respect to V_{CC}) . . . . . −20 to +0.3V
Clock and logic input voltages (with respect to V_{CC}) . . . . . −20 to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +330°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

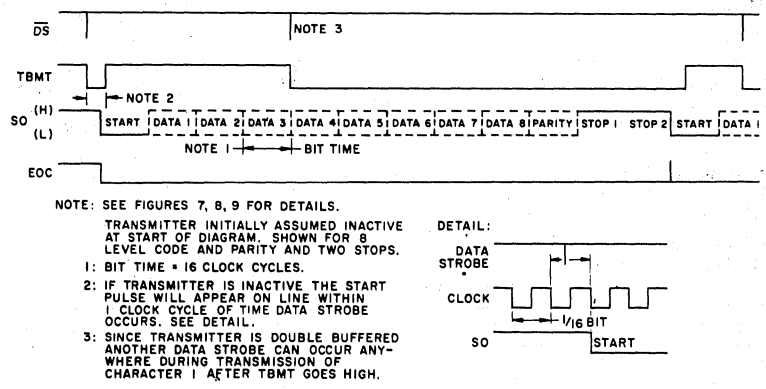
Standard Conditions (unless otherwise noted)

V_{GG} = −12V ±5%
V_{CC} = +5V ±5%
Temperature (T_A) = 0°C to +70°C (AY-5-1013A)
−40 C to +85°C (AY-6-1013 Plastic Package)
−55C to +125°C (AY-6-1013 Ceramic Package)

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Logic Levels					
Logic 0	0	—	0.8	Volts	(I_{IL} = −1.6mA max.)
Logic 1	V_{CC}-1.5	—	V_{CC}+0.3	Volts	Unit has internal pullup resistors
Input Capacitance					
All Inputs	—	—	20	pF	0 volts bias, f= 1MHz
Leakage Currents					
Three State Outputs	—	—	1.0	µA	0 volts
Data Output Levels					
Logic 0	—	—	+0.4	Volts	I_{OL}= 1.6mA (sink) } at 5.0 Volts
Logic 1	V_{CC}-1.0	—	—	Volts	I_{OH}= .3mA (source) } at 5.0 Volts
Output Capacitance	—	10	15	pF	
Short Ckt. Current	—	—	—	—	See Fig. 23
Power Supply Current					
I_{GG} } 25°C,all inputs +5V	—	14	16	mA	AY-5-1013A - See Fig.25
I_{GG} } 25°C,all inputs +5V	—	17	19	mA	AY-6-1013 - See Fig.25
I_{CC} } 25°C,all inputs +5V	—	18	20	mA	AY-5-1013A - See Fig.26
I_{CC} } 25°C,all inputs +5V	—	21	23	mA	AY-6-1013
AC CHARACTERISTICS					T_A = 25°C, output load capacitance 50pF max.
Clock Frequency	DC	—	640	kHz	AY-5-1013A
	DC	—	360	kHz	AY-6-1013
Baud	0	—	40	kbaud	AY-5-1013A
	0	—	22.5	kbaud	AY-6-1013
Pulse Width					
Clock Pulse	750	—	—	ns	AY-5-1013A - See Fig.9
	1.5	—	—	µs	AY-6-1013-See Fig.9
Control Strobe	300	—	—	ns	AY-5-1013A-See Fig. 15, 16
	600	—	—	ns	AY-6-1013
Data Strobe	190	—	—	ns	AY-5-1013A-See Fig. 14
	250	—	—	ns	AY-6-1013
External Reset	500	—	—	ns	AY-5-1013A - See Fig. 13
	1.0	—	—	µs	AY-6-1016
Status Word Enable	500	—	—	ns	AY-5-1013A - See Fig. 21
	600	—	—	ns	AY-6-1013 - See Fig. 21
Reset Data Available	250	—	—	ns	AY-5-1013A - See Fig. 22
	350	—	—	ns	AY-6-1013 - See Fig. 22
Received Data Enable	500	—	—	ns	AY-5-1013A - See Fig. 21
	600	—	—	ns	AY-6-1013 - See Fig. 21
Set Up & Hold Time					
Input Data Bits	0	—	—	ns	See Fig.14
Input Control Bits	0	—	—	ns	See Fig. 15, 16
Output Propagation Delay					
TPD0	—	—	500	ns	AY-5-1013A - See Fig. 21 & 24
	—	—	650	ns	AY-6-1013 - See Fig. 21 & 24
TPD1	—	—	500	ns	AY-5-1013A - See Fig. 21 & 24
	—	—	650	ns	AY-6-1013 - See Fig. 21 & 24

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



NOTE: SEE FIGURES 7, 8, 9 FOR DETAILS.

TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE WITHIN 1 CLOCK CYCLE OF TIME DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1 AFTER TBMT GOES HIGH.

Fig.5 UAR/T TRANSMITTER TIMING

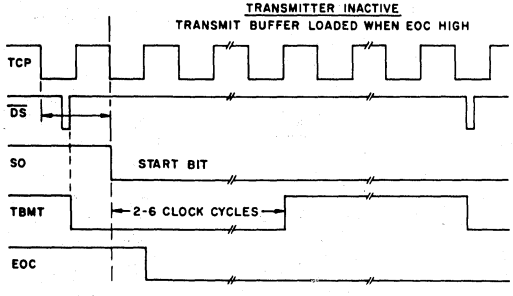


Fig.6 TRANSMITTER AT START BIT

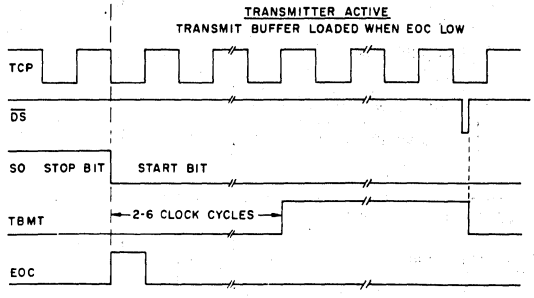
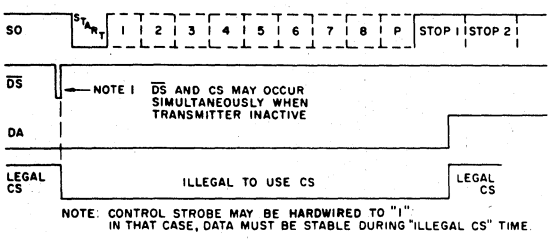
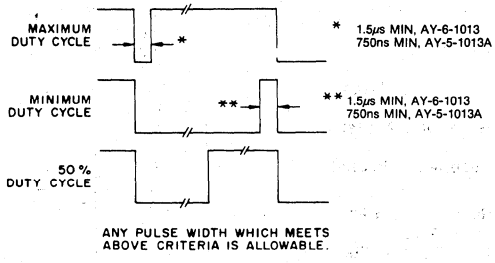


Fig.7 TRANSMITTER AT START BIT



NOTE: CONTROL STROBE MAY BE HARDWIRED TO "1". IN THAT CASE, DATA MUST BE STABLE DURING "ILLEGAL CS" TIME.

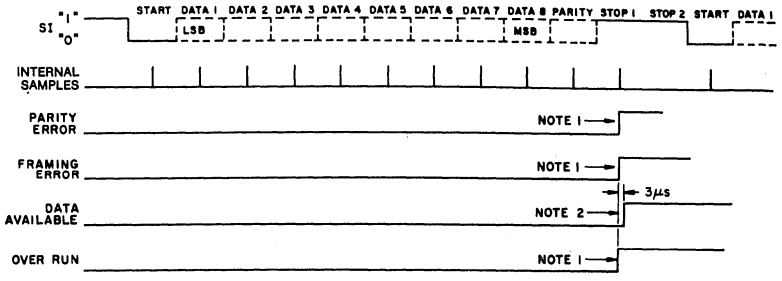
Fig.8 ALLOWABLE POINTS TO USE CONTROL STROBE



ANY PULSE WIDTH WHICH MEETS ABOVE CRITERIA IS ALLOWABLE.

Fig.9 ALLOWABLE TCP, RCP

TIMING DIAGRAMS



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE INDICATED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED*; THAT IS, LSB ALWAYS APPEARS IN RDI (PIN 12).

Fig.10 UAR/T RECEIVER TIMING

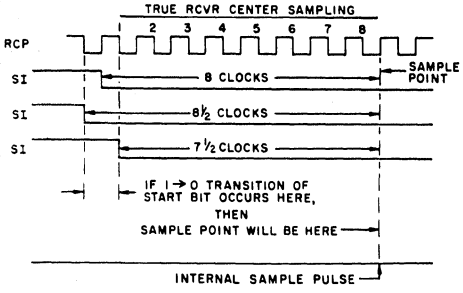


Fig.11

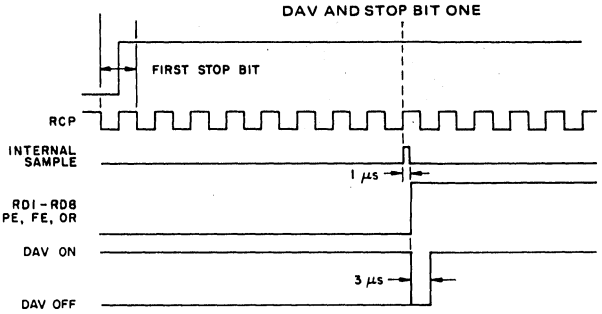
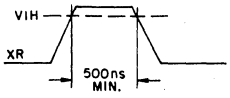


Fig.12 RECEIVER DURING 1st STOP BIT



WHEN NOT IN USE, XR MUST BE HELD AT GND.

XR RESETS EVERY REGISTER EXCEPT CONTROL REGISTER AND RECEIVED DATA. SO, T8MT, EOC ARE RESET TO 5V ALL OTHER OUTPUTS RESET TO 0V.

Fig.13 XR PULSE

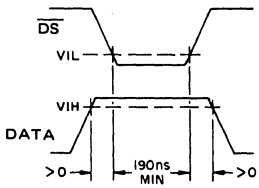
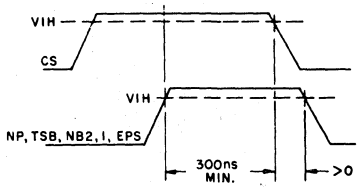
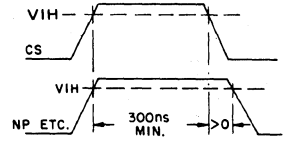


Fig.14 DS



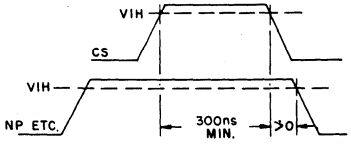
CONTROL BITS MUST BE STABLE FOR LAST 300ns OF CS.

Fig.15a CS



CONTROL STROBE AND CONTROL BITS MUST BE 300ns MINIMUM.

Fig.15b CS



LEADING EDGE OF DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED.

Fig.16 CS

TELECOM

TIMING DIAGRAMS

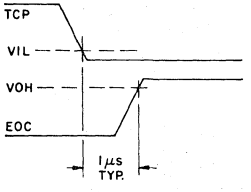


Fig.17 EOC TURN-ON

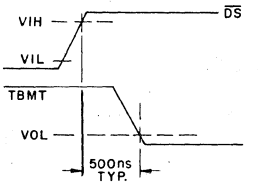


Fig.18 TBMT TURN-OFF

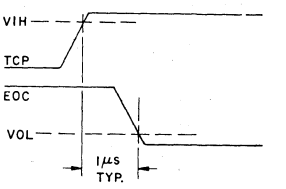


Fig.19 EOC TURN-OFF

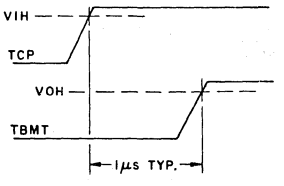


Fig.20 TBMT TURN-ON

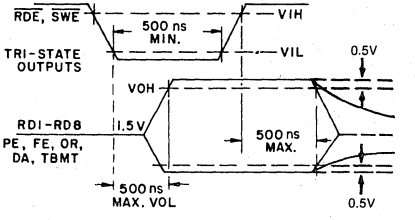


Fig.21 RDE, SWE

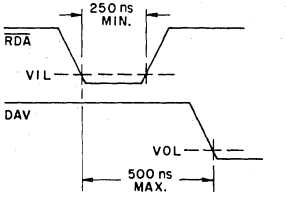


Fig.22 RDAV

TYPICAL CHARACTERISTIC CURVES

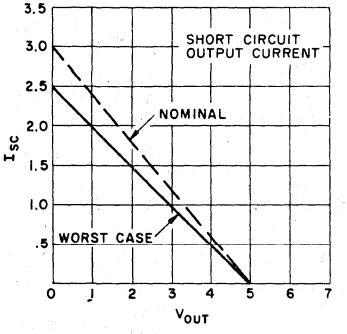


Fig.23 SHORT CIRCUIT OUTPUT CURRENT

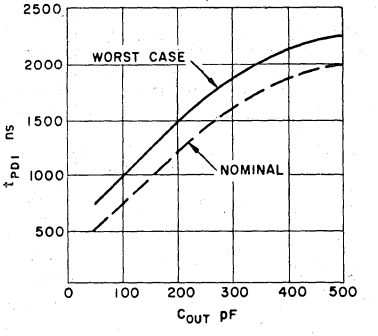


Fig.24 RE1, RD8, PE, FE, OR, TBMT, DAV

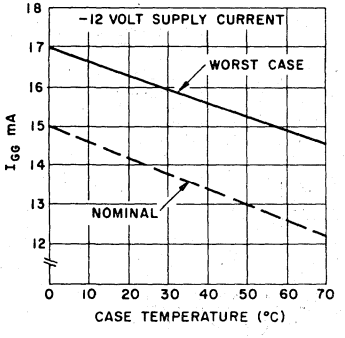


Fig.25 -12 VOLT SUPPLY CURRENT

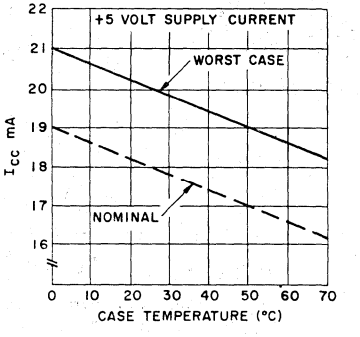


Fig.26 +5 VOLT SUPPLY CURRENT

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} (with respect to GND) . . . . . −0.3 to +16V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature. . . . . 0°C to +70°C
Lead Temperature (Soldering, 10 sec) . . . . . +330°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

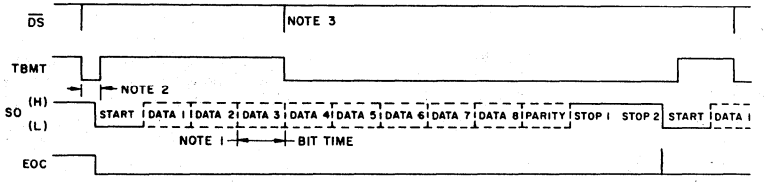
Standard Conditions (unless otherwise noted)

V_{CC} = +4.75 to +14V (AY-3-1014A)
V_{CC} = +4.75V to +5.25V (AY-3-1015D)
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Logic Levels (AY-3-1014A)					
Logic 0	0	—	0.8	Volts	
Logic 1: at V_{CC} = +4.75V	2.0	—	V_{CC} +0.3	Volts	
at V_{CC} = +14V	3.0	—	V_{CC} +0.3	Volts	
Input Logic Levels (AY-3-1015)					
Logic 0	0	—	0.8	Volts	
Logic 1	2.4	—	V_{CC}+0.3	Volts	AY-3-1015 has internal pull-up resistors to V_{CC}.
Input Capacitance					
All inputs	—	—	20	pF	0 volts bias, f = 1MHz
Output Impedance					
Tri-State Outputs	1.0	—	—	MΩ	
Data Output Levels					
Logic 0	—	—	+0.4	Volts	I_{OL} = 1.6mA (sink)
Logic 1: AY-3-1014A/1015D	2.4	—	—	Volts	I_{OH} = -40μA (source)—at V_{CC} = +5V
AY-3-1014A only	3.5	—	—	Volts	I_{OH} = -50μA (source)—at V_{CC} = +14V
Output Capacitance	—	10	15	pF	
Short Ckt. Current	—	—	—	—	See Fig.45.
Power Supply Current					
I_{CC} at V_{CC} = +5V (AY-3-1014A)	—	10	15	mA	See Fig.47.
I_{CC} at V_{CC} = +14V (AY-3-1014A)	—	14	20	mA	See Fig.48.
I_{CC} at V_{CC} = +5V (AY-3-1015D)	—	10	15	mA	
AC CHARACTERISTICS					T_A = 25°C, Output load capacitance 50 pF max.
Clock Frequency	DC	—	480/400	kHz	at V_{CC} = +4.75V/+14V
Baud	0	—	30/25	kbaud	at V_{CC} = +4.75V/+14V
Pulse Width					
Clock Pulse	1.0	—	—	μs	See Fig.31
Control Strobe	500		—	ns	See Fig.37
Data Strobe	200	—	—	ns	See Fig.36
External Reset	500	—	—	ns	See Fig.35
Status Word Enable	500		—	ns	See Fig.43
Reset Data Available	200	—	—	ns	See Fig.44
Received Data Enable	500	—	—	ns	See Fig.43
Set Up & Hold Time					
Input Data Bits	20	—	—	ns	See Fig.36
Input Control Bits	20	—	—	ns	See Fig.37
Output Propagation Delay					
TPD0	—	—	500	ns	See Fig.43 & 46
TPD1	—	—	500	ns	See Fig.43 & 46

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



NOTE: SEE FIGURES 28, 29, 30 FOR DETAILS.

TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS.

1: BIT TIME = 16 CLOCK CYCLES.

2: IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE 1 TO 2 CLOCK CYCLES AFTER THE DATA STROBE OCCURS. SEE DETAIL.

3: SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1 AFTER TBMT GOES HIGH.

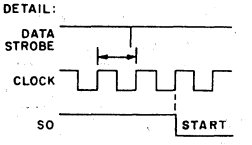


Fig.27 UAR/T — TRANSMITTER TIMING

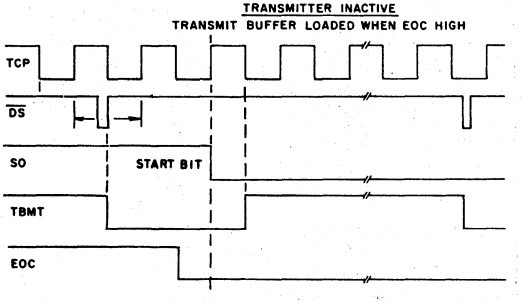


Fig. 28 TRANSMITTER AT START BIT NOT A TEST POINT

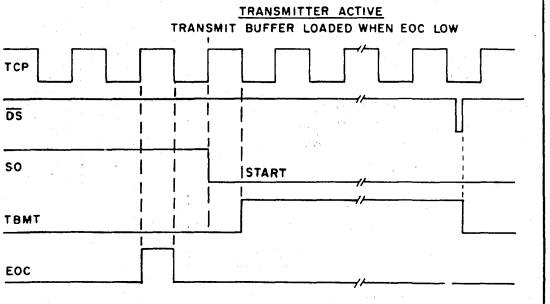
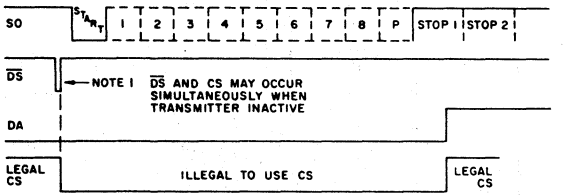
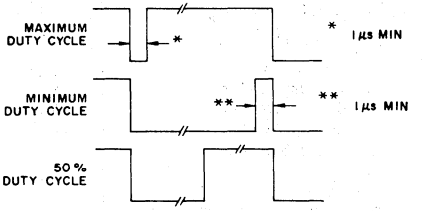


Fig.29 TRANSMITTER AT START BIT



NOTE: CONTROL STROBE MAY BE HARDWIRED TO "1" IN THAT CASE, CONTROL DATA BITS MUST BE STABLE DURING "ILLEGAL CS" TIME.

Fig.30 ALLOWABLE POINTS TO USE CONTROL STROBE

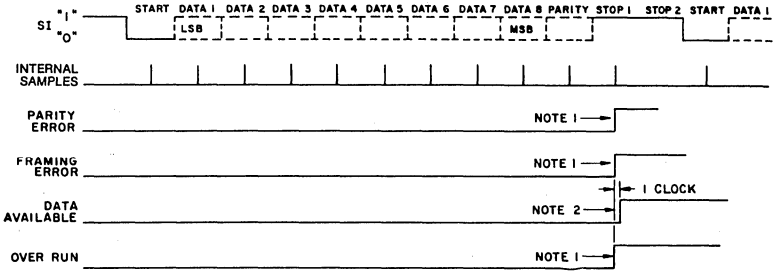


ANY PULSE WIDTH WHICH MEETS ABOVE CRITERIA IS ALLOWABLE.

Fig.31 ALLOWABLE TCP, RCP

TELECOM

TIMING DIAGRAMS



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE INDICATED, IF ERROR OCCURS.
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS. (SEE RECEIVER BLOCK DIAGRAM).
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER.
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA.
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED;* THAT IS, LSB ALWAYS APPEARS IN RD1 (PIN 12).

Fig.32 UAR/T — RECEIVER TIMING

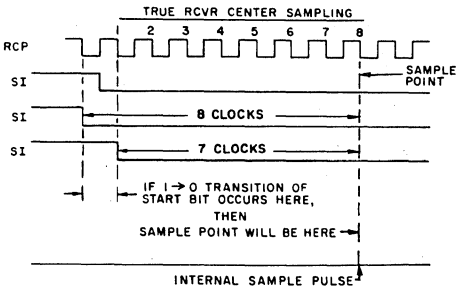


Fig.33

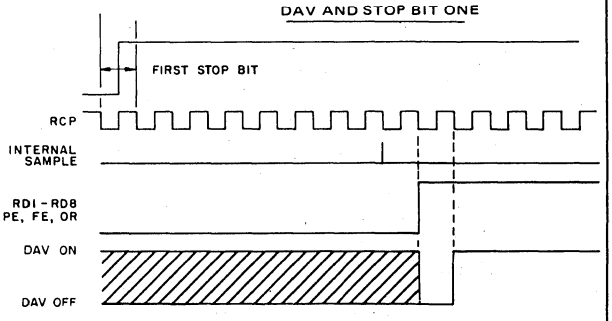
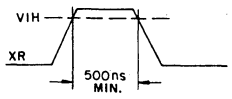


Fig.34 RECEIVER DURING 1ST STOP BIT



WHEN NOT IN USE, XR MUST BE HELD AT GND.

XR RESETS EVERY REGISTER EXCEPT THE CONTROL REGISTER. SO, TBMT, EOC ARE RESET TO 5V ALL OTHER OUTPUTS RESET TO OV.

Fig.35 XR PULSE

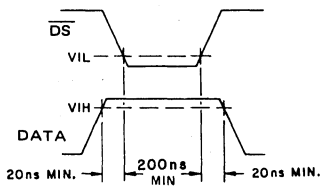
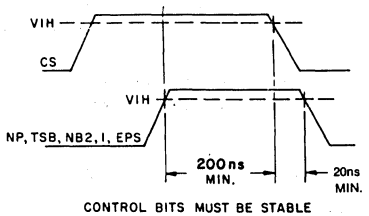
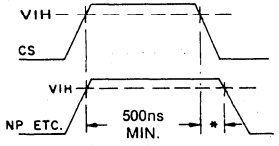


Fig.36 $\overline{DS}$



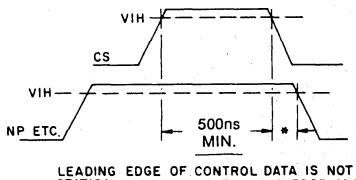
CONTROL BITS MUST BE STABLE FOR LAST 200ns OF CS.

Fig.37a CS



CONTROL STROBE AND CONTROL BITS MUST BE 500ns MINIMUM.

Fig.37b



LEADING EDGE OF CONTROL DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED.

* 20ns MIN.

Fig.38

TELECOM

TIMING DIAGRAMS

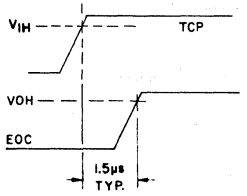


Fig.39 EOC TURN-ON

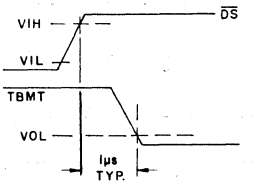


Fig.40 TBMT TURN-OFF

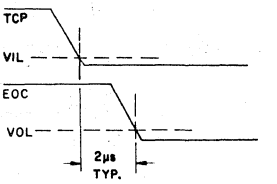


Fig.41 EOC TURN-OFF

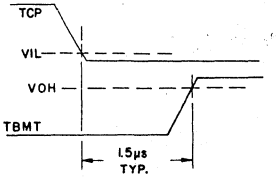


Fig.42 TBMT TURN-ON

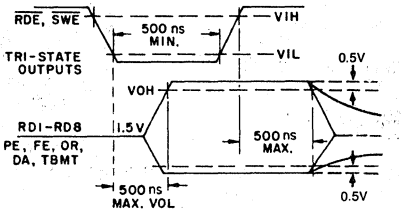


Fig.43 RDE, SWE

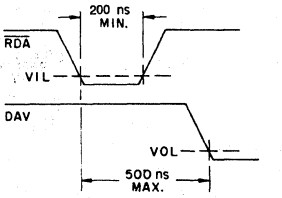


Fig.44 RDAV

TYPICAL CHARACTERISTIC CURVES

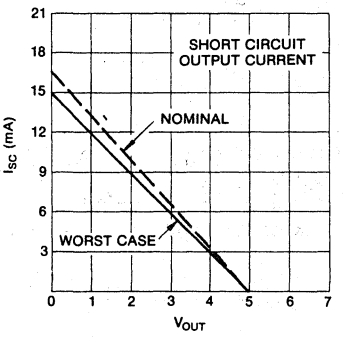


Fig.45 SHORT CIRCUIT OUTPUT CURRENT
(only 1 output may be shorted at a time)

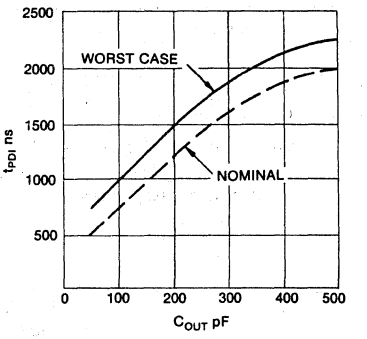


Fig.46 RD1-RD8, PE, FE, OR, TBMT, DAV

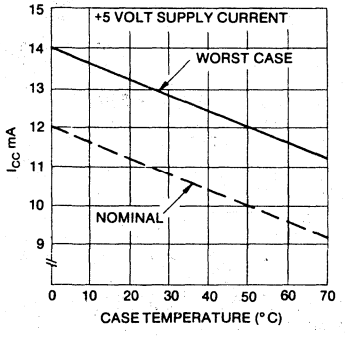


Fig.47 +5 VOLT SUPPLY CURRENT

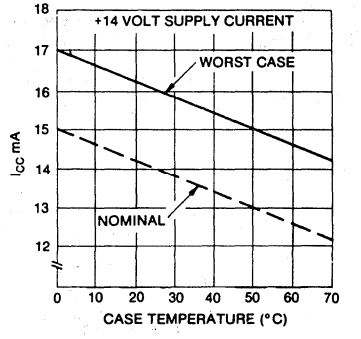


Fig.48 +14 VOLT SUPPLY CURRENT
(AY-3-1014A only)

Random/Sequential Access Multiplexers

FEATURES

- Directly interfaces with TTL/DTL and MOS
- Current or voltage modes of operation
- Random or sequential access
- Single ended or differential operation
- Expandable in either the sequential or random access modes
- Programmable length counter for sequential applications
- DC to 2MHz operation
- Extremely high off-resistance
- Choice of Operating Temperature Ranges:
  AY-5-1016 — 0°C to +70°C
  AY-6-4016 — −55°C to +125°C
- Zener network protection on all input leads

DESCRIPTION

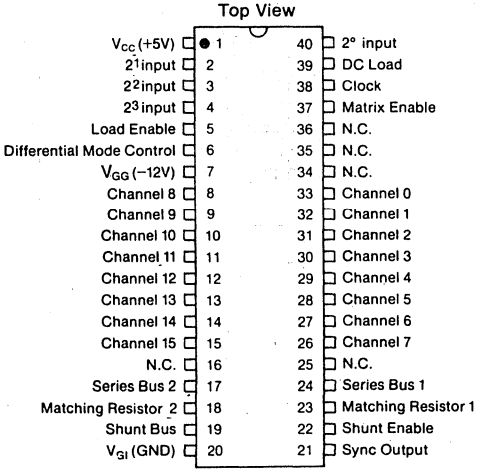
The AY-5-1016 and AY-6-4016 are each a 16 Channel Random/Sequential Access Multiplexer containing a programmable 4 stage binary counter, a 4 × 16 decode matrix, and 16 single-pole double-throw switches.

The Shunt Enable control line permits the selection of Current Mode or Voltage Mode operation and in conjunction with the Current Mode, matching resistors are provided to improve accuracy. The Differential Mode Control allows the switches to operate as eight ganged pairs, while the Matrix Inhibit line allows multiple AY-5-1016's (or AY-6-4016's) to be connected to form larger multiplexing arrays. The Load Enable control allows synchronous loading of the 4 address inputs on a low to high transition of the Clock. The DC load control is provided for asynchronous loading of the address inputs independent of the Clock and Load Enable inputs. The Sync Output occurs whenever Channel 15 is selected and is provided to allow expansion in the sequential mode of operation. Also by connecting the Sync Output to the Load Enable Input, the counter length can be programmed via the address inputs. Any desired length of from 1 to 16 states can be programmed in this manner.

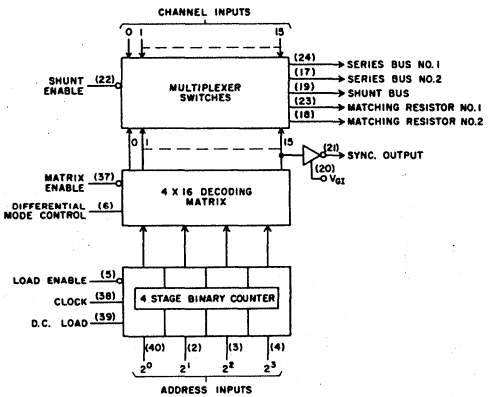
PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View



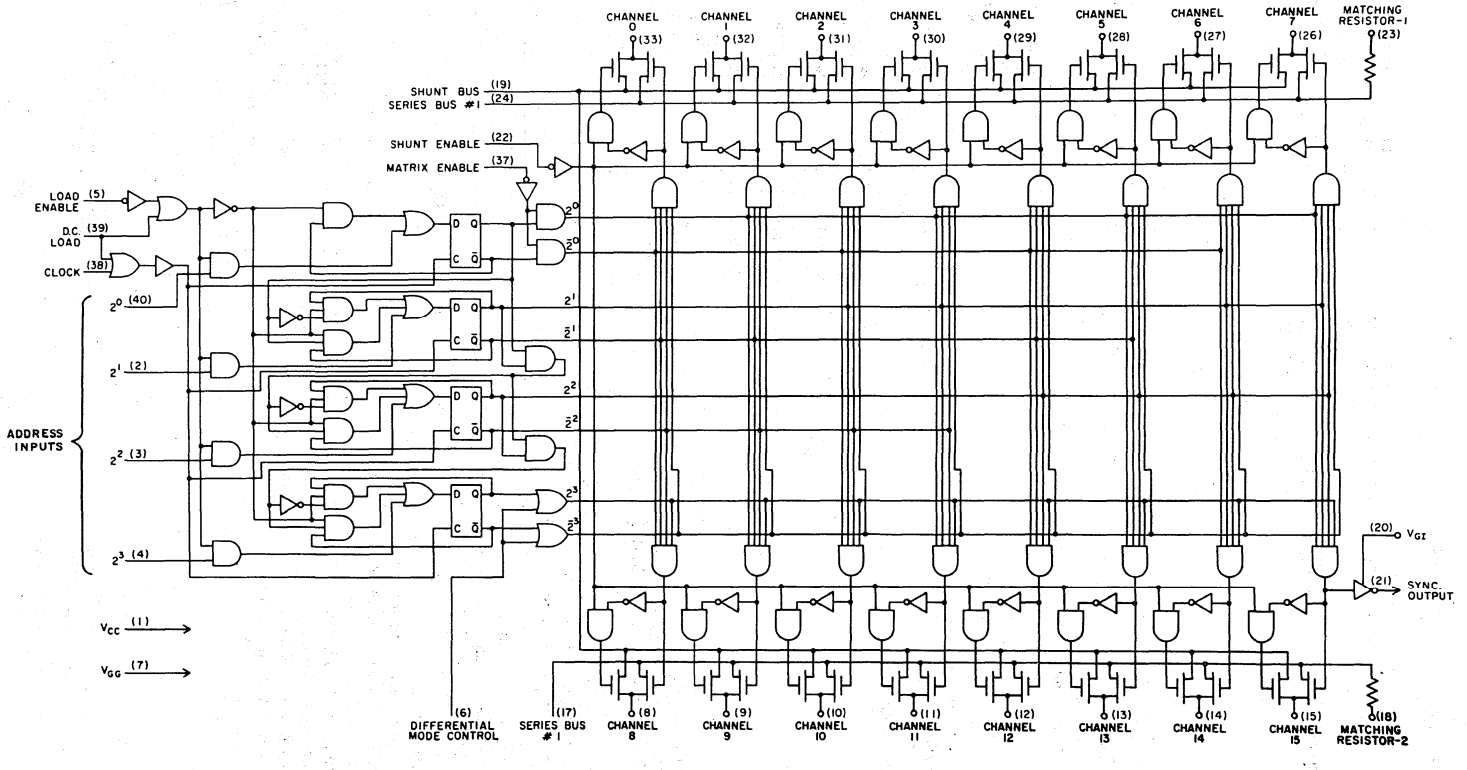
BLOCK DIAGRAM



TELECOM

LOGIC DIAGRAM

( ) = Pin Numbers



NOTES:

1. Direct Address gated when either DC Load = "1" or Load Enable = "0".
2. DC Load gives permanent high clock.
3. Matrix Enable = "1" inhibits matrix.
4. Shunt Enable = "0" connects shunt FETS into circuit.
5. Differential Mode Control = "1" connects channels 8-15 ganged to channels 0-7.
6. Sync Output = "0" when channel 15 is accessed.

ELECTRICAL CHARACTERISTICS

Maximum Ratings *

V_{GI} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Clock and Logic Input Voltages (with respect to V_{CC}) . . . . . −20V to +0.3V
Bus Voltages (Bus 1, Bus 2, and Shunt Bus with respect to V_{CC}) . . . −20V to .3V
Matching Resistor Nodes (with respect to V_{CC}) . . . . . −20V to .3V
Storage Temperature . . . . . −55°C to +150°C
Operating Temperature Range: . . . . . 0°C to +70°C (AY-5-1016)
−55°C to +125°C (AY-6-4016)

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} = Substrate voltage)
V_{GG} = −12 Volts ±1 Volt
V_{GI} = GND
Operating Temperature (T_A) = −0°C to +70°C (AY-5-1016)
−55°C to +125°C (AY-6-4016)

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Inputs (See Fig.1)					
Repetition Rate	DC	—	2.0	MHz	
Clock Pulse Width (ϕpw)	200	—	—	ns	at 2MHz, (See Note 1)
Clock Pulse Width (ϕpw)	1.0	—	—	μs	at 200Hz
Clock Pulse Delay (ϕd)	200	—	—	ns	See Note 1
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	12	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Rise & Fall Time (tr, tf)	—	—	1.0	μs	at 100 kHz
Rise & Fall Time (tr, tf)	—	—	50	ns	at 2MHz
Noise Immunity	+0.4	—	—	V	
Address Inputs (See Fig.1)					
Clock Lead Time	300	—	—	ns	
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	6	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Noise Immunity	+0.4	—	—	V	
Load Enable Input (See Fig.1)					
Clock Lead Time	300	—	—	ns	
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	7	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Noise Immunity	+0.4	—	—	V	
DC Load Input (See Fig.2)					
Pulse Width (90% points)	400	—	—	ns	
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	8	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Noise Immunity	+0.4	—	—	V	

**Typical values are at +25°C and nominal voltages.
NOTE 1: ϕpw + ϕd ≥ 500ns

TIMING DIAGRAMS

Fig.1

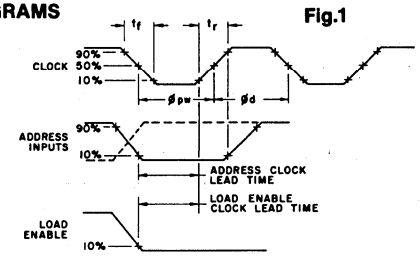
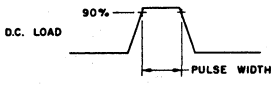


Fig.2



NOTE: Address Inputs and the Load Enable Input must be present during the 0 to 1 transition of the Clock.

TELECOM

Characteristic	Min	Typ**	Max	Units	Conditions
Shunt Enable					
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}–1.5	—	—	V	
Input Capacitance	—	6	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to –5V
Noise Immunity	+0.4	—	—	V	
Matrix Enable					
Response Time (See Fig. 3)					
T_{ON}	—	230	—	ns	} at 25°C Output voltage
T_{OFF}	—	120	—	ns	} response with10 MΩ, 10 pF load
Logic Levels					
Logic "0"	—	—	0.8	V	
Logic "1"	V_{CC}–1.5	—	—	V	
Input Capacitance	—	7	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN}= +5V to –V
Noise Immunity	+0.4	—	—	V	
Differential Mode Control					
Response Time (See Fig. 4)					
T_{ON}	—	200	—	ns	} at 25°C Output voltage
T_{OFF}	—	600	—	ns	} response with 10 MΩ, 10 pF load
Logic Levels					
Logic "0"	—	—	0.8	V	
Logic "1"	V_{CC}–1.5	—	—	V	
Input Capacitance	—	5	—	pF	
Input Impedance	1.0	—	—	MΩ	
Noise Immunity	0.4	—	—	V	
Series Switches					
R on (Current Mode)	—	460	750	Ω	I_{IN} = 100 μA Series Bus 1 = Series Bus 2 = 0V (V_{CC} –5V) T_A = 25°C V_{CC} = +5V V_{GG} = 12V
R on (Voltage Mode)	—	300	500	Ω	V_{IN} = +5V, R_L = 300 KΩ T_A = 25°C V_{CC} = +5V V_{GG} = –12V
	—	460	750	Ω	V_{IN} = 0V , R_L = 300 KΩ T_A = 25°C V_{CC} = +5V V_{GG} = –12V
R off	—	5	—	GΩ	V_{IN} = V_{CC} –10V T_A = 25°C
Turn On Time	—	300	—	ns	Output Voltage Waveform with 10 MΩ, 10 pF load T_A = 25°C

**Typical values are at 25°C and nominal voltages.

TIMING DIAGRAMS

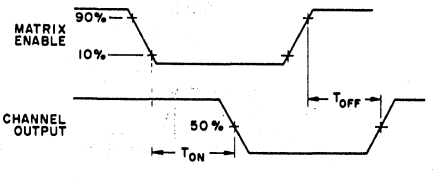


Fig.3

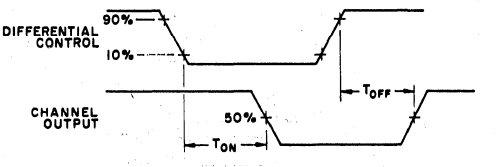


Fig.4

Characteristic	Min	Typ**	Max	Units	Conditions
Sync Output (See Fig.5)					
Logic "0"	—	—	+0.4	V	C = 10pF, I_{SINK} = 1.6mA min., I_{OF} = 100 μA min. } Output Load
Logic "1"	V_{CC}–1.0	—	—	V	
Rise Time (tr)	—	110	—	ns	at 25°C
Fall Time (tf)	—	40	—	ns	at 25°C
Response Time					
tpd –	—	200	—	ns	at 25°C
tpd +	—	160	—	ns	at 25°C
Input Leakage					
Channels 0-15 (Per Channel)	—	1.0	10	nA	V_{IN} = V_{CC} –5V at 25°C
Series Bus 1, 2	—	3.0	30	nA	V_{BUS} = V_{CC} –5V at 25°C
Shunt Bus	—	3.0	30	nA	V_{BUS} = V_{CC} –5V at 25°C
Shunt Switches					
R on	—	850	1300	Ω	I_{IN} = 100 μA, Shunt Bus = OV, V_{CC} = +5V, V_{GG} = —12V, T_A = 25°C
	—	550	900	Ω	I_{IN} = 100 μA, Shunt Bus = +5V, V_{CC} = +5V, V_{GG} = –12V, T_A = 25°C
R off	—	5	—	GΩ	V_{IN} = V_{CC} –10V, T_A = 25°C
Turn On Time	—	300	—	ns	Output Voltage Waveform with 10 MΩ, 10 pF load, T_A = 25°C
Matching Resistors	—	460	750	Ω	i_{IN} = 100 μA, V_{BUS} = OV
R on	—	300	500	Ω	I_{IN}= 100 μA, V_{BUS} = +5V
Channel Input Capacitance, Channels 0-15 (Per Channel)	—	4	—	pF	
Power Consumption	—	200	—	mW	Series MODE, V_{GG} = –12V, V_{CC} = +5V
	—	290	—	mW	Shunt MODE, V_{GG} = –12V, V_{CC} = +5V
Current Drain					
I_{CC}	—	12	—	mA	Series MODE, V_{GG} = –12V, V_{CC} = +5V
I_{GG}	—	12	—	mA	Series MODE, V_{GG} = –12V, V_{CC} = +5V
I_{CC}	—	17	—	mA	Shunt MODE, V_{GG} = –12V, V_{CC} = +5V
I_{GG}	—	17	—	mA	Shunt MODE, V_{GG} = –12V, V_{CC} = +5V
Power Dissipation (Device)	—	—	600	mW	
Per Channel	—	—	100	mW	

Typical values are at 25°C and nominal voltages.

TIMING DIAGRAMS

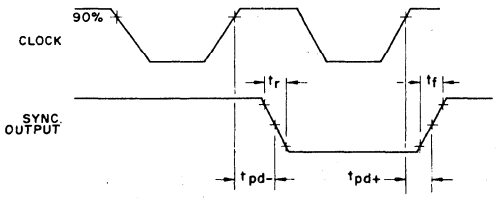
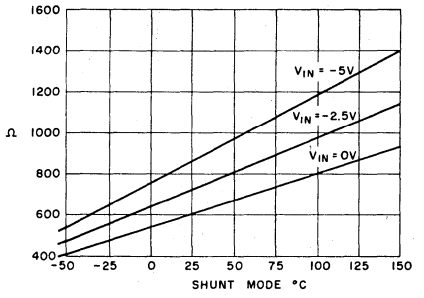
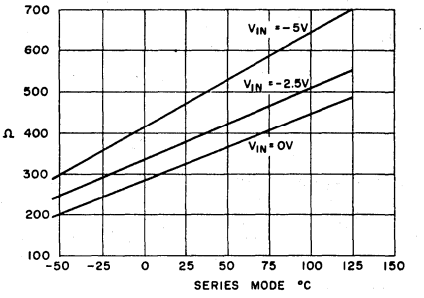
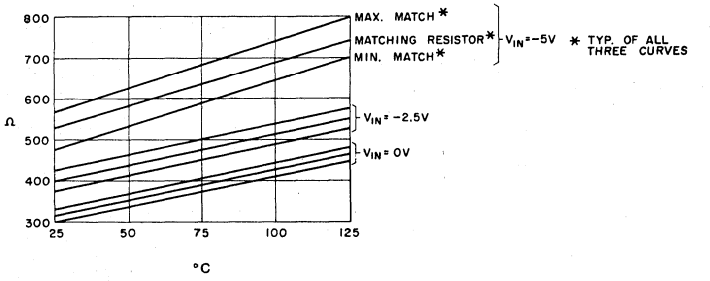


FIG.5

TYPICAL CHARACTERISTIC CURVES







TELECOM

Entertainment 7

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
			Radio
PROGRAMMABLE PLL TUNING CONTROLLERS	Provides full electronic control of a varactor tuned AM/FM radio mask programmable for custom tuning function. (ref. ER1400 for optional unpowered memory.)	AY-3-8118	7-4
	Microcomputer radio tuning controller. (ref. ER2055 for optional unpowered memory.)	AY-3-8120	7-10
			Television
OMEGA 82 CHANNEL TUNING SYSTEM	Provides full electronic control of a varactor-tuned 82-channel television from a two-digit calculator-like keyboard entry.	T-1002	7-14
		T-1102	7-14
		ER1400	7-18
		MEM 4956	7-21
		T-1201	7-14
ECONOMEGA 16 CHANNEL TUNING SYSTEM	Provides full electronic control of a varactor-tuned 8, 12 or 16 channel television, featuring automatic or manual tuning.	AY-3-8203	7-24
		ER1400	7-18
		MEM 4956	7-21
ECONOMEGA IIA TUNING SYSTEM	Provides electronic control of a varactor tuned TV from keyboard entry.	AY-3-8211	7-30
		ER1400	7-18
ECONOMEGA IV PLL TUNING SYSTEM	A five chip TV frequency synthesizer system.	AY-9-2010	7-38
		AY-3-2022	7-38
		PIC 1650	7-38
		ER1400	7-38
		AY-9-2017	7-38
ON-SCREEN CHANNEL/TIME DISPLAY	Various circuits in series to display channel numbers on TV screen with some additionally featuring either separate or simultaneous time display (ref. AY-5-1203A clock circuit)	AY-5-8301	7-39
		AY-5-8320	7-39
		AY-5-8321	7-39
ON-SCREEN TUNING SCALE	Provides an electronic on-screen tuning scale for varactor-tuned TV sets.	AY-3-8331	7-48
			Remote Control
R/C SYSTEM I	30 channel discrete frequency ultrasonic transmitter.	AY-5-8450	7-52
	16 channel discrete frequency ultrasonic receivers.	AY-5-8460	7-54
R/C SYSTEM II	264 command PCM infrared transmitter.	AY-3-8470	7-58
	264 command PCM infrared receiver.	AY-3-8475	7-64
			Sound Generation
TOP OCTAVE GENERATORS	Generates a complete octave of musical frequencies.	AY-1-0212	7-72
		AY-3-0214	7-74
		AY-3-0215	7-74
LATCHING NETWORK	Establishes priority of 13 pedal latch inputs/outputs.	AY-1-1313	7-76
CHORD GENERATOR	Produces major, minor, 7th chords, walking bass.	AY-5-1317A	7-78
PIANO KEYBOARD	Electronically simulates piano keyboard operation.	AY-1-1320	7-82
FREQUENCY DIVIDERS	7 stage dividers.	AY-1-5050	7-86
PROGRAMMABLE SOUND GENERATORS	Generates programmable sound effects via a microcomputer compatible bus without the aid of external components.	AY-3-8910	7-88
		AY-3-8912	7-88
MICRO-COMPUTER TUNES SYNTHESIZER	Produces musical tunes from pre-programmed microcomputer.	AY-3-1350	7-95

GENERAL INSTRUMENT

Radio

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
PROGRAMMABLE PLL TUNING CONTROLLERS	Provides full electronic control of a varactor tuned AM/FM radio mask programmable for custom tuning functions. (ref. ER1400 for optional unpowered memory.)	AY-3-8118	7-4
	Microcomputer radio tuning controller.(ref. ER2055 for optional unpowered memory.)	AY-3-8120	7-10

Programmable Phase-Locked-Loop AM/FM Radio Tuning Controller

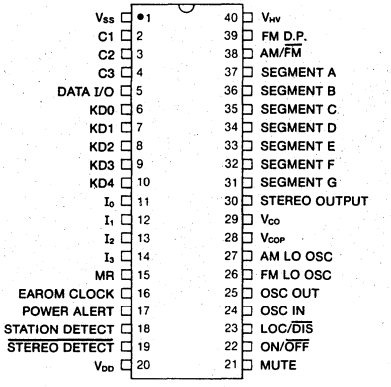
FEATURES

- On-chip fluorescent display drivers (5 digits)
- On-chip PLL directly drives varactor tuner
- Mask programmable IF frequency (4 to 460kHz AM)(10.7MHz FM)
- On-chip 2.6MHz oscillator (external crystal required)
- Internal Microcomputer architecture with 128 x 29 instruction ROM
- Internal digit and keyboard debounce circuitry
- Single mask customization permitting options such as:
  a. Manual tune up/down, local/distant
  b. Automatic search up/down, local/distant
  c. Automatic stereo search up/down, local/distant
  d. Scan (audition)
  e. Favorite scan
  f. Direct digit entry
- Ten favorite station selections (any mix AM/FM)
- AM, FM, Stereo indicator drivers
- Optional EAROM interface or internal favorite station memory
- Emulation and PROM programmable field demonstrator available

PIN CONFIGURATION

40 LEAD DUAL IN LINE
AY-3-8118

Top View



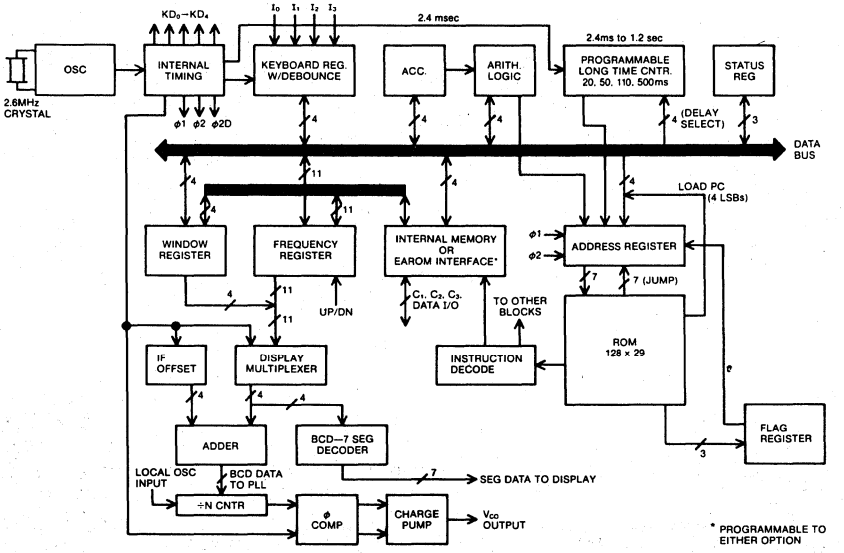
DESCRIPTION

The AY-3-8118 is a dedicated microcomputer designed specifically to control a phase-locked-loop varactor-tuned AM/FM radio. It is intended for use in the automotive and home stereo receiver market.

The AY-3-8118 is designed to operate in a receiver system with a minimum of support components. The AY-3-8118 has an on-chip fluorescent display driver, a phase-locked-loop comparator with charge pump, direct keyboard decoding and built-in EAROM interface for optional add-on unpowered memory retention.

Being microcomputer based, the AY-3-8118 allows for internal ROM programming to alter operating characteristics thus performing custom tuning functions. These alterations in the program allow for various functions such as automatic or manual station searching, up and down scan and audition of each station, scan of favorite stations stored in memory, and for direct entry by frequency of a radio station.

AY-3-8118 BLOCK DIAGRAM



ENTER-TAINMENT

PIN FUNCTIONS

Pin No.	Name	Function
1	V_{SS}	Negative supply (ground)
2,3,4	C1,C2,C3	Mode control signals for ER1400
5	Data I/O	Bi-directional data transfer line to and from ER1400.
6-10	KD0,KD1,KD2,KD3,KD4	Outputs from controller: they strobe both the display digit drive and the matrix keyboard. A digit drive is high to enable a digit.
11-14	I_0,I_1,I_2,I_3	Inputs from 4 x 5 matrix keyboard. Pull down resistors are provided internally.
15	MR	Master reset for the controller; on the low to high transition of this signal, a status restoration routine is executed. No internal pull up resistor is provided.
16	EAROM Clock	Timing reference to ER1400. (Grounding this pin selects internal RAM memory.)
17	Power Alert	This input is low to indicate V_{DD} will drop in no less than 80ms. When this input is low, the keyboard is locked out and mute is held high.
18	Station Detect	Input from radio; high to indicate the presence of a station. A pull-up resistor is provided internally.
19	$\overline{\text{Stereo Detect}}$	Input from radio; low to indicate the presence of a stereo station. A pull-up resistor is provided internally.
20	V_{DD}	Positive supply (12V nominal).
21	Mute	Output from controller; high to silence radio during station change operations.
22	On/$\overline{\text{Off}}$	Output from controller; high to switch radio on, low for off.
23	Loc/$\overline{\text{Dis}}$	Output from controller; high to reduce sensitivity of station detector to implement local/distant search operations.
24,25	OSC IN, OSC OUT	These pins are for connection to a 2.6MHz crystal network.
26	FM LO OSC	This input is for the FM local oscillator. It must be divided externally by a ÷100 prescaler.
27	AM LO OSC	This input is for the AM local oscillator.
28	V_{COP}	Positive power supply to V_{CO} buffer.
29	V_{CO}	This output is used to control the AM and FM local oscillators.
30	Stereo Output	Used to drive stereo indicator; high to indicate stereo search or presence of stereo station.
31-37	Segments G,F,E,D,C,B,A	Controller output drivers to fluorescent display; high for segment on, low for off.
38	AM,$\overline{\text{FM}}$	Band identification outputs to fluorescent display. High indicates band of operation.
39	FM Decimal Point	Connects to D.P. on display.
40	V_{HV}	High voltage power supply input to VF drive buffers.

ROM BASIC INSTRUCTION FORMAT

Name	$\overline{K_1}\,\overline{K_2}\,\overline{K_3}\,\overline{K_4}$	S_0 S_1 S_2	Load/ Jump	Band/ Step	Cmd. Enbl.	Jmp_3 Jmp_2 Jmp_1	$\overline{Ld}$ Acc	$\overline{Rd}$ Acc	$\overline{Enbl}$ AM/FM	$\overline{Rd}$ ROM	R_0 R_1 R_2 R_3	J_0 J_1 J_2 J_3 J_4 J_5 J_6	$\overline{Ld}$ PC
Bit No.	1 2 3 4	5 6 7	8	9	10	11 12 13	14	15	16	17	18 19 20 21	22 23 24 25 26 27 28	29
Function	Command Bus FM Data to Bus	**Step Mode** Binary Code Represents Step # **Band Mode** S_0 S_1 S_2 0 0 1 set AM 0 1 0 set FM 0 0 0 no change	Selects Load or jmp in Step mode	Selects Band or Step mode	Enables Command Code	**Jump Mode** 000 No Jump 001 ≠ 010 = 011 $\overline{eq}$ 100 eq 101 > 110 < 111 uncond	Loads Acc with Data Bus	Places Acc on Data Bus	Places AM/$\overline{FM}$ data on Data Bus	Places ROM data on Data Bus	Rom Data to Bus AM Data to Bus	Jump Address	Ld Program Counter 111+Data Bus (111 $R_3R_2R_1R_0$)

Fig. 4

ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... −3 to 18 Volts
Storage temperature range ..... −65°C to 150°C
Ambient operating temperature range ..... −30°C to 70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{DD} = +9.0 to +13.5 Volts
V_{SS} = 0 Volts
T_A = −30°C to +70°C

Characteristic	Min	Max	Units	Conditions
Local Oscillator Inputs				
AM Local Oscillator Input				
Logic 1	3.5	V_{DD}	V	
Logic 0	−0.3	0.5	V	
Frequency Range	0.53	2.5	MHz	
FM Local Oscillator Input				
Logic 1	3.5	V_{DD}	V	
Logic 0	−0.3	0.5	V	
Frequency Range	0.881	1.2	MHz	
Function Inputs				
Station Detect, $\overline{\text{Stereo Detect}}$ Inputs				
Logic 1	5.0	V_{DD}	V	
Logic 0	−0.3	0.5	V	
Input pull up current	0.2	−1.5	mA	
Power Alert Input				
Logic 1	7.0	V_{DD}	V	
Logic 0	−0.3	0.5	V	
Master Reset Input				
Logic 1	V_{DD}−2	V_{DD}	V	
Logic 0	−0.3	1.0	V	
Keyboard Inputs $\overline{I_0}$-$\overline{I_3}$				
Logic 1	5.0	V_{DD}	V	
Logic 0	−0.3	0.5	V	
Input pull down current	50	500	μA	
Outputs				
Digit Strobe Outputs				
Logic 1	V_{DD}−3	V_{DD}	V	at 2.1mA
Logic 0	2.0	3.0	V	at 0.7mA
Segment A-G, FM, AM, Stereo Outputs				
Logic 1	V_{DD}−3	V_{DD}	V	at 0.7mA
Logic 0	2.0	3.0	V	at 0.7mA
Mute Local/$\overline{\text{Distant}}$ Outputs				
Logic 1	5.0	V_{DD}	V	at 0.5mA
Logic 0	0	0.5	V	at 0.1mA
On/$\overline{\text{Off}}$ Output				
Logic 1	5.0	V_{DD}	V	at 1.5mA
Logic 0	0	0.5	V	at 0.1mA
EAROM Interface				
Data I/O				
Input Logic 0	—	−5	V	
Input Logic 1	V_{DD}−2	—	V	
Output Logic 0	0	V_{DD}−8	V	
Output Logic 1	V_{DD}−2	V_{DD}		
EAROM Clock, C1, C2, C3 Outputs				
Output Logic 1	0	V_{DD}−8	V	
Output Logic 0	V_{DD}−2	V_{DD}		
Power Supply Current				
I_{DD}	—	40	mA	
Display Input Voltage				
V_{HV}	0	24.0	V	
Varactor Input Supply Voltage				
V_{COP}	0	18.0	V	

ENTER-TAINMENT

OPERATION

The functions of the AY-3-8118 are controlled by the self-contained microcomputer within the chip. The microcomputer uses several working registers which are under control of the Program ROM.

Internally the chip takes the AM or FM local oscillator input and compares it against a preselected frequency count digitally. The preselected frequency can be inserted by the user either from direct keyboard entry or from memory (internal RAM or external EAROM). The filtered Vco output is then changed either up or down in voltage to make the local oscillator agree in frequency measurement with the preselected frequency.

The AY-3-8118 uses a 2.6MHz crystal to control the on-board oscillator which produces the total internal clocking functions. The microprogram is used to control the features operations such as scan the keyboard, display the frequencies and band selection. An important feature of the AY-3-8118 is the internal window register which is programmed to display a fifth alphanumeric segment digit on the display. This fifth digit may be used to display the functional mode of the chip and indicate when the chip is in the program mode, automatic search mode, entry mode and the stored program number.

The AY-3-8118 contains a RAM for program storage, thus requiring power to remain on the chip for memory. An optional EAROM, General Instrument part number ER1400 can be interfaced directly with the AY-3-8118 to store program information without power having to remain on.

AY-3-8118-001 and -002 STANDARD PARTS

General Instrument has developed two standard AY-3-8118 parts for circuit evaluation, system developments and general use.

These parts share the same functions and differ only in their AM local oscillator input frequencies. The AY-3-8118-001 has been programmed to accept an IF frequency of 260kHz and the AY-3-8118-002 accepts 455kHz as an AM IF input frequency.

The AY-3-8118 standard parts are programmed to do the following functions:

1. Automatic and manual search tune both the AM and FM bands in both local and distant modes
2. Accept manual entry of station frequencies digit by digit
3. Display AM and FM functions on the display
4. Accept 10 favorite stations in AM, FM or any combinations
5. 19-key keyboard with 1 spare
6. Mode Window to indicate Enter, Program and Auto Modes
7. Automatic Stereo Search
8. Keyboard power ON/OFF

The keyboard layout is as follows:

	I_0	I_1	I_2	I_3
KD_0	0	1	2	3
KD_1	4	5	6	7
KD_2	8	9	LOC	DIS
KD_3	AM	FM	STEREO	ON/OFF
KD_4	NOT USED	UP	DOWN	P/B SET

PROGRAMMING

Custom programs can be composed and simulated with the AY-3-8118 emulator available from General Instrument Microelectronics. This emulator when connected to an appropriate teletype with a paper tape punch enables the customer to produce a custom program to control his receiver system and a punched tape of the program. The tape then enables General Instrument to manufacture a custom mask and produce custom programmed AY-3-8118s.

Also available will be field demonstrators which consist of a ROM-less AY-3-8118 supported by standard PROMs all on a single printed circuit board. This field demonstrator will enable a customer to demonstrate his custom programs in a small module which can be contained in a prototype system.

For more information on AY-3-8118 emulators, and field demonstrators, contact any General Instrument Microelectronics sales office.

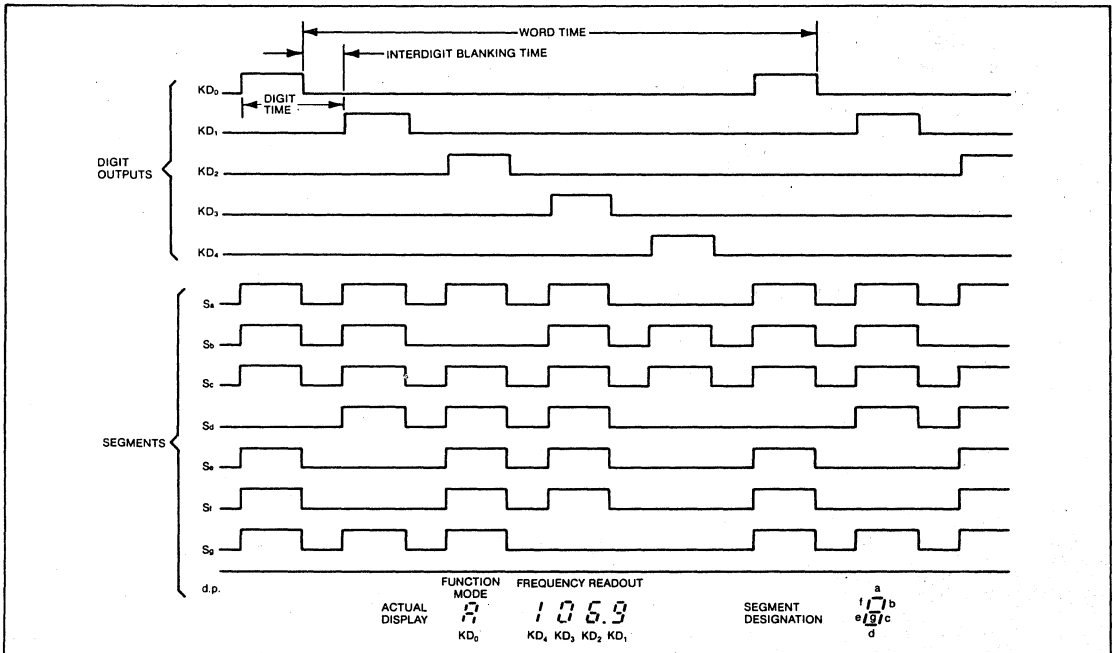


Fig. 5 DIGIT STROBE AND DISPLAY LOGIC TIMING DIAGRAM

	8 of 29 Internal ROM Bits								
Function	**K4**	**K3**	**K2**	**K1**	**R3**	**R2**	**R1**	**R0**	**Secondary**
Read Keyboard	0	0	0	1	X	X	X	X	
Read Keyboard Numeric	0	0	1	0	X	X	X	X	Reset Keyboard Latch
Reset Keyboard Latch	0	0	1	0	X	X	X	X	Read Keyboard Numeric
	0	1	1	1	0	X	X	X	
Reset Long Time Counter	0	1	0	0	X	X	X	X	
	1	1	X	1	X	X	X	X	Reset Stereo Blank
Read Long Time Counter (20 msec)	0	1	0	1	1	1	1	0	
Read Long Time Counter (50 msec)	0	1	0	1	1	1	0	1	Set Mute
Read Long Time Counter (110 msec)	0	1	0	1	1	0	1	1	
Read Long Time Counter (500 msec)	0	1	0	1	0	1	1	1	
Read Status	0	1	1	0	X	X	X	X	
Set On/$\overline{\text{Off}}$	0	1	1	1	0	0	0	1	Reset Keyboard Latch
Reset On/$\overline{\text{Off}}$	0	1	1	1	0	1	1	1	Reset Keyboard Latch
Set Local/$\overline{\text{Dist}}$	0	1	1	1	0	0	1	1	Reset Keyboard Latch
Reset Local/$\overline{\text{Dist}}$	0	1	1	1	0	1	0	0	Reset Keyboard Latch
Set Stereo	0	1	1	1	0	1	0	1	Reset Keyboard Latch
Reset Stereo	0	1	1	1	0	1	1	0	Reset Keyboard Latch
Set Mute	0	1	0	1	1	1	0	1	Read Long Time Counter 50 msec
Reset Mute	0	1	1	1	1	0	0	0	Reset Search
Set Stereo Blank	0	1	1	1	1	0	0	1	
Reset Stereo Blank	1	X	X	X	X	X	X	X	
Load All (S1,S2,S3, & Window)	1	1	1	0	X	X	X	X	Reset Stereo Blank, Ld. Window
Load Window	1	X	1	0	X	X	X	X	Reset Stereo Blank
Load S1	1	0	0	1	X	X	X	X	Reset Stereo Blank
Load S2	1	0	0	0	X	X	X	X	Reset Stereo Blank
Load S3	1	0	1	1	X	X	X	X	Reset Stereo Blank
Set Up F/F	1	1	0	0	0	0	0	1	Set Search FF, Reset Stereo Blank
Reset Up F/F	1	1	0	0	0	0	1	0	Set Search FF, Reset Stereo Blank
Set Search F/F	1	1	0	0	0	0	X	X	Reset Stereo Blank
Reset Search F/F	0	1	1	1	1	0	0	0	Reset Mute
Inc/Dec Freq. Counter	1	1	0	0	1	0	0	0	Reset Stereo Blank, Reset LTC
Send Favorite to EAROM	1	1	0	1	0	0	0	0	Reset Stereo Blank, Reset LTC
Recall Favorite	1	1	0	1	0	0	0	1	Reset Stereo Blank, Reset LTC
Send Favorite to EAROM	1	1	0	1	0	0	1	0	Reset Stereo Blank, Reset LTC
Recall Power Freq.	1	1	0	1	0	0	1	1	Reset Stereo Blank, Reset LTC
Send Power Status & Window	1	1	0	1	0	1	0	X	Reset Stereo Blank, Reset LTC
Recall Power Status & Window	1	1	0	1	0	1	1	X	Reset Stereo Blank, Reset LTC
Recall Status Only	1	1	0	1					Reset Stereo Blank, Reset LTC
End Erase	1	1	1	1	0	0	0	1	Reset Stereo Blank, Reset LTC
End Write	1	1	1	1	0	0	1	0	Reset Stereo Blank, Reset LTC

*Send Status Only 1101
X = Don't Care

Fig. 6 STANDARD FUNCTIONAL MICRO INSTRUCTION FORMAT

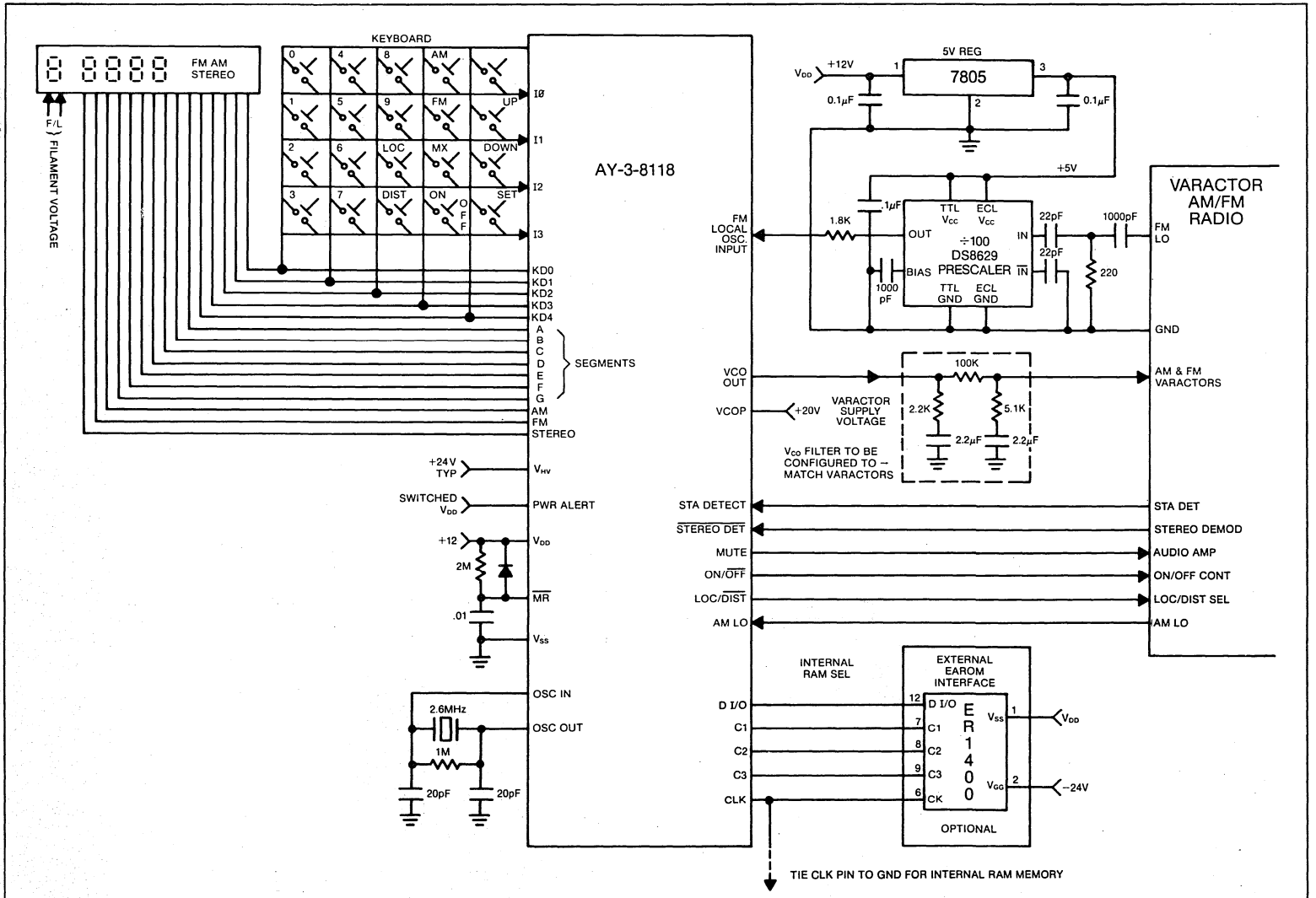


Fig. 7 AY-3-8118 BASIC AM/FM RECEIVER DIAGRAM

ENTER-TAINMENT

Programmable Phase-Locked-Loop AM/FM Radio Tuning Controller

BASIC FEATURES

- Microcomputer Controller
- Covers standard AM/FM bands including the new FCC created bands
- Stores 10 favorite stations—5 AM and 5 FM
- Manual two speed tune up and down
- Signal Seek Up—scans up frequency band at a rate of 20 channels per second. Stops at first valid station and locks loop
- Mute Output controls receiver amplifier during tuning operations
- Four digit common anode LED display direct drive
- Interfaces with General Instrument EAROM for unpowered station memory

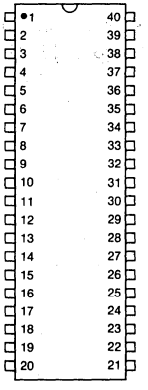
OPTIONAL FEATURES

- Interfaces with remote control operation easily
- Direct digit by digit frequency entry by keyboard
- Favorite Station scan—scans only frequencies stored in memory
- Pin Programmable IF correction—compensates for inaccuracies of filters used in FM reception
- On board time-of-day clock

PIN CONFIGURATION

40 LEAD DUAL IN LINE
AY-3-8120

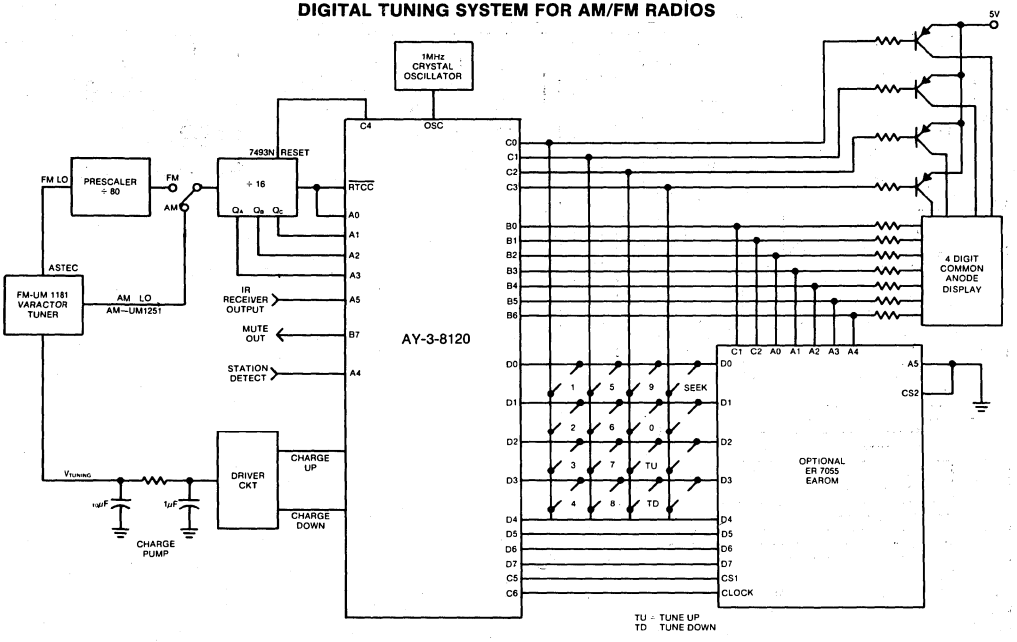
Top View



to be defined

BLOCK DIAGRAM

DIGITAL TUNING SYSTEM FOR AM/FM RADIOS



ENTER-TAINMENT

SYSTEM OPERATION

An external TTL counter is used to divide the AM local oscillator frequency by sixteen. This input then drives the PIC real time counter. The maximum AY-3-8120 input frequency is 125 kc/s since the maximum AM local oscillator frequency is 2 mc/s. By dividing the FM local oscillator frequency by a further eighty, an input similar to the AM frequency is obtained.

Typical time specifications require the station to be tuned to within 150 kc/s on the AM range and 20 kc/s on the FM range. This requires the frequency to be measured to an accuracy of 14 bits. By utilizing the parallel output from the TTL counter as intputs to the AY-3-8120, the time taken to measure to this accuracy can be reduced to some 8 milliseconds. Over this period of time, one bit will be equivalent to 125 kc/s on the AM range and 10 kc/s on the FM range.

During the scan mode the frequency measurement need only be sufficiently accurate to reliably display the station frequency. Measuring to 12 bits over a 3ms period is sufficient for stations separated by 10 kc/s on AM and 200 kc/s on FM. The nearest channel is displayed i.e., the display changes about the middle of the frequency gap between two stations. The scan rate should be about 20 channels/sec.

In the control loop the AY-3-8120 keeps measuring the input frequency and compares it with an internally generated number. Any error causes the PIC to generate a pulse on either the charge up or the charge down line. A small error causes the AY-3-8120 to put out a series of very short pusles, the number of pulses dependent on the error. In the tune-up or tune-down mode the PIC generates a long pulse on each increment of channel on the appropriate output and then a series of shorter pulses to properly tune-in the station. When the push buttons are held down continuously, a DC level is applied on the appropriate output. During this time the receiver is muted. The value of the change capacitor is so chosen that the maximum setting time is 100ms. The maximum allowable ripple on the tuning voltage is 300 μV in lock.

Television

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
OMEGA 82 CHANNEL TUNING SYSTEM	Provides full electronic control of a varactor-tuned 82-channel television from a two-digit calculator-like keyboard entry.	T-1002	7-14
		T-1102	7-14
		ER1400	7-18
		MEM 4956	7-21
		T-1201	7-14
ECONOMEGA 16 CHANNEL TUNING SYSTEM	Provides full electronic control of a varactor-tuned 8, 12 or 16 channel television, featuring automatic or manual tuning.	AY-3-8203	7-24
		ER1400	7-18
		MEM 4956	7-21
ECONOMEGA IIA TUNING SYSTEM	Provides electronic control of a varactor tuned TV from keyboard entry.	AY-3-8211	7-30
		ER1400	7-18
ECONOMEGA IV PLL TUNING SYSTEM	A five chip TV frequency synthesizer system.	AY-9-2010	7-38
		AY-3-2022	7-38
		PIC 1650	7-38
		ER1400	7-38
		AY-9-2017	7-38
ON-SCREEN CHANNEL/TIME DISPLAY	Various circuits in series to display channel numbers on TV screen with some additionally featuring either separate or simultaneous time display (ref. AY-5-1203A clock circuit)	AY-5-8301	7-39
		AY-5-8320	7-39
		AY-5-8321	7-39
ON-SCREEN TUNING SCALE	Provides an electronic on-screen tuning scale for varactor-tuned TV sets.	AY-3-8331	7-48

OMEGA / 82 Channel Digital Tuning System

SYSTEM DESCRIPTION

The Omega System combines an electronic solid state channel selector with a VHF/UHF varactor tuner pair. The system accepts a calculator-like 2 digit keyboard entry and provides the selected channel number on a two digit seven element display. Controls are also provided for fine-tune, coarse-tune, search, digital step tuning up and down. Single digit entry for favorite television channels is available as a design option.

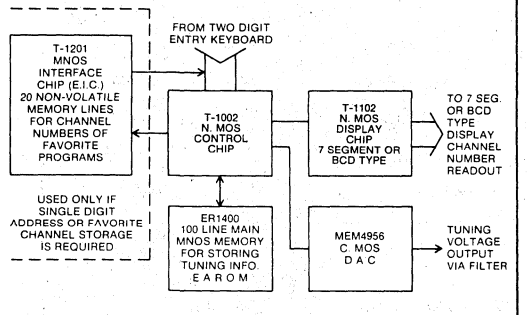
The digital counterparts of the analog channel voltages corresponding to the frequencies tuned are stored in a non-volatile Electronically Alterable Read Only Memory (EAROM) which retains, without standby power, the desired coarse- and fine-tune data for all channels. The system has been designed to be extremely insensitive to supply voltage variations, component aging and environmental changes. The tuning accuracy depends only on a single well regulated reference voltage for its stability.

The method of D/A conversion used is a pulse width modulator driving a low-pass filter. The DC component out of the filter is applied to the varactor tuner. A complementary MOS device is used between the control chip and the low-pass filter to achieve the precise and stable amplitudes required at the input to the filter.

The EAROM is a 1400 bit solid state memory organized into one hundred words of 14-bits each. This technology provides a non-volatile memory for 98 channels of tuning information. Two words or lines in the EAROM are reserved to remember the two digit channel number for the last program selected by the viewer. When the set is turned on again after being off indefinitely, it automatically selects the last channel selected before shut down. Each word can be erased and rewritten without affecting the 99 other words and is updated any time the viewer adjusts the tuning of his set. Adequate space in the memory is provided for the 12 VHF and 70 UHF channels, plus 16 locations reserved for other services.

ENTER-TAINMENT

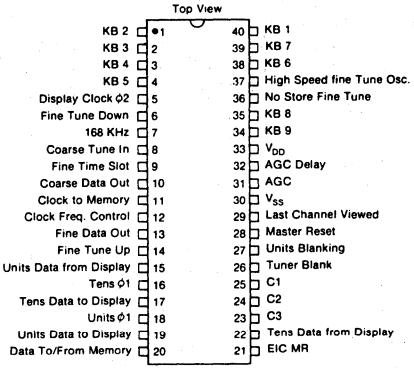
BLOCK DIAGRAM



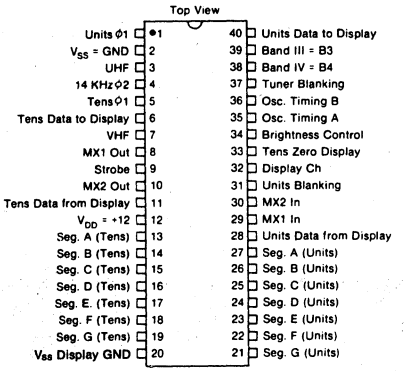
PIN CONFIGURATIONS

40 LEAD DUAL IN LINE

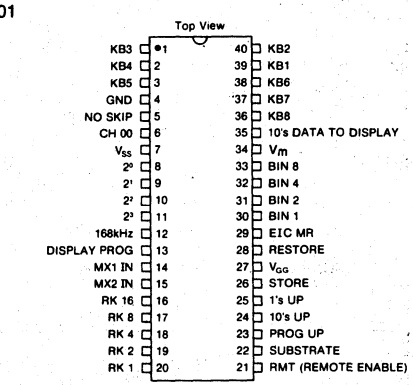
T-1002



T-1102



T-1201



Control Chip (T-1002)

The control chip scans the keyboard at a 14 kHz rate on constant alert for a switch closure. A closure may command one of the following functions:

(a) Two digit random channel selection
(b) Channel stepping (units or tens digits)
(c) Coarse-tune
(d) Fine-tune
(e) Search

The control chip also is designed to accommodate a signal input from a remote control receiver and a "power-up" signal from a power supply to trigger the last-channel-viewed function.

Display Chip (T-1102)

Each digit of the channel number entry is converted into a one-out-of-ten code and serially sent to the display chip where it is stored and decoded both for a seven segment or character generator display and for band switching.

EAROM Chip (ER1400)

This channel number is also used as a two digit address (00 thru 97) for the EAROM memory to locate the corresponding memory line. This twenty bit address is sent serially to the EAROM on a single wire bi-directional data bus.

The EAROM memory is designed to accept a two digit 20-bit address. This format was selected to provide ease of keyboard encoding, ease of display encoding, EAROM address decoding, and ease of address incrementation (one bit shift).

The slow speed and simple timing requirements of the memory permit address and data to flow both to and from memory on a single wire. A further economy of interconnects is achieved by using a three bit parallel code to command the memory into one of its seven modes of operation including: Input Address, Input Data, Erase, Write, Read, Data Out and Stand By.

For a complete description of the operation and specifications of the ER1400, refer to the separate data sheet in this section.

D/A Converter Chip (MEM 4956)

The CMOS D-to-A converter chip provides interface between the control chip outputs and the filter. In order to achieve optimum trade-off in the D/A system between clock frequency, ripple content of the filter output, and filter settling time, the 14-bit conversion is done in two parts. The 10 most significant bits generate a variable duty factor waveform with 1000 resolution elements of fixed amplitude.

The four least significant bits are used to generate a narrow pulse (equal in width to one coarse resolution element) but variable in amplitude to 15 discrete levels. The variable width and variable amplitude components are multiplexed together in the CMOS chip and drive the input to the low-pass filter. The filter integrates the area under both component waveforms and delivers a dc voltage to the varactor tuner. The ripple is kept below 100 μV and the settling time is about 50 ms. This is accomplished with a maximum clock rate of 1 MHz and with a resolution of 1 part in 15,000 of the reference supply voltage.

For a complete description of the operation and specifications of the MEM 4956, refer to the separate data sheet in this section.

Interface Chip (T-1201)

Where single digit entry is required for up to 20 favorite channels a fifth Chip (Interface Chip) is added to the system. This Interface Chip is a PMNOS device incorporating a 20 line non-volatile memory (EAROM) of 12 bits per line together with all logic functions to address the 20 line memory as well as to interface directly with the rest of the Omega system via the control chip keyboard input lines.

Each memory line in this chip is capable of storing a two digit channel number ("zero" before a single digit channel number) which is entered via a tens and ones input that can be sequenced through 0 to 9 with wraparound, but without carry over and can be stored by pressing a store button.

The channel number output from the display chip always shows the correct channel number that is stored in the data registers of the interface chip whenever any function on it is selected.

The tuning voltage output from the DAC also corresponds to the data stored in the main 100 line memory for that channel number. The Interface Chip uses a binary input keyboard to provide single digit access to each of up to twenty memory lines via a diode matrix or to directly interface with binary coded, remote systems for a single digit address.

Provision has been made for sequencing through all 20 memory lines for simplified remote control, with the capability of introducing a skip code (0,0) to bypass any memory line. Memory line or single digit button number outputs are also available in both binary and BCD format.

SYSTEM OPERATION

A. Two digit entry (4 chip OMEGA system)

To select a channel the viewer depresses two digits ("zero" before a single digit channel number) on a keyboard connected to the keyboard entry pins on the control chip. A one of six subroutine counter in the control chip is used to continuously scan the keyboard for a closure which then stops the scanner. A debounce device is used to confirm the closure after a debounce period of approximately 15 msecs. Confirmation of key closure converts the subroutine counter into a shift register which passes the data contained in it to a register in the display chip. The process is repeated when the second digit is entered. When both digits of a valid entry are received by the data registers in the display chip the following sequence occurs.

a) The control chip addresses word/line 99 in the 100 line main memory (EAROM) via the EAROM address register.

b) One digit of the channel number stored in the display chip registers is shifted via the control chip to the data register of the EAROM and upon receiving a "write" signal from the control chip the data is shifted into the EAROM memory line accessed by the address register (in this case line 99). This is repeated for writing the second channel number digit into line 98 and the combination represents the storing of the last channel viewed information used during power up of the system.

c) After storing the last channel viewed information the channel number stored in the display chip register is sent via the control chip to the address register of the EAROM so that the memory line corresponding to this channel number can be read on command from the control chip.

d) The read-from-memory command causes the data in the 14 bit memory line accessed to be read into the Data register of the EAROM and from there out to a 14 bit register in the control chip which also doubles as two polynomial counters of 10 and 4 bits.

e) After receiving the information from the data register of the EAROM, the 14 bit register in the control chip becomes a ten bit and a four bit polynomial counter. The 10 bit polynomial counter is used to produce, via a set/reset flip flop, a variable duty cycle square wave (amplitude is V_{DD} to V_{SS}) which is used to generate, via the CMOS DAC, the coarse tuning voltage corresponding to the code in the line of the EAROM that was accessed.

f) The four bit polynomial counter acts similarly to the 10 bit counter, but in a different time frame. It gives a variable duty cycle square wave at a frequency of approximately 67kHz.

g) The coarse and fine tune data is fed from the control chip to the DAC where it is amplified to the level of V_{REF} (tuning voltage reference). The fine tune information is also filtered to a DC level and then inserted at the end of each coarse tune pulse. It is this combined output of the DAC that is filtered by a 5 pole filter network to produce the tuning voltage V_T for the varactor tuners. The output impedance of the filter is approximately 47K ohm and its rise time is about 50 msecs.

Operation of the fine tuning controls (UP or DOWN) on the control chip alters the 4 bit polynomial counter which has carry over to the 10 bit polynomial counter. Therefore use of these controls allows the user to scan through the total tuning voltage range at a speed that is determined by the time constant of the network connected to pin 37 of the control chip. Alteration of the time constant is used to provide coarse tune speed for set up, as well as equalization of the tuning rate (MHz/sec) between VHF and UHF.

The action of the store-fine-tuning command, which may be made manually, or automatically on release of the fine tune button, cause the two polynomial counters to chain together into a 14 bit shift register which then shifts its contents into the data register of the EAROM which is then written into the memory line of the EAROM corresponding to the channel number that is in its address register.

The new tuning data is still retained in the control chip register which returns to its polynomial counter mode and continues operating as previously described.

On power-up, a master reset pulse is generated in the control chip to reset all clocks. The control chip then also addresses lines 99 and then line 98 of the EAROM in sequence causing the information stored in those lines (last channel number viewed) to be put into the display chip register (if last channel viewed option is used) which then starts up the sequence described previously just as if this data came from the control chip keyboard. Read and write times of the EAROM lines are approximately 20 msecs. All times are referenced to the internally generated 1 MHz clock in the control chip.

Channel number information in the display chip register is used to automatically decode the band information which is fed out as logic signals by the 4 band outputs of the display chip. The channel number information is also available (depending on display chip used) in a form suitable for common anode type seven segment displays (units and tens digit information are separate) or for character generator type display in BCD format. Timing waveform outputs and inputs are provided on the display chip for decoding channel number information where appropriate.

B. One digit entry (5 chip option)

The use of the Interface chip for single digit entry for up to 20 favorite channels does not basically modify the operation of the system as described above. This chip interfaces with the keyboard lines on the control chip and the operational sequence is identical to that of a two digit entry from the keyboard except that the two digit information comes from the Interface chip register which is fed the two digit channel number information stored in one of its twenty memory lines (non volatile), which can be accessed by single digit entry as described above.

When the Interface chip is used there is an option available as an alternative to the obtaining the last channel viewed on power-up. This alternative option always returns the system to memory line "one" on the Interface chip on power-up.

ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... +20V to −.3V
Storage Temperature Range ..... −35°C to +85°C
Operating Temperature Range ..... 0°C to +85°C

*Exceeding these ranges could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

T-1002 Standards Conditions (unless otherwise stated)

V_{SS} = Ground
V_{DD} = +12V ±1.2V
T_A = 0°C to +70°C

Characteristic	Min.	Typ.	Max.	Units	Conditions
Supply Voltage, V_{DD}	10.8	12	13.2	V	
Supply Current, I_{DD}	—	15	35	mA	With clock running
Master Clock, f_m	0.7	0.8	0.9	MHz	R = 100K ± 5% to V_{DD}
Fine Tune Clock, f_r	9.7	11.2	12.5	kHz	C = 68, 75, or 82pF ± 10% to V_{SS}
Inputs:					
Logic "1"	8.0	—	V_{DD}	V	
Logic "0"	0.0	—	1.0	V	
Outputs:					
Logic "1"	V_{DD} -2	—	V_{DD}	V	
Logic "0"	0.0	—	0.5	V	
Rise & Fall TIme t_r, t_f	—	—	1	µs	

T-1102 Standard Conditions

V_{SS} = Ground
V_{DD} = +12V ±1.2V
T_A = 0°C to +70°C

Characteristic	Min.	Max.	Units	Conditions
V_{DD}	10.8	13.2	V	
I_{DD}	—	10	mA	With clock running
V_L	V_{SS}	V_{DD}	V	
Quiescent Current	—	10	mA	Clock Frequency = 0Hz
V_{LN} (Logic Low Signal In)	0.0	1.0	V	At all inputs unless otherwise specified.
V_{HN} (Logic High Signal In)	8.0	V_{DD}	V	At all inputs unless otherwise specified.
V_{LO} (Logic Low Signal Out)	0.0	1.0	V	For Pins 8, 9, 10, 11 & 28 into 1MΩ, 20pF load
V_{HO} (Logic High Signal Out)	V_{DD} -2 V_{DD} -3	V_{DD} V_{DD}	V V	For Pins 11, & 28 into 1 MΩ, 20pF load For Pins 8, 9, & 10 into 1 MΩ, 20pF load
Ø1 (Units & Tens Clock)	9.2	16.8	kHz	Pins 1, 5
T_R, T_F	—	550	ns	Pins 1, 4, 5
Ø2	9.2	16.8	kHz	Pin 4.
Duty Cycle Ø1 (Typical)	1/12 of clock Frequency			Pins 1, 5.
Duty Cycle Ø2 (Typical)	1/6 of clock Frequency			Pin 4.
T_{DELAY}	.45	.55	µs	Delay between rise of Ø1 and Ø2 = 1/F
T_R, T_F	—	1	µs	Pins 8 thru 11 and 28 Load = 10pF
R_{OUT}	—	24	kΩ	I_L = 1mA Pins 3,7,38,39
V_O	2.0V	Variations Between These Outputs on any 1 chip to be 1V Max.	V	At I_O Min. = 17mA. Additionally each output shall be capable of sustaining I_O max 25mA pins 13, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 27. For LED display only. In the off condition leakage current at +20V to be no greater than 10µA.
I_O	1.6	—	mA	For indirect display drive — 13, 14, 15, 16, 24 thru 27. Outputs to be compatible to TTL or CMOS without interface. V_O = 0.6V.

ENTER-TAINMENT

1400 Bit Serial Electrically Alterable Read Only Memory

FEATURES

- 100 Word × 14 bit organization
- Word alterable
- 10 years unpowered data storage
- Write/Erase time 20ms/word
- Single −35 volt supply
- No voltage switching required
- MOS compatible signal levels

DESCRIPTION

The ER1400 is a serial input/output 1400 bit electrically erasable and reprogrammable ROM, organized as 100 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus.

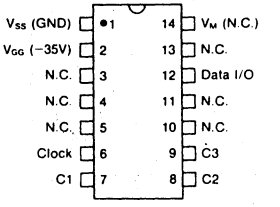
Addressing is by two consecutive one-of-ten codes.

Mode selection is by a 3 bit code applied to C1, C2 and C3.

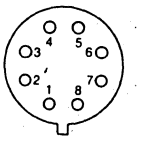
Data is stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 1400 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

PIN CONFIGURATIONS

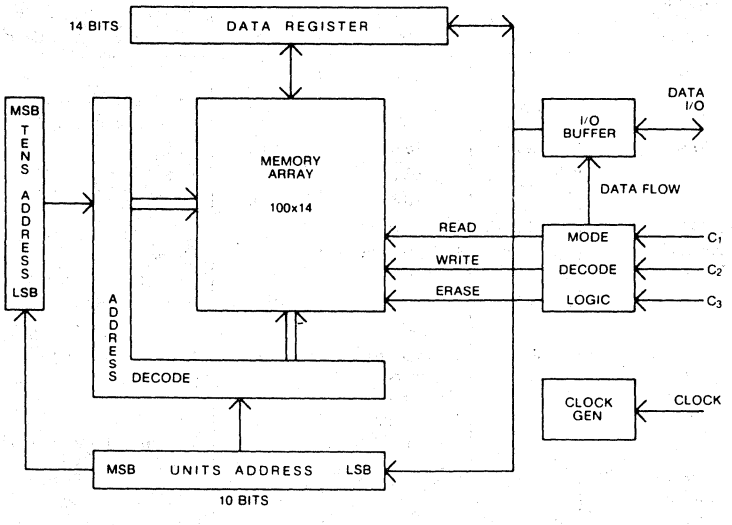
Standard package
14 LEAD DUAL IN LINE



Special Order Package
8 LEAD TO-8 (ER1400T)



BLOCK DIAGRAM



ENTER-TAINMENT

PIN FUNCTIONS

Name	Function
Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respectively. In the Shift Data Out mode this pin is an output pin designed to drive MOS. In Standby, Read, Erase and Write, this pin is left floating.
V_M	Used for testing purposes only. Must be left unconnected for normal operation.
V_{SS}	Chip substrate. Normally connected to ground.
V_{GG}	DC supply. Normally connected to V_{SS} −35 Volt supply.
Clock	Timing reference. Required for all operations. May be left at logic zero when device is in standby.
C1,C2,C3	Mode control pins. Their operation is as follows:

C1	C2	C3	Function
0	0	0	Standby - contents of Address and Data Register remains unchanged. Output buffer is left floating.
0	1	1	Accept Address - Data presented at the I/O pin is shifted into the Address Register with each clock pulse. Addressing is by two consecutive one-of-ten codes.
1	0	0	Read - The address word is read from memory into the data register.
1	0	1	Shift Data Out - The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.
0	1	0	Erase - The word stored at the addressed location is erased to all zeros.
1	1	1	Accept Data - The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.
1	1	0	Write - The word contained in the Data Register is written into the location designated by the Address Register.
0	0	1	Not Used

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
(except V_{GG}) with respect to V_{SS} ..... −20V to +0.3V
V_{GG} with respect to V_{SS} ..... −40V
Storage temperature (No Data Retention) ..... −65°C to +150°C
Storage temperature (with Data Retention)
Operating ..... −25°C to +75°C
Unpowered ..... −65°C to +80°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

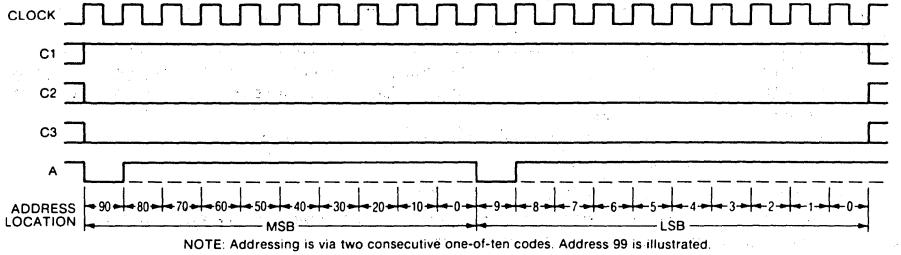
Standard Conditions (unless otherwise noted)
V_{SS} = GND
V_{GG} = −35V ± 8%
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input logic "1"	V_{IL}	V_{SS}−15.0	—	V_{SS}−8.0	V	
Input logic "0"	V_{IH}	V_{SS}−1.0	—	V_{SS}+0.3	V	
Input leakage	I_L	—	—	10	μA	V_{IN} = −15V
Output logic "1"	V_{OL}	—	—	V_{SS}−12.0	V	Load = 1.5MΩ, 100pF
Output logic "0"	V_{OH}	V_{SS}−1.0	—	V_{SS}+0.3	V	I_{SOURCE} = 200μA
Power consumption	P_{GG}	—	—	300	mW	
Power supply current	I_{GG}	—	—	8.0	mA	
AC CHARACTERISTICS						
Clock Frequency	fϕ	10.0	14.0	17.0	kHz	
Clock duty cycle	Dϕ	35	50	65	%	
Write time	tw	10.0	20.0	24.0	ms	
Erase time	te	10.0	20.0	24.0	ms	
Rise, fall time	tr, tf	—	—	1.0	μs	
Control, Data set up time	t_{CS}	1	—	—	μs	
Control, Data hold time	t_{CH}	0	—	—	μs	
Propagation delay	tpw	—	—	20.0	μs	Load = 1MΩ, 100pF
Unpowered non-volatile data storage	T_S	10	—	—	Years	See Note 1.
Number of erase/write cycles	N_W	—	—	10^4	—	Per word. See Note 2.
Number of read accesses between writes	N_{RA}	10^9	—	—	—	Per word

**Typical values are at +25°C and nominal voltages.
NOTE 1: T_S is for powered or unpowered storage.
NOTE 2: N_W (-10^4) is a maximum for data retention times greater than 10 years. beyond 10^4 reprograming cycles, there is a gradual, logarithmic reduction in retention time with 1 year being a typical value after 10^5 cycles.

ENTER-TAINMENT

TIMING DIAGRAMS



NOTE: Addressing is via two consecutive one-of-ten codes. Address 99 is illustrated.

Fig.1 ACCEPT ADDRESS

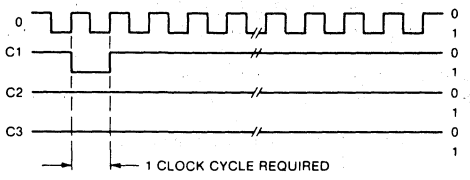
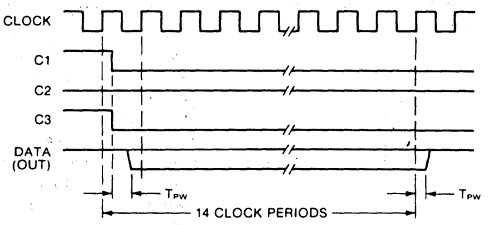


Fig.2 READ



T_{PW} measured initially from control line transition to data out, then measured from the positive clock edges to data changes. Timing measurements are made at V_{SS} 2 and 10 volt points

Fig.3 SHIFT DATA OUT

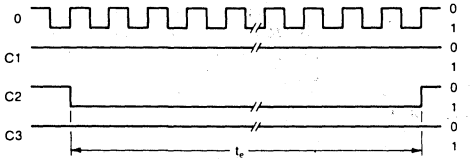


Fig.4 ERASE

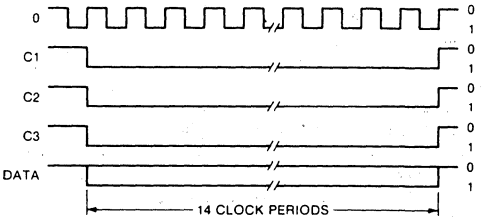


Fig.5 ACCEPT DATA

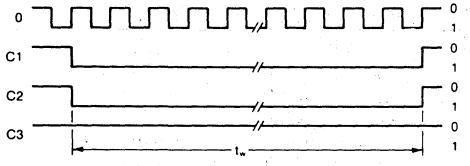


Fig.6 WRITE

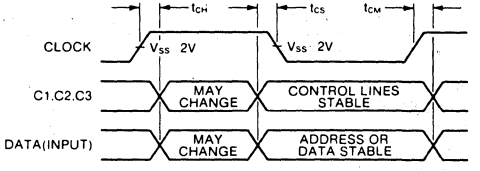


Fig.7 INPUT TIMING

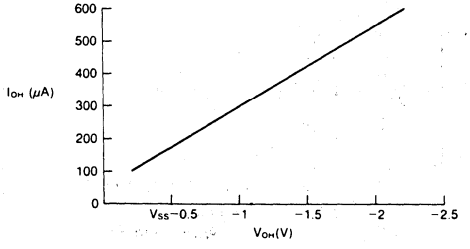


Fig.8 TYPICAL OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

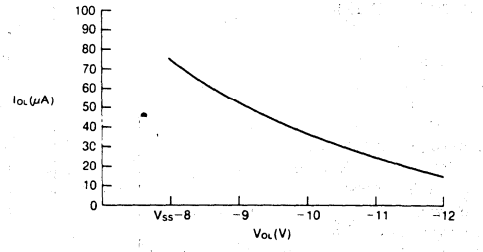


Fig.9 TYPICAL OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

ENTER-TAINMENT

CMOS D/A Converter

FEATURES

- Combined and/or separate Coarse and Fine Tuning
- 30V Tuning Voltage Range
- High Stability
- Low Power Consumption

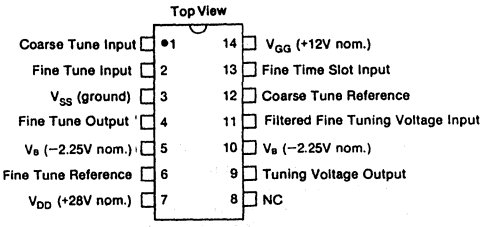
DESCRIPTION

The MEM 4956 is a CMOS D/A Converter designed to operate in conjunction with the General Instrument Omega and Economega Digital Tuning Systems.

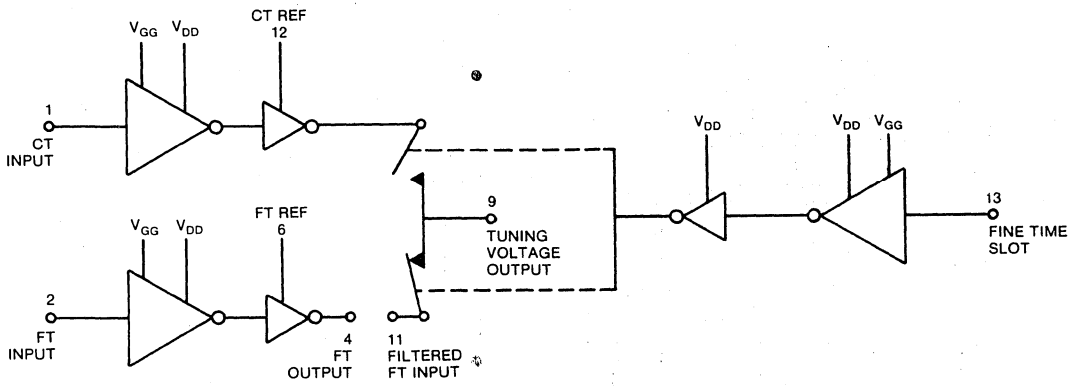
It consists of two level shifting amplifier-drivers with a common output. A control input determines which amplifier is connected to the output.

PIN CONFIGURATION

14 LEAD DUAL IN LINE



BLOCK DIAGRAM



ENTER-TAINMENT

PIN FUNCTIONS

Pin No.	Name	Function
1	Coarse Tune Input	Positive going pulse. The duty cycle determines the Tuning Voltage Output.
2	Fine Tune Input	Positive going pulse. The duty cycle determines the Fine Tuning Voltage Output.
3	V_{SS}	Negative power supply.
4	Fine Tune Output	Amplified version of Fine Tune Input. Switches between Vss and Fine Tune Reference.
5	V_B	−2.25 Bias used to increase breakdown voltage.
6	Fine Tune Reference	Power supply to Fine Tune Buffer Amplifier: 28V nom.
7	V_{DD}	Power supply for Logic: 28V nom. (V_{DD} must be the most positive power supply).
9	Tuning Voltage Output	Combined Coarse and Fine tuning data which after filtering is used to tune the TV.
10	V_B	−2.25 Bias used to increase breakdown voltage.
11	Filtered Fine Tuning Voltage Input	The Filtered Fine Tuning Voltage connected to this input is combined with the Coarse Tuning Data by the action of the Fine Time Slot input.
12	Coarse Tune Reference	Power supply to Coarse Tune Buffer Amplifier: 28V nom.
13	Fine Time Slot Input	When at logic '0' the Coarse Tuning information is connected to the Tuning Voltage Output. When at logic '1' the Fine Tuning information is connected.
14	V_{GG}	+12V reference for input level shifting circuit.

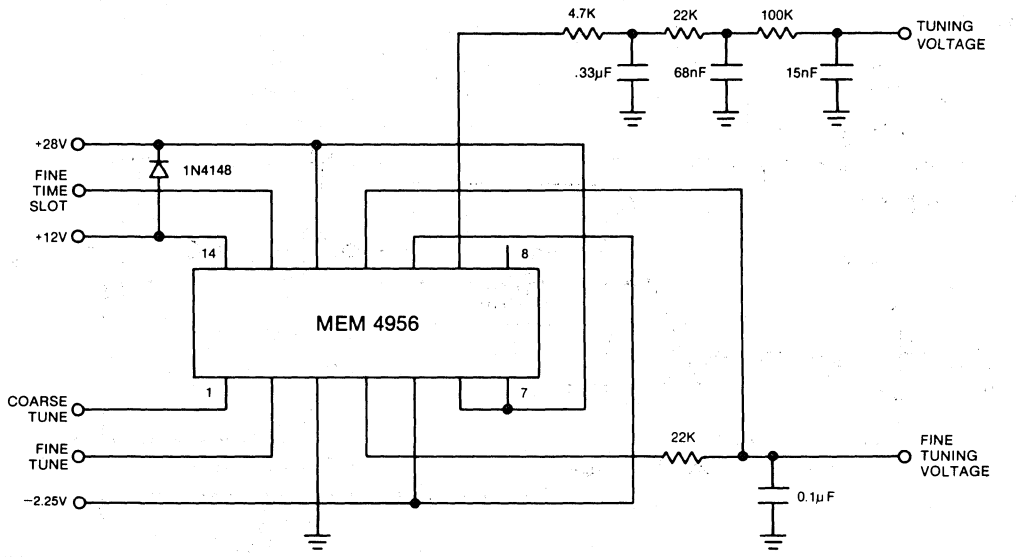
STANDBY

The −2.25 V_B supply may be reduced to 0V during standby provided that V_{DD}, V_{REF1} and V_{REF2} are reduced to +12V (V_{GG}). The V_B pins must not be open circuited.

BIAS SUPPLY

The −2.25 V_B supply must have a source impedance of 2.2K or less and be decoupled to V_{SS} by a 10nF ceramic capacitor.

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

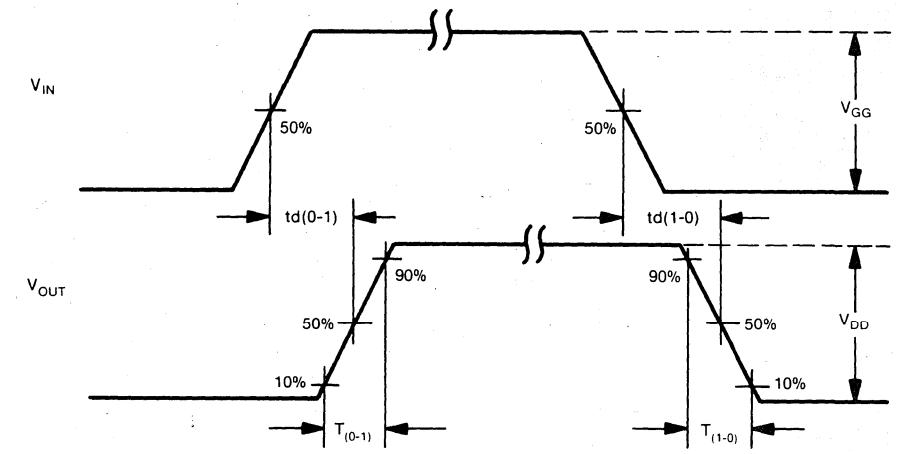
Voltage of any pin with respect to V_{SS} pin 3 (except V_{REF1}, V_{REF2}, V_{DD} and V_B) ..... -0.3 to +20V
Voltage on V_{REF1}, V_{REF2}, V_{DD} with respect to V_{SS} pin ..... V_{GG} to +36V
Voltage on V_B with respect to V_{SS} pin ..... -4 to +0.3V
Storage Temperature Range ..... -40°C to +100°C
Ambient Operating Temperature Range ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)
V_{SS} = 0V
V_{GG} = +12V ± 10%
V_{DD} = V_{REF1} = V_{REF2} = +28 to +30V
V_B = −2.25V ± 10%
T_A = +25°C

Characteristic	Min.	Typ.	Max.	Units	Conditions
Input					
Logic '0'	-0.2	—	+0.3	Volts	
Logic '1'	10	—	V_{GG}	Volts	
Fine Tune Output on Resistance					
Logic '0'	—	70	200	Ω	
Logic '1'	—	100	300	Ω	
Tuning Voltage Output on Resistance					
Logic '0'	—	200	500	Ω	Pin 4 connected to Pin 11
Logic '1'	—	300	700	Ω	R1 = 10K
Output Propagation Delay					
Logic '0' to Logic '1'	—	90	—	ns	} C1 = 100pF
Logic '1' to Logic '0'	—	80	—	ns	
Output Switching Time					
Logic '0' to Logic '1'	—	80	—	ns	} C1 = 100pF
Logic '1' to Logic '0'	—	70	—	ns	
Supply Current					
V_{GG},	—	75	—	μA	V_{DD} = V_{REF1} = V_{REF2} = +28V
V_B	—	75	—	μA	V_{GG} = +12V
V_{DD}, V_{REF1}, V_{REF2} (Total)	—	1.2	—	mA	V_B = −2.25V

TIMING DIAGRAM



ENTER-TAINMENT

ECONOMEGA / 16 Channel Digital Tuning System

FEATURES

- 8/12/16 Programs
- 3/4 Bands
- 10 bit Coarse-Tune
- 4 bit Fine-Tune
- Non-Volatile Memory without battery
- Auto or Manual Tuning
- Auto or Manual Band switching

DESCRIPTION

The ECONOMEGA Digital Tuning system is a three chip voltage synthesizer. The first chip (AY-5-8203) is an n-channel control chip which interfaces the remote control system, memory and D/A converter. The second chip (ER1400) is a non-volatile EAROM memory which stores the tuning and band information for 16 programs. The third chip is a CMOS Buffer amplifier/switch. This amplifies the converter output from the control chip to a fixed reference voltage and also contains the switch circuitry for the fine time slot. For details on the MEM 4956 D/A converter circuit and the ER1400 EAROM, refer to the separate data sheet in this section.

NOTE: 10 bits of coarse time and 4 bits of fine tune does not mean the resolution is 14 bits (described later). The overall resolution is:

Band 3 — 11 bits

Bands 1, 2, & 4 — 10 bits

PIN CONFIGURATION

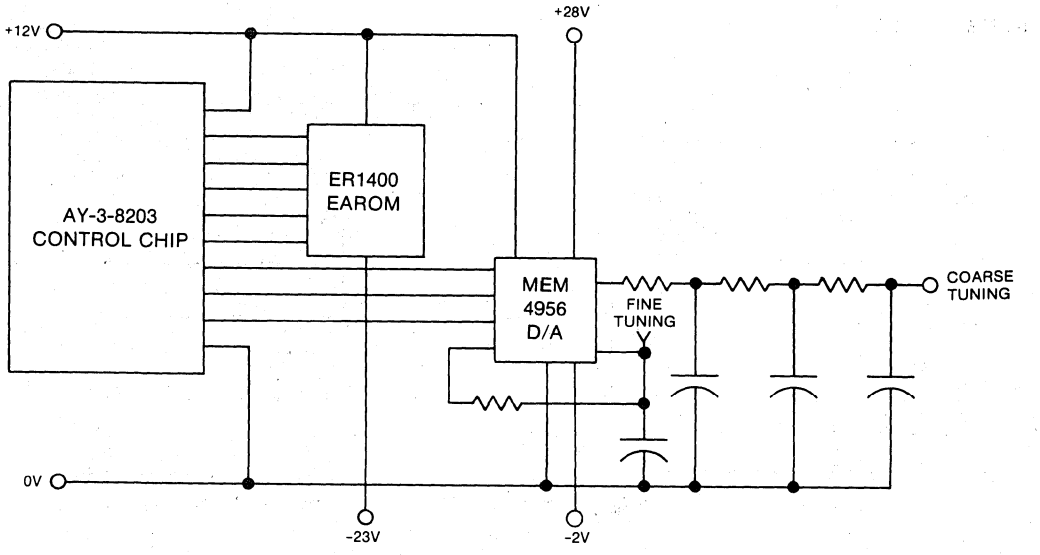
40 LEAD DUAL IN LINE

AY-3-8203

Top View

V_{SS} (neg. supply)	1	40	V_{CC} (pos. supply)
Data I/O	2	39	Band 1 Output
C3	3	38	Band 2 Output
C2	4	37	Band 3 Output
C1	5	36	Band 4 Output
Clock	6	35	Course Tune Output
Start Input/Band 1 Input	7	34	Fine Time Slot Input/Output
3/4 Band Select Input/Band 2 Input	8	33	Fine Tune Output
Auto Band-Switching Select — Band 3 Input	9	32	Audio Visual Output
Auto Band-Switching Select — Band 4 Input	10	31	Muting Output
Tuning Clock	11	30	Constant Time Scan Input
Fine Tune Up Input	12	29	Auto Stop Input
Fine Tune Down Input	13	28	Validate Input
System Clock	14	27	Remote Start and Store Input
Program Read Input	15	26	Store Input
Program Up Input	16	25	2^3 Input/Output
Program Down Input	17	24	2^2 Input/Output
Load Input	18	23	2^1 Input/Output
Input/Output Select	19	22	2^0 Input/Output
8/12/16 Program Select Input	20	21	Serial Remote Input

SYSTEM BLOCK DIAGRAM



ENTER-TAINMENT

PIN FUNCTIONS

Pin No.	Name	Function
1	V_{SS}	Ground
2	Data I/O	To ER1400 EAROM
3	C3	To ER1400 EAROM
4	C2	To ER1400 EAROM
5	C1	To ER1400 EAROM
6	15.6kHz	Control Chip Clock +128
7	Band 1 Input (Start Input)	When connected to V_{SS} selects Band 1 and initiates scan. (Connect to V_{SS} to start scan).
8	Band 2 Input (3/4 Band Select Input)	When connected to V_{SS} selects Band 2 and initiates scan. (Connect to V_{SS} for Bands 1, 2, 3. Leave open for Bands 1, 2, 3, 4).
9	Band 3 Input } Auto Bandswitch Select Input	When connected to V_{SS} selects Band 3 and initiates scan. } Connect to V_{SS} for Auto Bandswitching.
10	Band 4 Input } Auto Bandswitch Select Input	When connected to V_{SS} selects Band 4 and initiates scan. } Connect to V_{SS} for Auto Bandswitching.
11	Tuning Clock	Controls speed of coarse and fine tuning, set by external R-C network. 1.28kHz nominal. Runs only while scanning.
12	Fine Tune Up Input	When connected to V_{SS} causes FT to increment automatically.
13	Fine Tune Down Input	When connected to V_{SS} causes FT to decrement automatically.
14	System Clock	System clock 2.0MHz nominal set by external R-C network.
15	Program Read Input	When connected to V_{SS} reads EAROM (includes 20ms antibounce delay).
16	Program Up Input	When connected to V_{SS} increments program number by 1. There is a 20msec antibounce delay on this input.
17	Program Down Input	When connected to V_{SS} decrements program number by 1. There is a 20msec antibounce delay on this input.
18	Load Input	When connected to V_{SS} new data is loaded into program number register from the program number inputs and the EAROM data is read. When left open the program number inputs are inhibited.
19	Input/Output Select	When connected to V_{SS} selects input mode for 2^0, 2^1, 2^2, 2^3 pins.
20	8/12/16 Program Select Input	Fixes the number of programs that can be selected using the Program UP and DOWN inputs. Open circuit =12, V_{SS}=16, V_{CC}=8.
21	Serial Remote Input	Accepts a train of 0.5 msec negative pulses, the number of pulses determines the program number to be selected.
22	2^0 Input/Output	Binary program number input/output. When used as an input accepts data in positive logic convention. (0000 = prog. 1). When used as an output the data is static and in positive logic convention. These outputs are TTL compatible.
23	2^1 Input/Output	Binary program number input/output. When used as an input accepts data in positive logic convention. (0000 = prog. 1). When used as an output the data is static and in positive logic convention. These outputs are TTL compatible.
24	2^2 Input/Output	Binary program number input/output. When used as an input accepts data in positive logic convention. (0000 = prog. 1). When used as an output the data is static and in positive logic convention. These outputs are TTL compatible.
25	2^3 Input/Output	Binary program number input/output. When used as an input accepts data in positive logic convention. (0000 = prog. 1). When used as an output the data is static and in positive logic convention. These outputs are TTL compatible.
26	Store Input	When connected to V_{SS} stores Tuning and Band information in EAROM.
27	Remote Start and Store Input	A short positive pulse (<1 msec) initiates scanning. A long positive pulse (>3 msec) stores the tuning and band information in the EAROM.
28	Validate Input	Confirms valid stop command. Positive for a valid TV signal.
29	Auto Stop Input	Initiates Autostop sequence on a positive going edge (except in constant time scan mode when a negative edge is used).
30	Constant Time Scan Input	When connected to V_{SS} a constant scan rate of 8 sec per Band is selected. In addition on Band 3 stop is executed on a negative edge rather than a positive edge and the Muting output is active low with the same output specification as Band.
31	Muting Output	Active high during scan and program change (active low in constant time scan mode and Auto Band Switching mode).
32	Audio Visual Output	Goes to logic '0' when the last program is selected (8, 12 or 16) and is on Band 3.
33	Fine Tune Output	Fine Tuning Information, 4 bits resolution.
34	Fine Time Slot Input/Output	Used by MEM 4956 CMOS D/A to combine Coarse and Fine data when separate FT is not required. Connect to V_{SS} when MEM 4956 is not used to invert CT and FT Outputs. The Fine Tune slot is a 2 µsec pulse repeated every 250 µsec on Band 3, a 10 µsec pulse on Bands 2 and 4 and a 30 µsec pulse on Band 1.
35	Coarse Tune Output	Coarse Tuning Information, 10 bits resolution.
36	Band 4 Output	This output goes to logic '0' when Band 4 is selected.
37	Band 3 Output	This output goes to logic '0' when Band 3 is selected.
38	Band 2 Output	This output goes to logic '0' when Band 2 is selected.
39	Band 1 Output	This output goes to logic '0' when Band 1 is selected.
40	V_{CC}	Positive power supply, +12V ± 10%.

ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin .....−0.3V to +20 Volts
Storage Temperature Range ..... −65°C to +150°C
Ambient Operating Temperature Range..... 0°C to +70°C
Package Thermal Resistance .....63°C/Watt

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{CC} = +12V ± 10%
System Clock = 1.44 to 2.15MHz (2.0MHz nominal)

Parameter	Min	Typ**	Max	Units	Conditions
Control Inputs					
Logic '0' Level	—	—	1.0	Volts	
Logic '1' Level	8	—	V_{CC}	Volts	
Resistance	200	400	1200	kΩ	to V_{CC}
Program No Inputs					
Logic '0' Level	—	—	0.5	Volts	
Logic '1' Level	8	—	—	Volts	
Resistance	100	200	600	kΩ	to V_{CC}
8/12/16 Input					
Logic '0' Level	—	—	0.5	Volts	
Logic 0/1 Level	—	open	—		
Logic '1' Level	10	—	—	Volts	
Input Resistance	30	100	300	kΩ	
Band, AV, Outputs					
Logic '0' Level	—	—	2	Volts	I_{sink} = 5mA
Off Leakage	—	—	10	μA	V_{out} = V_{CC}
Muting Output					
Logic '1' Level	6	—	—	Volts	Isource = 2mA
Off Leakage	—	—	10	μA	Note 1.
Program Outputs					
Logic '0' Level	—	—	0.4	Volts	Isink = 1.6mA
Logic '1' Level	8	—	—	Volts	Isource = 10μA
Supply Current					
V_{CC} (+12)	—	51.8	—	mA	at +25°C
	—	—	60	mA	at 13V and +70°C

**Typical values are at +25°C and nominal voltages.
NOTE: 1. In the constant time scan mode, the Muting Output has the same specification as the Band and AV outputs.

ENTER-TAINMENT

OPERATION

1. Coarse Tune
The coarse tune resolution is 10 bits with a predominant output ripple at 3.9kHz.

2. Fine Tune
The fine tune resolution is 4 bits with an output ripple at 15.6kHz. The fine tune steps twice per second related to system clock; it does not wrap around or overflow into coarse tune. During scanning it is reset to mid range.

3. Scanning
The actual tuning rates are fixed by the Tuning Clock and may be adjusted over wide limits. Typical figures are shown below.

(a) Normal Mode

Operation of a band button initiates scanning on the selected band, typical scan rates are as follows:

Band	Scan Time
1	0.8 sec.
2	1.6 sec.
3	8.0 sec.
4	1.6 sec.

(b) Constant Time Scan Mode

Operation of a band button initiates scanning on the selected band. The scan rate is a constant 8 seconds for each band.

(c) Auto Band Switching Mode

At the end of each scan the band is automatically changed in the sequence 1, 2, 3, 4. In the 3 band mode, band 4 is omitted.

4. Auto Stop and Validate
In the Normal Mode a stop is executed immediately on a positive going input transition. If validate goes positive within 256 msec the system stops, if not the scan will restart (See Fig. 1 for a suggested validate circuit).

At the end of a band the tuning voltage goes back to zero and after a delay of 256 msec scanning restarts. In the Constant Time Scan mode in Band 3, the stop is executed on a negative going transition.

5. Manual Operation
In the Normal Mode Stop and Validate can be linked to the Band Inputs to give full manual control of the tuning operation.

6. Muting
The Muting output is active from the time that a Scan is initiated until the Validate input goes positive after a Stop command. When a program change is made the Muting output is activated for 256 msec.

7. Tuning Procedure

(a) 1. Select required program number (1 to 16).
2. Press required band button, scanning commences from the station currently tuned, scanning stops at the next station.
3. Fine tune if required.
4. Store Data.

(b) Alternatively using the circuitry shown in Fig. 2, the following procedure is available:
1. Press Band or Start.
2. Press Store.
3. Press required program.

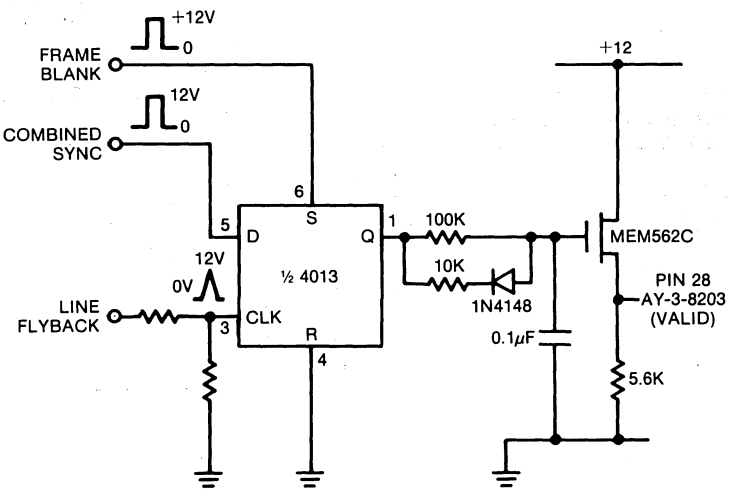


Fig.1 "VALID" CIRCUIT

ENTER-TAINMENT

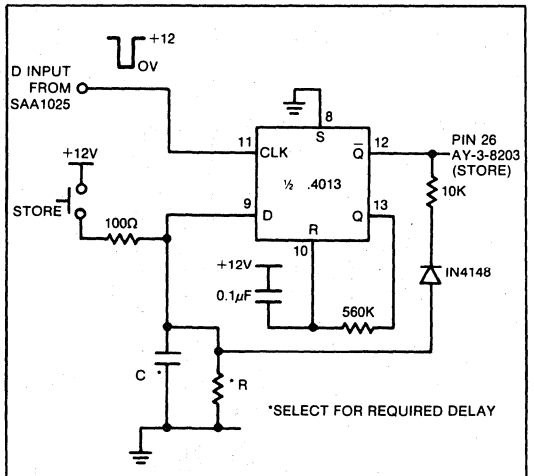


Fig.2 "DELAYED STORE" CIRCUIT

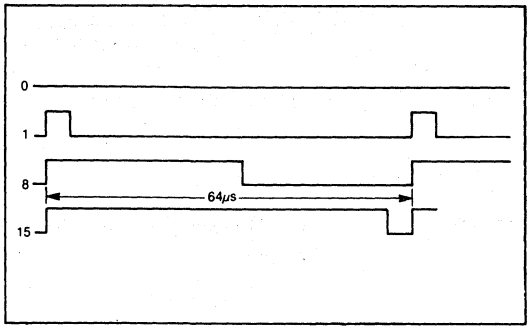
8. Fine Tune Resolution

When the MEM4956 D/A is used to combine the Coarse and Fine Data the relationship between Coarse Tune and Fine Tune is as follows:

Band 1	1 FT step = 7.5 CT steps
Band 2, 4	1 FT step = 2.5 CT steps
Band 3	1 FT step = 0.5 CT steps

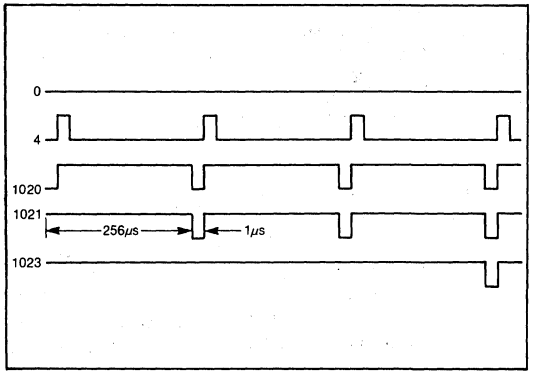
9. Additional Fine Tune Information

The fine tune output is a rectangular waveform with a frequency of 15.6kHz (system clock +128). The mark/space ratio defines the fine tune level, 16 steps being possible. The following diagram relates the binary number within the fine tune store to the output waveform. Bit width is approximately 3.8μs for a 15.6kHz output waveform.



10. Additional Coarse Tune Information

The Coarse tune output is a rectangular waveform with a predominant ripple frequency of 3.9kHz (system clock +512). The mark/space ratio indicates the coarse tune level. The addition of a coarse tune bit increases the mark period by approx. 1.0μs for a 2.0MHz clock. There are thus 256 bits within the 3.9kHz period. This accounts for 8 of the 10 coarse tune bits. The information from the remaining 2 bits (LS Bits) is used to add 0, 1, 2, or 3 extra bit periods (1.0μs) over 4 periods of the basic waveform. The complete coarse tune waveform repeats every 1ms.

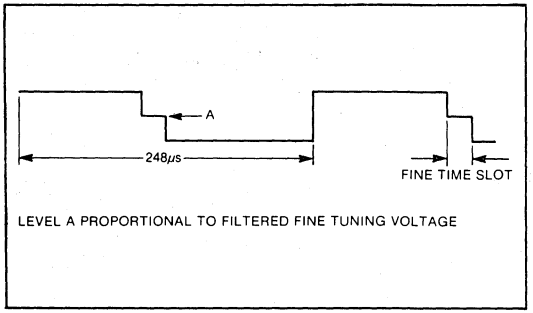


11. MEM 4956 Buffer

This buffer combines coarse and fine data under the control of the Fine Time slot output from the control chip.

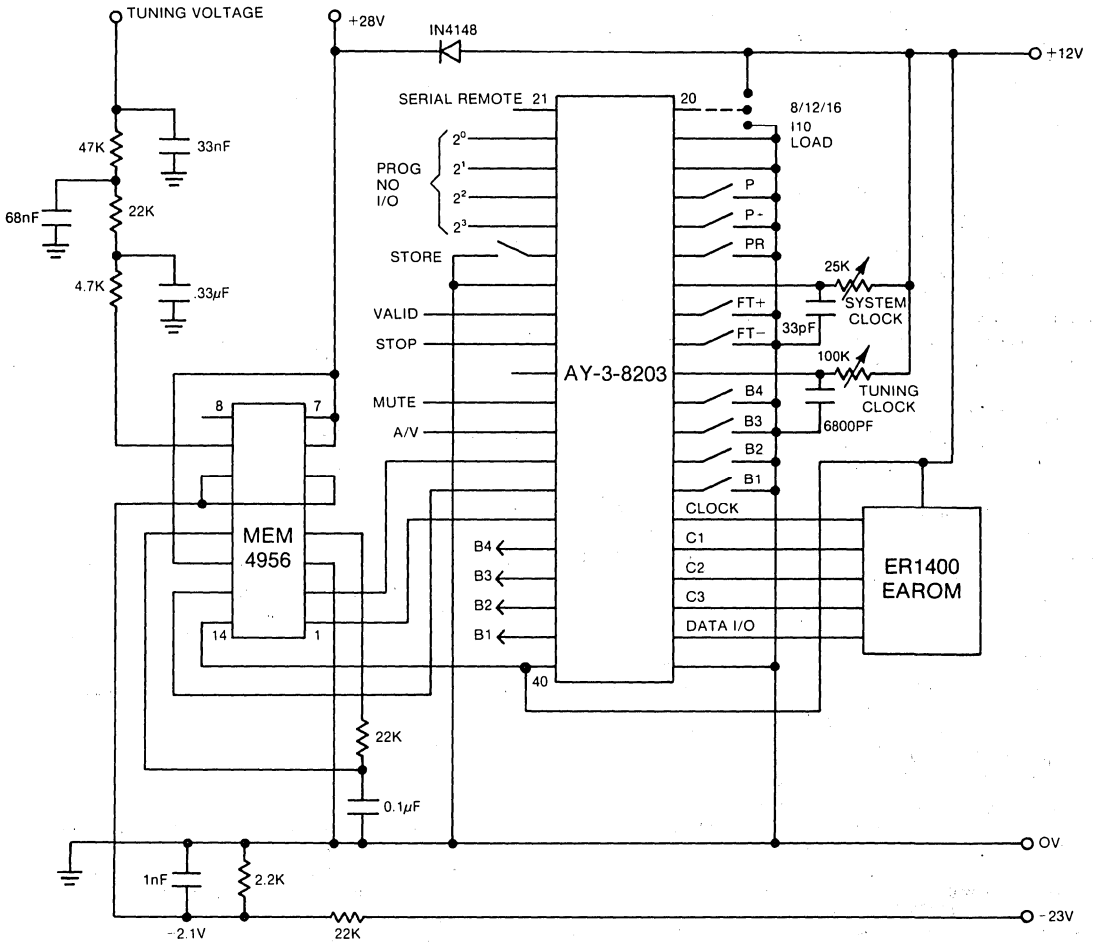
The fine time slot controls the CMOS switch and hence the times the coarse tune or fine tune information are routed to the output filter. Note the fine tune waveform is filtered before being routed to the switch.

A typical output waveform of pin 9 of the device is shown below.



ENTER-TAINMENT

SYSTEM DIAGRAM



ECONOMEGA IIA Digital Tuning System

FEATURES

- 16/32 Program Options
- 4 Bands
- 14 Bit Tuning Resolution on B3
- Program Copying
- Non-Volatile Memory without Battery
- Manual Up/Down tuning
- Manual Band Switching
- Mute output at program selection
- Search active output
- Local program Up/Down Control
- Validate circuitry
- Referenced tuning waveform output
- Band step option 3/4 select

DESCRIPTION

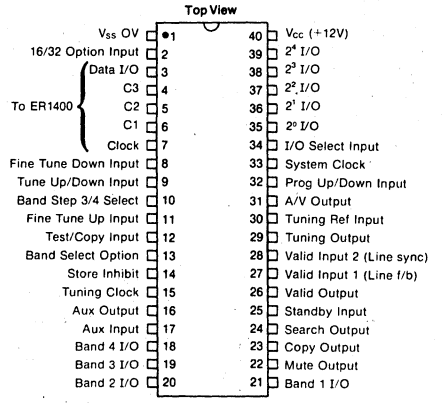
The Economega IIA Digital Tuning system is a voltage synthesizer for both Radio and TV manual tuning applications.

The AY-3-8211 N-Channel control chip interfaces directly with an ER1400 non-volatile memory enabling storage of up to 32 programs.

Variable mark space ratio tuning information from the AY-3-8211 is amplified and filtered, and the resulting DC level used to control the TV or Radio tuner.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



OPERATION

Tuning—Resolutions are as follows:

	Option 1	Option 2
B1 (Band 1)	11 bits (16mV)	12 bits (8mV)
B2 (Band III), B4	12 bits (8mV)	13 bits (4mV)
B3 (UHF)	14 bits (2mV)	14 bits (2mV)

These are the tuning information incrementing resolutions controlled by the Tune Up/Down, Band Inputs, and Fine Tune inputs. Voltages relate to approximately 30 volt tuning range.

Fine Tune—The Fine Tune steps approximately 8 times per second (related to system clock). The Fine Tune input is disabled when searching (Band inputs pressed or Tune Up/Down active) and when Mute is active. Tuning resolutions as above 'Tuning.'

Scanning—The actual tuning rates, fixed by the Tuning Clock, may be adjusted over a wide limit, typical figures are quoted below.

Operation of a Band Input or Tune Up/Down initiates scanning on the selected band, and the Search O/P goes low.

Typical Scan rates are as follows:

	Scan Time	
Band	Option 1	Option 2
1	1.25 sec	2.5 sec
2, 4	2.5 sec	5 sec
3	10 sec	10 sec

This corresponds to a Tuning Clock of approximately 1.6kHz.

When the Tuning Output overflows, scanning pauses for 256ms to allow time for the tuning voltage to settle and, if in the Band Step Mode, also the Band outputs.

This pause occurs at the bottom of the tuning range when tuning up and at the top of the tuning range when tuning down.

Muting—When a program change is made and at 'Power on' and 'Standby to OFF', the mute output is activated for 256 msecs and diables the Fine Tune Inputs for this time, Mute O/P is also active while scanning i.e. when a Band I/P or Tune Up/Down I/P is active.

Tuning Procedure—Three tuning procedures are available:

(a) 1. Select required program number (1 to 16 or 32).
2. Press required band button, scanning commences from the station currently tuned, scanning stops immediately on release of button.
3. Fine tune if required.
4. Tuning information is stored automatically on release of band button or release of Fine Tune button.
5. The tuning information may be copied by pressing Copy and selecting a new program number.

(b) With Tuning Option selected.
1. Select Band—this is latched on.
2. Tune Up or Down using Tune Up/Down Input.
3. Fine Tune if required.
4. Tuning information is stored automatically on release of Tune Up/Down or release of Fine Tune Up/Down.
5. A program location is selected by first pressing Copy and then selecting the required Program number.

(c) With Band Step 3 or 4 selected and Tuning Option Selected.
1. Select band—this is latched on.
2. Tune Up or Down.
3. Tuning will now follow from band to band.
4. Once a station is tuned release Tune Up/Down and Fine Tune if required.
5. Tuning information is stored automatically on release of Tune Up/Down or release of Fine Tune Up/Down.
6. A Program location is selected by first pressing copy and then selecting required program number.

Output Signals—Tuning voltage and Band outputs are not disturbed by internal sequences, for example STORE and COPY. Only program change will disturb these outputs — program change being either a change of band and/or tuning information.

ENTER-TAINMENT

Memory Recall—The memory recall sequence is triggered by a program change and after the 256 millisecond Power On reset. The sequence is as follows:

a) 20 millisecond antibounce delay on the I/O Select or Program inputs.

b) Mute and Fine Tune input inhibit triggered for 256 milliseconds and a memory read initiated.

c) Approximately 12 milliseconds after the inititiation of memory read the new tuning and band information will be output.

d) The rest of the 256 milliseconds period allows time for the band drives and tuning voltage to settle.

Power On—At power on (Vcc on) a 256 millisecond reset allows the power supplies to settle. Mute is active for this period and all inputs are inhibited. At the end of this 256 millisecond period a memory recall sequence is triggered.

3 recall modes now possible:

a) I/O select low i.e. input mode—in this case band and tuning voltage information will be output for the program number input.

b) I/O select high output mode—program 1 together with associated band and tuning voltage information will be output.

c) I/O select open circuit—program 1 band and tuning information will be output. If now, I/O Select goes high, then program 1 will be output on the Program I/O lines.

Standby—When leaving standby Mute is activated for 256 milliseconds, and all inputs are inhibited. A memory recall sequence now follows this delay period. See section 8 for memory recall sequence. Note that the memory recall sequence occurs irrespective of whether there is a program 'change' or not. 3 'Standby off' modes are possible:

a) I/O Select in either output mode or open circuit. Progam information will be as it was prior to Standby being entered.

b) I/O Select in input mode and program remains unchanged. Once again, program information will be as it was prior to entering stand-by mode.

c) I/O Select in input mode and program has changed. The new program information will be output during the memory recall sequence. (Section 8).

Tuning Output Waveform—The tuning output is a rectangular waveform of variable mark space ratio. This output is filtered to produce the tuning voltage. The mark space ratio and hence tuning voltage can be varied, up to a maximum resolution on Band 3, of 14 bits. See earlier "1. Tuning" for the resolutions on other bands.

Seven fundamental frequency components can be present in the output waveform, depending on 'tuning position.' The following table lists these frequencies together with their maximum effective mark space ratios. The condition for which all these 7 components make up the output waveform, would result in a condition of maximum ripple at the output of the tuning filter. The worse case tuning voltage ripple can therefore be determined.

Frequency	Mark/Space Ratio
4kHz	1:1
2kHz	1:511
1kHz	1:1023
500 Hz	1:2047
250 Hz	1:4095
125 Hz	1:8191
62.5 Hz	1:16383

Fig. 1 FUNDAMENTAL TUNING WAVEFORM COMPONENTS

Program change timing with I/O Select in input mode (low)

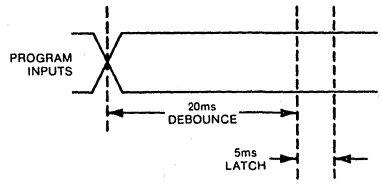


Fig. 2 PROGRAM STROBE TIMING

Any program input change is detected, and after a 20 millisecond antibounce period the program lines are latched in and the corresponding tuning information output. The program lines must be stable for the 5 millisecond 'latch' time shown above.

Latched Program information using I/O Select feature

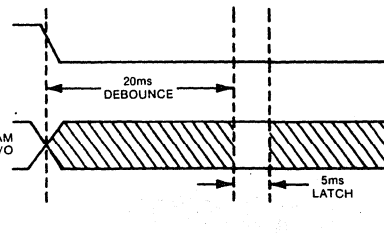
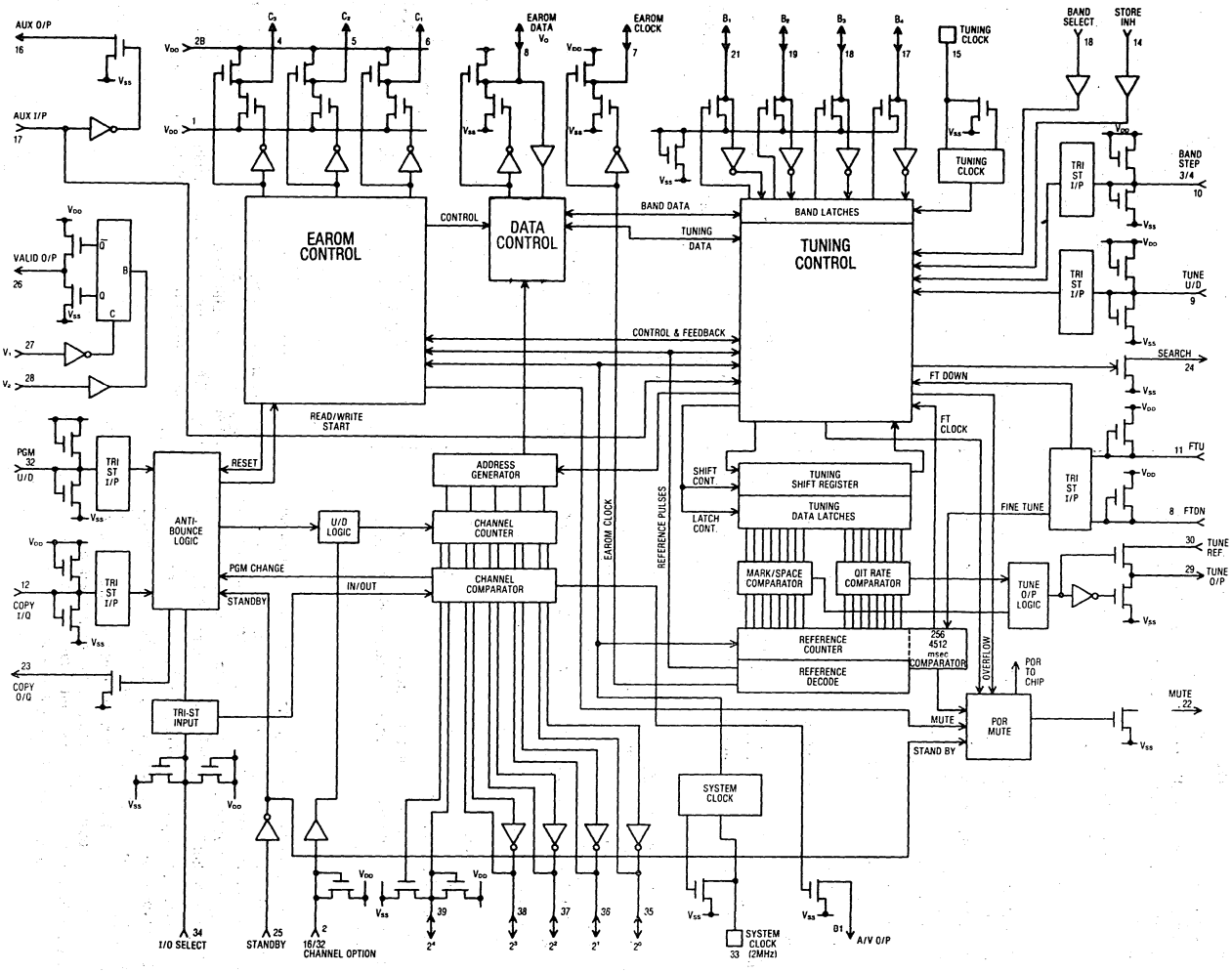


Fig. 3 LATCHED PROGRAM TIMING

I/O Select to low converts the program lines to input mode and triggers a 20mS antibounce period. The program lines are then latched into the chip and the corresponding tuning information output. The program data must be stable for the 5mS 'latch' period. I/O Select to high converts the program lines back to the output mode.

ENTERTAINMENT


AUX O/P
16
AUX I/P
17
EAROM CONTROL
DATA CONTROL
CONTROL
BAND DATA
TUNING DATA
BAND LATCHES
TUNING CONTROL
TUNING CLOCK
BAND SELECT
STORE INH
BAND STEP 3/4
TUNE U/D
SEARCH
FT DOWN
FT CLOCK
FTU
FTON
FINE TUNE
TUNE REF.
TUNE O/P
TUNE O/P LOGIC
VALID O/P
26
CONTROL & FEEDBACK
READ/WRITE START
PGM U/D
32
RESET
ANTI-BOUNCE LOGIC
U/D LOGIC
ADDRESS GENERATOR
CHANNEL COUNTER
CHANNEL COMPARATOR
PGM CHANGE
IN/OUT
STANDBY
COPY I/Q
12
COPY O/Q
23
TRI-ST INPUT
SHIFT CONT.
LATCH CONT.
TUNING SHIFT REGISTER
TUNING DATA LATCHES
EAROM CLOCK
REFERENCE PULSES
MARK/SPACE COMPARATOR
BIT RATE COMPARATOR
REFERENCE COUNTER
REFERENCE DECODE
256 4512 msec COMPARATOR
OVERFLOW
POR TO CHIP
POR MUTE
MUTE
22
STAND BY
SYSTEM CLOCK
SYSTEM CLOCK (2MHz)
33
I/O SELECT
34
STANDBY
25
16/32 CHANNEL OPTION
A/V O/P
31

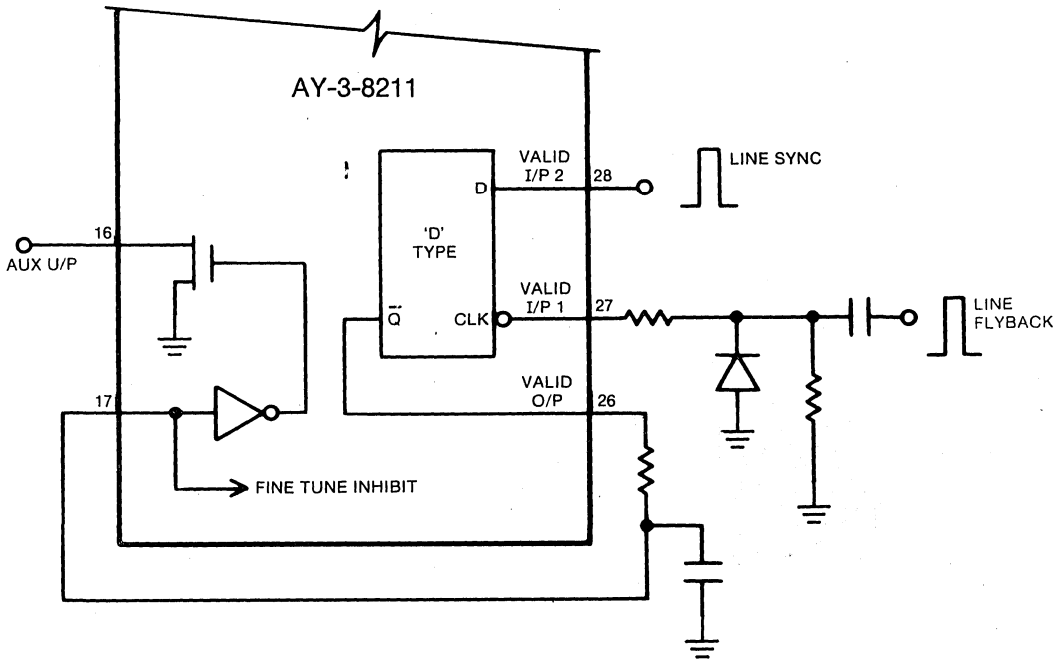


Fig. 4 SUGGESTED VALID SCHEME

For TV Applications the presence of a TV carrier can be determined and the output used to control auxiliary function, for example scanning speed and AFC.

Line sync information in the form of composite sync is sampled by line flyback with the 'D' type flip flop. The output is filtered to produce a 'valid' signal.

For a valid signal, line flyback (27) going low, clocks in line sync (28) high, and Q, Valid Output (26), goes low.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... −0.3V to +20 Volts
Ambient operating temperature range ..... 0°C to +70°C
Storage temperature range ..... −65°C to +150°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

Temperature 0°C to +70°C
V_{SS} = 0V
V_{CC} = +12V ±10%
System Clock = 1.44 to 2.15MHz (2.048 MHz) Nominal (10.8 to 13.2 Volts)

Characteristic	Min	Typ	Max	Units	Conditions
Option (2, 13), Fine Tune Up (11), Fine Tune Down (8) Inputs					
Low Level	V_{SS}	—	3.0	V	
High Level	V_{CC}-3	—	V_{CC}	V	
Pull Up to V_{CC}					
Low Level Source	—	—	0.5	mA	$V_{IN} = V_{SS}$
High Level	V_{CC}-3	—	—	V	$I_{SOURCE} = 10\mu A$
Standby (25) Auxiliary (17) Inputs					
Low Level	V_{SS}	—	3.0	V	
High Level	V_{CC}-3	—	13.2	V	
Input Leakage to V_{SS}	—	—	10	μA	V_{IN} = 13.2 Volts
Store Inhibit (14), Test/Copy (12) Tune Up/Down(9),Band Step 3/4 Select (10), Program Up/Down (32), I/O Select (34) Inputs					
Low Level	V_{SS}	—	1.0	V	
'Open Circuit' Level	3	—	5	V	
High Level	V_{CC}-3	—	V_{CC}	V	
Pull up to V_{CC} (Note 3)					
Low Level Source	—	—	0.5	mA	$V_{IN} = V_{SS}$
Open Circuit' Level	3	—	—	V	I_{SOURCE} 10μA
Pull down to V_{SS} (Note 3)					
High Level Sink	—	—	0.5	mA	$V_{IN} = V_{CC}$
'Open Circuit' Level	—	—	5	V	I_{SINK} 10μA
Band Input/Output (18 to 21)					
Output Low Level	3	—	5	V	I_{SINK} 5mA
Off Leakage to V_{SS}	—	—	10	μA	$V_{OUT} = V_{CC}$
Input Low Level	V_{SS}	—	1.0	V	
Input High Level	3	—	V_{CC}	V	
Copy (23), Mute (22), Search (24), Auxiliary (16), A/V (31) Outputs					Open Drain
Low Level	—	—	1	V	I_{SINK} max 10mA
Off Leakage to V_{SS}	—	—	10	μA	$V_{OUT} = V_{CC}$
Program I/O (35 to 39)					
Input Low Level	V_{SS}	—	3.0	V	
Input High Level	V_{CC}-3	—	V_{CC}	V	
Input Pull Up to V_{CC}					
Low Level source	—	—	0.5	mA	$V_{IN} = V_{SS}$
High Level	V_{CC}-3	—	—	V	I_{SOURCE} =10μA
Output Low Level	—	—	0.4	V	I_{SINK} = 1.6mA
Output High Level	As above Pull Up High Level				
Control, Data + Clock Outputs to ER1400 (4, 5, 6, 3 +7)					
Low Level	—	—	1.0	V	I_{SINK} 20μA
High Level	V_{CC}-0.5	—	—	V	I_{SOURCE} 20μA
Rise time, fall time (Note 2)	—	—	1	μs	C = 30pF
Clock to ER1400 (7)	11.25	16.0	16.79	kHz	System Clock ÷ 128
(50% Duty Cycle)					
Data Input from ER1400 (3)					
Low Level	*	—	3	V	*Note 4
High Level	V_{CC}-3	—	V_{CC}	V	
Input Leakage to V_{SS}	—	—	10	μA	$V_{IN} = V_{CC}$
Input Leakage from V_{CC}	—	—	8	μA	V_{IN} = 3 Volts

ENTER-TAINMENT

Characteristic	Min	Typ	Max	Units	Conditions
Tuning Clock (15)					
External resistor to V_{CC}	47	—	1000	KΩ	
External capacitor to V_{SS}	1.0	—	220	nF	
Leakage to V_{SS} (Tuning Clock OFF)	—	—	1	μA	$V_{IN} = V_{CC}$
System Clock (33)					
External Resistor to V_{CC}	2	—	330	KΩ	
External capacitor to V_{SS}	10	—	100	pF	Normally adjusted to give 16.0kHz at Pin 7.
Valid 1 (27) Valid 2 (28) Inputs					
Low Level	*	—	3	V	*Note 4
High Level	V_{CC}-3	—	V_{CC}	V	
Input leakage to V_{SS}	—	—	10	μA	$V_{IN} = V_{CC}$
Valid Output (26)					Push Pull
Low Level	—	—	1.0	V	$I_{SINK} = 1mA$
High Level	V_{CC}-0.5	—	—	V	$I_{SOURCE} = 1mA$
Tuning Output (29)					V_{REF} 5 to 7.5 Volts
Low Level	—	—	0.4	V	I_{SINK} 1.3mA
High Level	V_{REF}-0.4	—	—	V	I_{SOURCE} 1.3mA
Rise time, fall time 10-90%	—	—	50	ns	C = 10pF
Tuning Reference (30)	5	—	7.5	V	
Supply Current Vcc (40)	—	—	45	mA	

NOTES: 1. All 'Pull Ups,' unless otherwise stated, are configured with Depletion FET's with Gate connected to Source. They have non-linear VI characteristics.
2. Rise time and fall times measured V_{CC}-1 to V_{CC}-8 Volts.
3. Tristate 'Pull Ups' and 'Pull Downs' are configured with Enhancement FET's. They have non-linear VI characteristics.
4. Guard ring to clamp any input more negative than V_{SS}. Maximum clamp current minus 100μA.

PIN FUNCTIONS

Pin No.	Name	Function
1	V_{SS}	Connect to zero volts.
2	16/32 Program/Resolution Option	Selects number of program and tuning resolution. Low 32 mode, high 16 mode.
3	Data I/O	To ER1400
4	C3	
5	C2	
6	C1	
7	16.0 kHz Clock	System Clock ÷ 128
8	Fine Tune Down	When connected low causes Fine Tune to decrement automatically at approximately 8 steps/second. There is a pause of approximately ⅛ second before the first step is executed. The input is disabled if either a Band Input is selected, Tune Up or Tune Down is selected or if MUTE is active. The tuning information is stored when Fine Tune Down is released. There is a 20 millisecond debounce on this store function.
9	Tune Up/Down Input	This is a tristate input which determines the direction of Tuning. Tune down for low, tuned up if open circuit or connected high. When using the 'Band Select Option' this input is used for tuning, low tune down, high tune up and open circuit 'OFF.' The Fine Tune Up/Down input is inhibited while tuning and the tuning information is stored automatically on release of either tune up or down. There is a 20ms antibounce delay on this store function. Note: Tuning will occur if this input is active, independently of the Band Inputs.
10	Band Step 3/4 Select	This is a tristate input. When connected low the 3 band step search mode is selected. When connected high the 4 band step search mode is selected. Tuning is now carried out using the Tune Up/Tune Down input.

Resolution

	B1	B2, 4	B3
Open 16 Prog.	11	12	14
Low 32 Prog.	12	13	14

In the 16 program mode, program numbers up to 32 are accepted on the 2^0, 2^1, 2^2, 2^3 and 2^4 inputs. The number of programs is limited to 16 only when the Program Up/Down input is used, in the 16 program mode.

ENTER-TAINMENT

Pin No.	Name	Function
11	Fine Tune Up	When connected low causes Fine Tune to increment automatically at approximately 8 steps per second. There is a pause of approximately ⅛ second before the first step is executed. This input is disabled if a Band Input is selected, Tune Up or Tune Down is selected or if Mute is active. The tuning information is stored when Fine Tune Up is released. There is a 20 millisecond antibounce delay on this store function.
12	Test/Copy Input	This is a tristate input. When connected low a copy bistable is set and COPY O/P goes low. Selection of a new program then copies the tuning information into this new program location and COPY O/P goes off. There is a 20ms antibounce delay on this input. When connected high puts the chip into Test mode.
13	Band Select Option	With this input low tuning procedure becomes: 1. Select band—this is latched on. 2. Tune Up or Down using the Tune Up/Down input.
14	Fine Tune, Tune Up/ Down Store Inhibit	Tristate Input, open circuit 'Store' active, low, Fine Tune 'Store' inhibit, high, Tune Up/Down and Fine Tune 'Store' inhibit.
15	Tuning Clock	Controls speed of tuning, (but not Fine Tuning), set by external RC network. Approximately 1.6kHz. Runs only while searching.
16	Auxiliary Output	This is an open drain output which turns on when the Auxiliary Input is low.
17	Auxiliary Input	Controls the Auxiliary Output. Also when high inhibits the Fine Tune inputs.
18	B4 Input/Output	These outputs go to 'Band Output' Low Level when the Band is selected. The band is selected by forcing 'Band Input' low onto the output. Operation of a band input starts the scan. Scan stops if band button is released and the tuning information is then stored automatically.
19	B3 Input/Output	
20	B2 Input/Output	
21	B1 Input/Output	
22	Mute Output	Active low for 256 milliseconds during program change, power on and 'standby OFF.' Also active if a Band I/P or Tune UP/DOWN I/P is active.
23	Copy Output	Active low when Copy is set. See earlier pin 12.
24	Search Output	Active low if a Band I/P or Tune UP/DOWN active. Goes off for 256ms as Tuning O/P overflows.
25	Standby Input	When low, disables Band, Program Up/Down, Fine Tune, Copy and Tune Up/Down inputs.
26	Valid Output	For TV Applications, with line sync connected to Valid Input 2 and line flyback to Valid Input 1, the presence of a VALID TV signal can be determined by filtering the Valid Output. This output can then be used for controlling auxiliary functions for example tuning speed and AFC. Valid output set high at Power on Reset.
27	Valid Input 1	
28	Valid Input 2	
29	Tuning Output	Tuning resolution, 14 bits maximum (see 'Option Input').
30	Tuning Reference Input	A tuning reference voltage can be connected to this pin. The tuning waveform output is then referenced to this level.
31	A/V Output	Active low if program, 16 or 32 is selected.
32	Program Up/Down Input	Connection to low decrements program number by 1 and connection to high increments program number by 1. There is a 20 millisecond debounce on this input. NOTE: Pin 2 state determines either a 16 or 32 Up/Down cycle.
33	System Clock	2.048MHz nominal, set by external RC network. This clock determines the tuning waveform ripple frequency and the Fine Tuning rate.
34	I/O Select Input	When connected low selects input mode for 2^0, 2^1, 2^2, 2^3 and 2^4 Prog. data. When I/O is low the EAROM is read every time data changes. Data is also read every time I/O goes low. When open circuit the 2^0, 2^1, 2^2, 2^3, and 2^4 Input/Outputs are high. When connected high the output mode is selected.
35	2^0 Input/Output	Binary program number Input/Output. When used as an input accepts data in positive logic convention (00000 = prog. 1). When used as an output the data is static and in positive logic convention.
36	2^1 Input/Output	
37	2^2 Input/Output	
38	2^3 Input/Output	
39	2^4 Input/Output	
40	Vcc	Connect to positive power supply +12 volts ±10%.

ENTER-TAINMENT

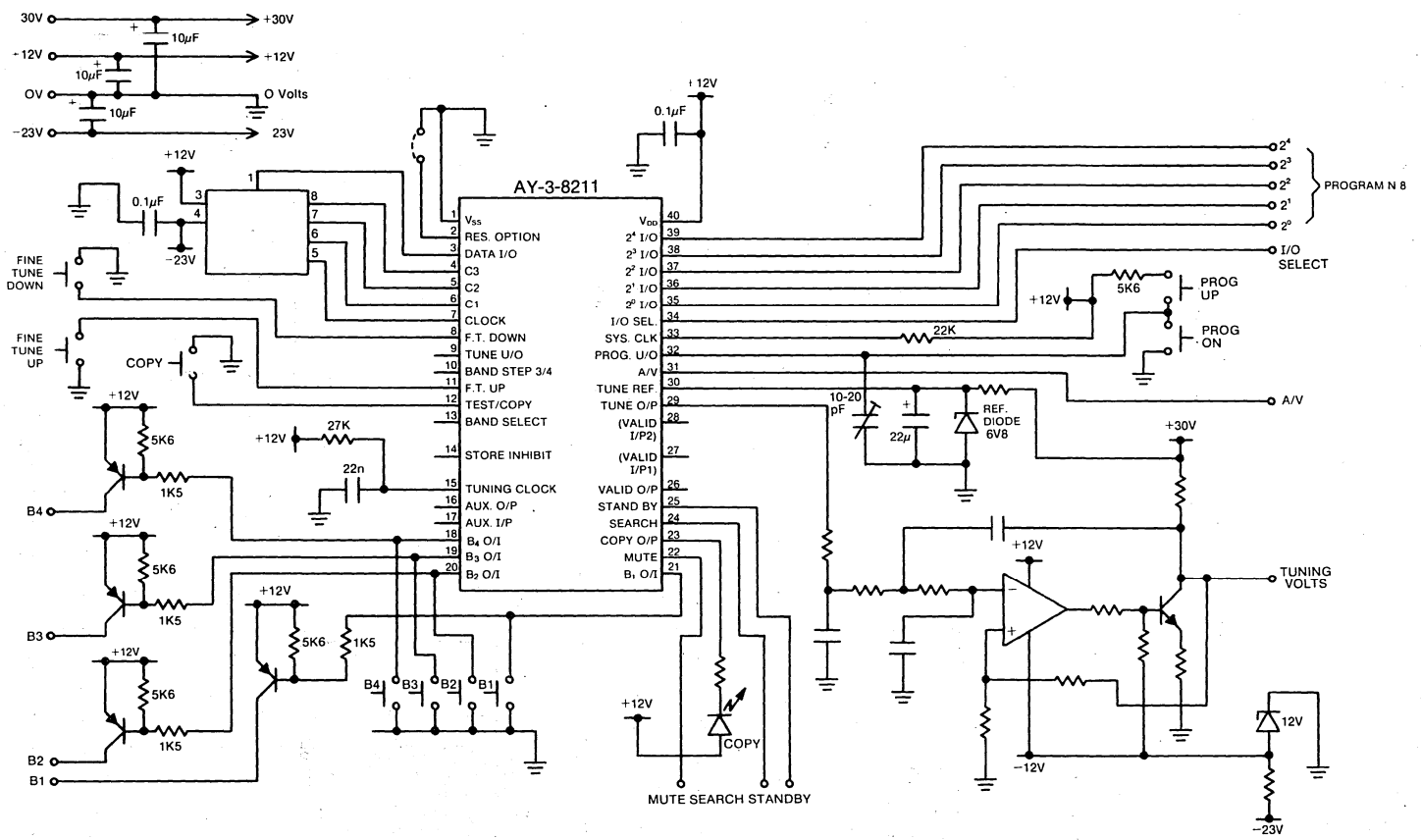


Fig. 5 BASIC SYSTEM IMPLEMENTATION

PLL Tuning System

FEATURES

- 100 channel tuning capability—includes all CCIR standard channels, Italian and Australian special channels
- 32 Favorite programs
- Automatic Sweep tuning option (with Automatic Fine Tune)
- Fine tune in 50kHz steps (manual for stable transmitters, Automatic for unstable transmitters)
- Two digit channel no. display
- Two digit program no. display
- EAROM non volatile memory
- Lock up time 10ms typical

DESCRIPTION

The TV Frequency Synthesizer is a system designed for accurate tuning of Color TV. It consists of the following five chips.

(a) Prescaler and Preamplifier—AY-9-2010	8 pin DIL
(b) Frequency Synthesizer—AY-3-2022	24 pin DIL
(c) Controller—PIC 1650	40 pin DIL
(d) Non-volatile Memory—ER1400	14 pin DIL
(e) Peripheral Circuit—AY-9-2017	18 pin DIL

The Controller is Microcomputer based so alternative features may be specified and the system could easily be reprogrammed for American requirements.

Channel No. Entry

Two buttons, Tens and Units, allow the channel number to be set. When operated the number increments every 0.5 secs., with no carry from the units. On release of the button the Channel number is stored in the memory against the selected Program Number.

Program No. Entry

Activation of parallel 5 bit binary input recalls the required program.

Program Display

This is available as a 2 digit multiplexed BCD output.

Channel Display

This is available as a 2 digit multiplexed BCD output.

Manual Fine Tune Up/Down

50kHz steps with a range of +4.0 MHz and -3.95MHz around the selected channel with roll over at both ends. On depression of the button one step is made, after a delay of 0.4 sec. steps are made every 50ms. The fine tuning is automatically stored on release of the button.

Automatic Fine Tune

This mode is selected if the Auto/Manual button is pressed, the status for any Program is stored in the EAROM. The Fine Tuning is then controlled by the output of the AFC discriminator and the system will track the Incoming Signal within ±25kHz. If there is no signal present the system will search within a range of ±4MHz in 50kHz steps at a rate of 12ms per step.

Auto Sweep Mode

Operating the Auto Sweep button causes the system to sweep through all the channels in steps of 250kHz at a rate of 100 steps per second. The channel number is incremented appropriately. When a station is found the sweep stops and the Auto Fine tune mode is entered.

Band Output

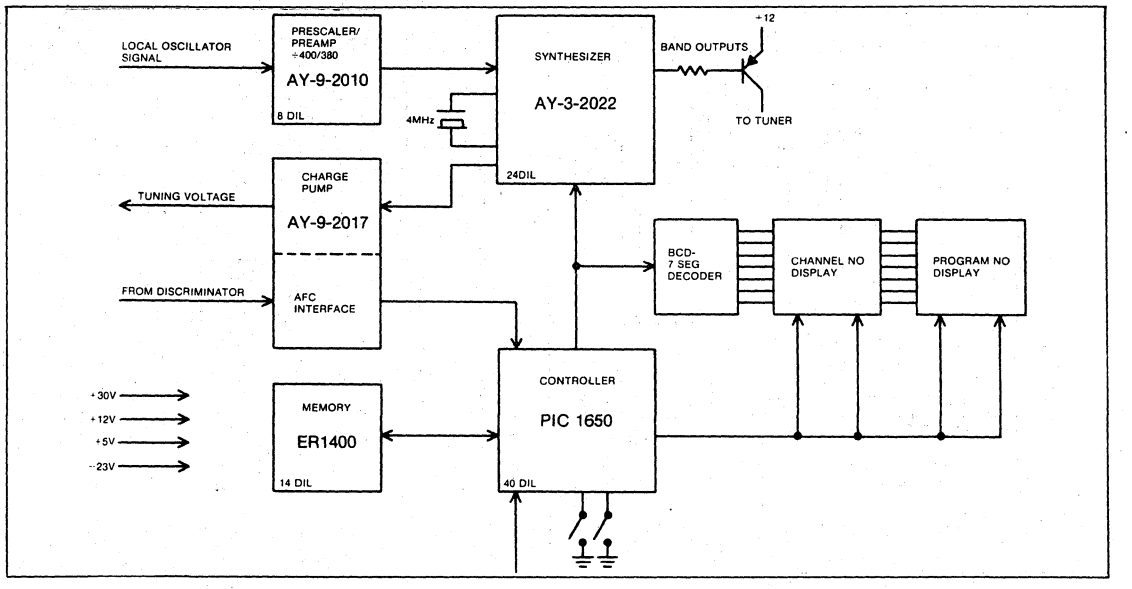
Four outputs are provided.

Memory

An ER1400 non volatile memory is used to store the Channel No., Fine Tune offset and Fine Tune mode for each of the 32 programs.

Power Up

At switch on Program 1 is selected.



TV Time/Channel Display Circuits

FEATURES

- Channel Display 1 to 16
- 4 Digit Clock Display option
- Color character on black background or color character on color background
- 14 or 24 DIL package

OPTIONS

Part Number	Channel	Time
AY-5-8301	1-16	No
AY-5-8320/21	1-16	

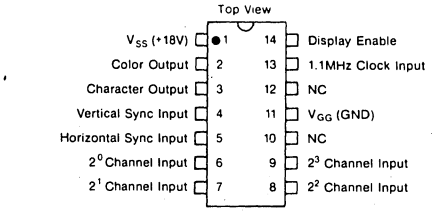
*The AY-5-8320/21 are capable of either simultaneous or separate time and channel display and have automatic display enable.

DESCRIPTION

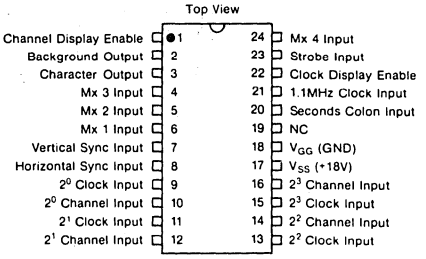
The AY-5-8300 series is a family of MOS circuits designed to display channel and time information on the screen of a TV set. The information is displayed as colored characters on a black or color background. Channel information is displayed as a single character 1 to 16. Time is provided as a 4 digit hours and minutes display. The display is positioned at the top right hand corner or at the bottom center of the screen; the display may be permanent or momentary. Any of the AY-5-8300 series may be used for either 525 or 625 line systems.

PIN CONFIGURATION

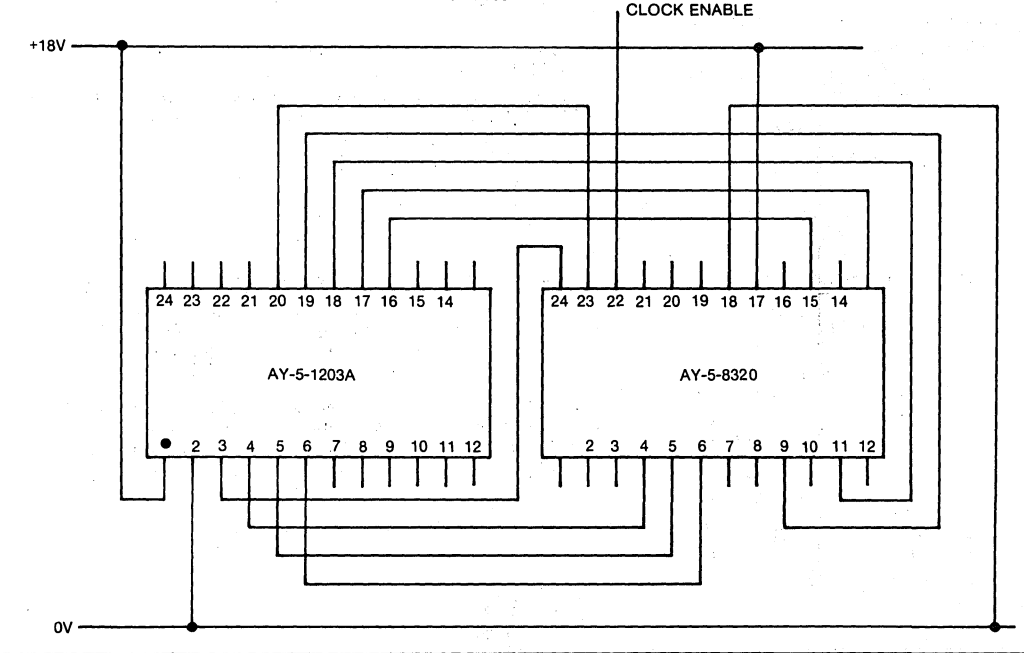
14 LEAD DUAL IN LINE
AY-5-8301



AY-5-8320/21



INTERCONNECT DIAGRAM FOR TV TIME DISPLAY



ENTER-TAINMENT

PIN FUNCTIONS

Name	Function
ALL TYPES:	
Vertical Sync Input	Resets the circuit at the end of each frame. At logic '0' during vertical flyback.
Horizontal Sync Input	Activates the line counter. At logic '0' during horizontal flyback.
1.1MHz Clock Input	Determines character position and width. Must be synchronized by horizontal sync pulse to prevent ragged edges on character.
Channel Inputs 2^0-2^3	
AY-5-8301 Display Enable	When taken to logic '0', the display is enabled. If an RC network is connected to this pin, a momentary display can be obtained.
AY-5-8301 Character Output	Defines the background border and the character.
Color Output	Determines the character color. Goes to logic '1' during a character block.
AY-5-8320/21 Clock Inputs 2^0-2^3	Multiplexed 4 digit BCD clock data inputs such as available from the AY-5-1203A clock circuit.
Mx1-Mx4	Multiplex inputs, at logic '1' during multiplex time slot. For the AY-5-8310/11, when operating in the 00-99 channel mode, Mx1 and Mx2 time slots are used.
Strobe Input	This input must go to a logic '1' during the middle of each Mx time slot to load the clock data into the chip.
AY-5-8320/21 Character Output	Defines the character outlines. At logic '1' when displaying a character.
Background Output	Defines the background block. At logic '1' when outputting background.
Channel Display Enable	When taken to logic '1', the channel display is enabled. The display is automatically enabled when the channel is changed.
Clock Display Enable	When taken to logic '1', the clock display is enabled.
Seconds Colon Input	This input controls the colon between the hours and minutes display. When at logic '0', the colon is blanked. If connected to the DP output of the AY-5-1203A clock circuit, the colon will flash once per second.

Code 2^3 2^2 2^1 2^0	Display AY-5-8301/20/21
0 0 0 0	1
0 0 0 1	2
0 0 1 0	3
0 0 1 1	4
0 1 0 0	5
0 1 0 1	6
0 1 1 0	7
0 1 1 1	8
1 0 0 0	9
1 0 0 1	10
1 0 1 0	11
1 0 1 1	12
1 1 0 0	13
1 1 0 1	14
1 1 1 0	15
1 1 1 1	16

ENTER-TAINMENT

OPERATION

The display is positioned digitally in both the vertical and horizontal directions. The vertical position is determined by counting horizontal sync pulses (the counting is initiated by the vertical sync pulse). The timing relationships are shown in Figs. 8a and 8b. Additionally, for the AY-5-8320/21, the time display is positioned 35 lines further down so that it appears immediately below the channel display.

In the horizontal direction the display is positioned by counting pulses from an external 1.1MHz oscillator which is synchronized with the horizontal sync pulse to prevent ragged edges on each character.

Each character is made up of 15 dots in a 3×5 matrix. With a one dot border around each character a total matrix of 35 dots in a 5×7 format is utilized. Each dot lasts 0.9 μsec in the horizontal direction and is 5 lines high. This gives a rectangular dot and characters as shown in Fig. 1.

The various channel/time display formats are illustrated in Figs. 4, 6 and 7. The display positioning on the TV screen is shown in Figs. 6a and 6b.

In the AY-5-8301, the character display is controlled by two outputs. Character and Color. The video channels are controlled in the following manner:

(a) Black/white display

Character	Color	
0	0	Normal picture
1	0	Black (luminance channel full off)
1	1	Black
0	1	White

(b) Black/Yellow display

Character	Color	Normal picture
1	0	Black (luminance full off)
1	1	Black (luminance full off and blue suppressed)
0	1	Yellow (luminance full on and blue suppressed)

Other color displays are generated by suppressing one or two chrominance channels.

In the AY-5-8320/21, one video output defines the characters and the other a background block. Using these outputs, a display of any color character on a background of any color may be obtained. these outputs, a display of any color character on a backgound of any color may be obtained.

The channel data is input on four lines; in 1—16 channel mode, this information is applied in binary from a diode encoder attached to the varactor tuning drivers. Binary numbers greater than 9 are detected and displayed at a two digit character.

In the clock mode, data is entered on a 4 line BCD bus multiplexed into 4 time slots. A strobe signal occurring in the middle of each time slot is used to read the data into the chip.

When the AY-5-1203A clock is used it can be directly connected to the AY-5-8320/21 with no external components. The AY-5-8320/21 displays the time with hours, minutes and a flashing colon for seconds (Fig. 5).

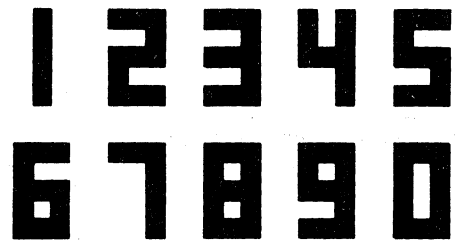


Fig. 1 CHARACTER SET (AY-5-8301/20/21)

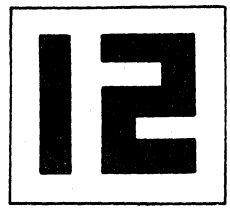


Fig. 2 CHANNEL DISPLAY

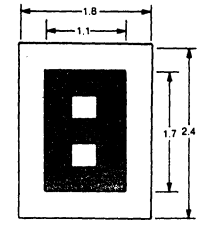


Fig. 3 CHARACTER SIZE (25/26 INCH SCREEN)

ENTER-TAINMENT

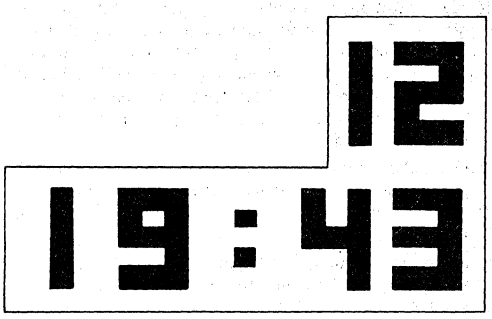


Fig.5 TIME AND CHANNEL DISPLAY (AY-5-8320/21)

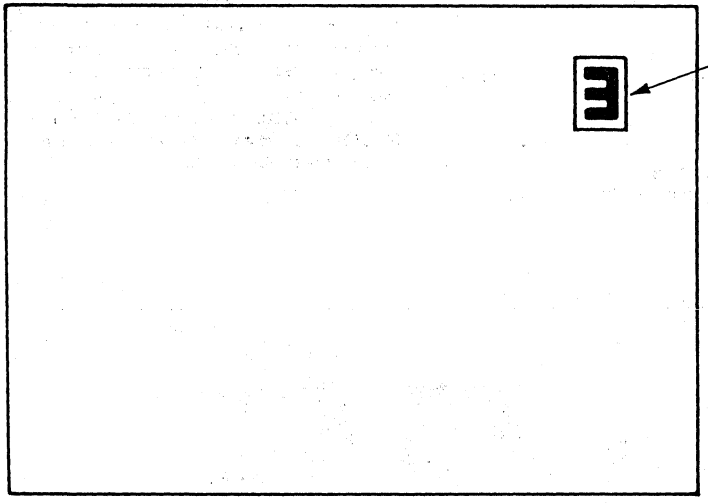


Fig.6a DISPLAY POSITION-CHANNEL

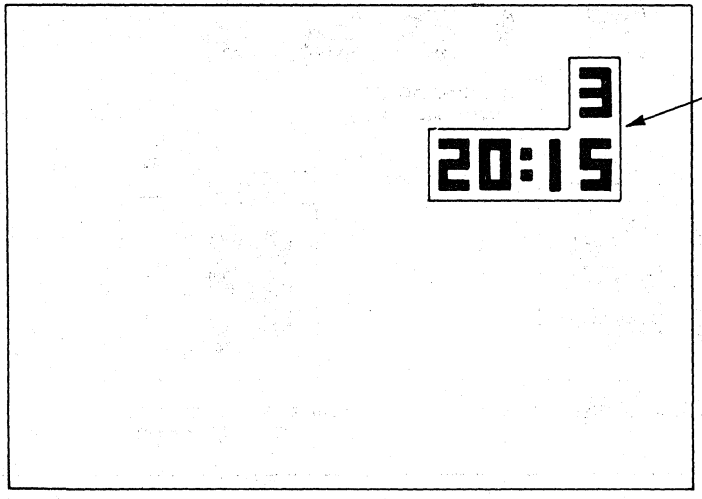


Fig.6b DISPLAY POSITION-CHANNEL

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . +0.3 to −20V
Ambient Operating temperature range . . . . . 0°C to +85°C
Storage temperature range. . . . . −65°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{GG} = 0V
V_{SS} = +17V to +19V
Operating Temperature (T_A) = 0°C to +85°C

Characteristic	Min	Typ**	Max	Units	Conditions
Vertical Sync Input (Note 1)					
Logic '0'	0	—	7	V	
Logic '1'	V_{SS} −5	—	V_{SS} +0.5	V	
Rise & Fall Time	—	—	5	μs	10% to 90% Min slew rate 5V/μsec
Horizontal Sync Input					
Logic '0'	0	—	7	V	
Logic '1'	V_{SS} −1.5	—	V_{SS} +0.3	V	
Rise & Fall Time	—	—	1	μs	10% to 90%
1.1MHz Clock Input	1.0	1.1	1.15	MHz	
Logic '0'	0	—	7	V	
Logic '1'	V_{SS} −5	—	V_{SS} +0.3	V	
Rise & Fall Time	—	—	300	ns	10% to 90%
Pulse width	250	—	—	ns	at logic 0 and logic 1 levels
Channel Inputs (Note 1)					
Logic '0'	0	—	7	V	
Logic '1'	V_{SS} −5	—	V_{SS} +0.5	V	
Leakage	—	—	10	μA	V_{IN} = (V_{SS}−19) Volts
Display Enable Inputs					
Switch point positive edge	V_{SS} −8	—	V_{SS} −5	V	
Outputs					
On resistance	—	—	1.5	kΩ	V_{OUT} = V_{SS} −2V
Off leakage	—	—	1	μA	V_{OUT} = 0V
Turn ON time	—	—	200	ns	10-90% load 25K & 20pF to ground
Power: AY-5-8301	—	—	400	mW	V_{SS} = +19V
AY-5-8320	—	—	750	mW	V_{SS} = +19V

**Typical values are at +25°C and nominal voltages.
NOTE:
1. These inputs are diode clamped to V_{SS}. Maximum clamp current 50μA.

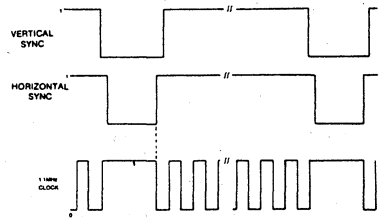


Fig. 7 INPUT WAVEFORMS

ENTER-TAINMENT

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . +0.3 to −20V
Ambient Operating temperature range . . . . 0°C to +70°C
Storage temperature range. . . . . −65°C to +150°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{GG} = 0V
V_{SS} = +11.4V to +12.6V
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Vertical Sync Input (Note 1)					
Logic '0'	0	—	3	V	
Logic '1'	V_{SS} −3.5	—	V_{SS} +0.3	V	
Rise & Fall Time	—	—	5	μs	10% to 90% Min slew rate 5V/μsec
Horizontal Sync Input					
Logic '0'	0	—	3	V	
Logic '1'	V_{SS} −3.5	—	V_{SS} +0.3	V	
Rise & Fall Time	—	—	1	μs	10% to 90%
1.1MHz Clock Input	1.0	1.1	1.15	MHz	
Logic '0'	0	—	3	V	
Logic '1'	V_{SS} −3.5	—	V_{SS} +0.3	V	
Rise & Fall Time	—	—	100	ns	10% to 90%
Pulse width	300	—	—	ns	at logic 0 and logic 1 levels
Channel Inputs (Note 1)					
Logic '0'	0	—	3	V	
Logic '1'	V_{SS} −3.5	—	V_{SS} +0.3	V	
Clock Inputs, Multiplex, Strobe Inputs					
Logic '0'	0	—	3	V	
Logic '1'	V_{SS} − 0.5	—	V_{SS} +0.3	V	
Input Resistance	—	20	—	kΩ	To V_{GG}
Display Enable Inputs					
Switch point negative edge	V_{SS} −5.5	—	V_{SS} −3.5	Volts	
Outputs					
On resistance	—	—	1	kΩ	V_{OUT} = V_{SS} −2V
Off leakage	—	—	1	μA	V_{OUT} = 0V
Turn ON time	—	—	200	ns	10-90% load 25K & 20pF to ground
Power	—	150	—	mW	V_{SS} = +12V

**Typical values are at +25°C and nominal voltages.
NOTE:
1. These inputs are diode clamped to V_{SS}. Maximum clamp current 0.5mA.

ENTER-TAINMENT

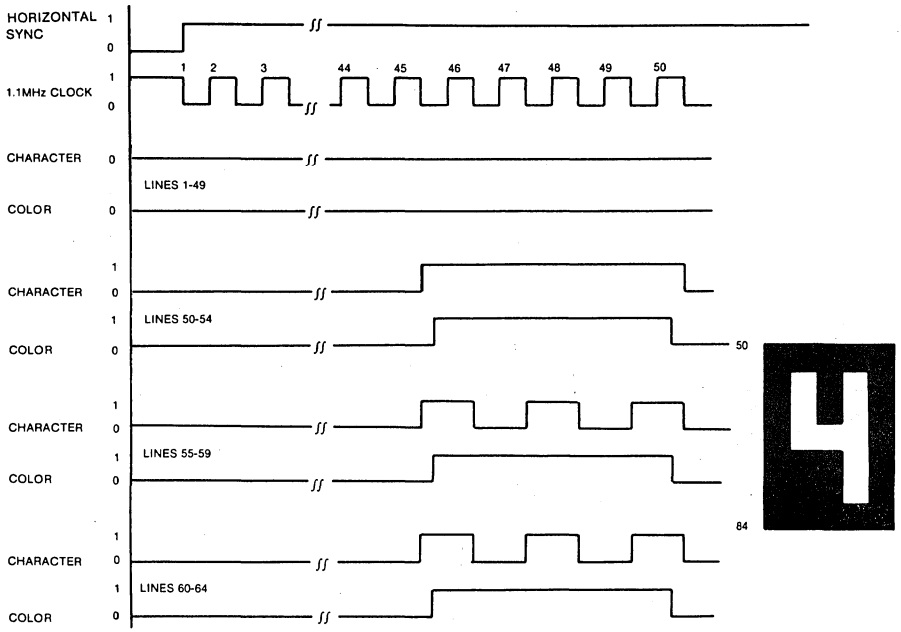


Fig. 8a OUTPUT WAVEFORMS (AY-5-8301)

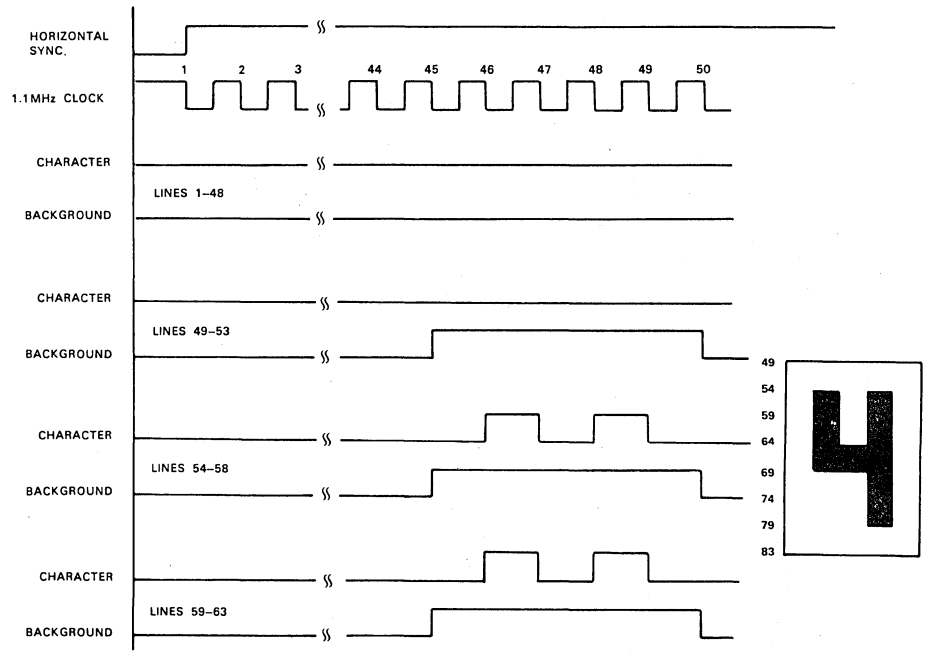


Fig. 8b OUTPUT WAVEFORMS (AY-5-8320/21)

ENTER-TAINMENT

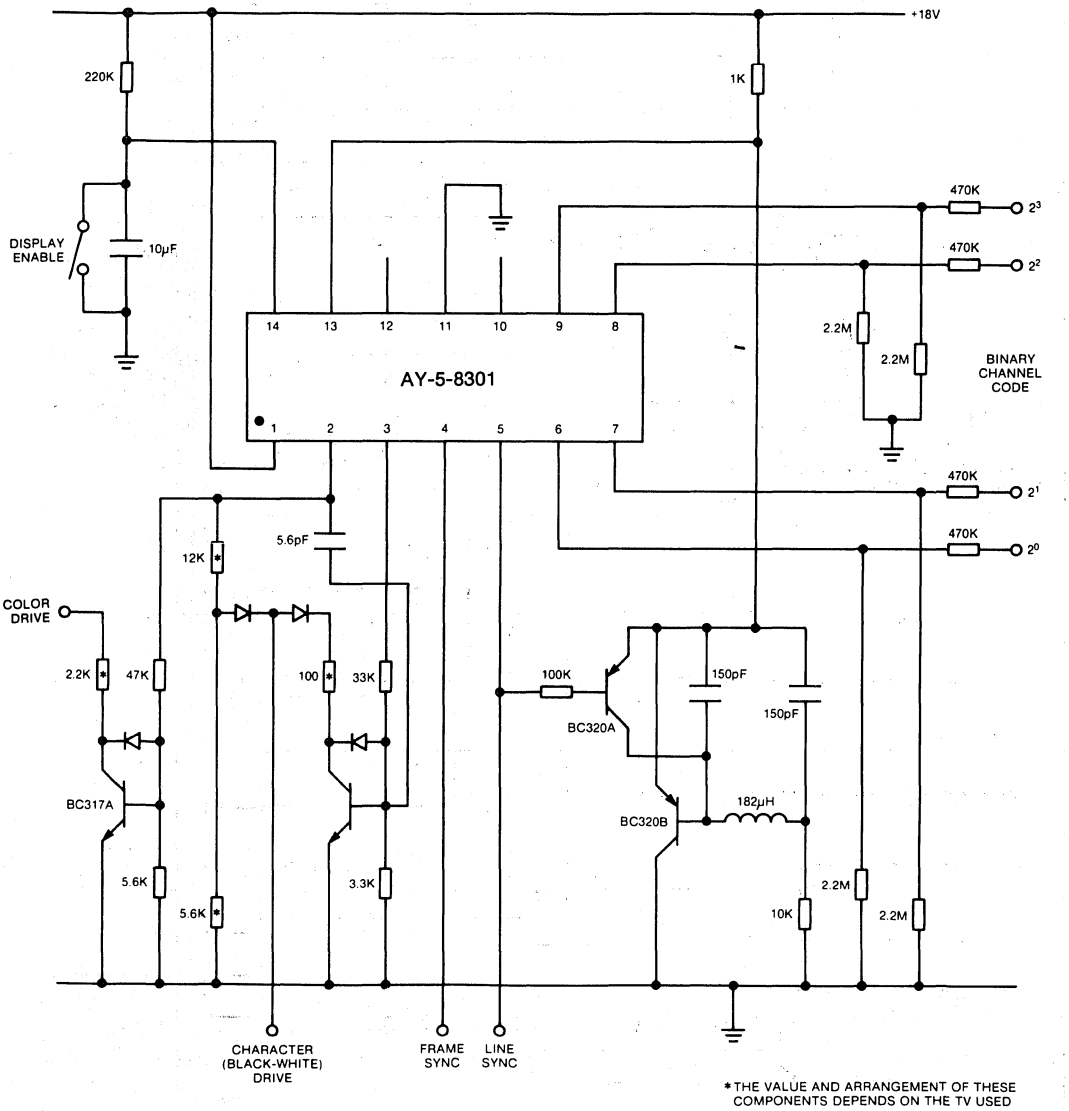


Fig.9

ENTER-TAINMENT

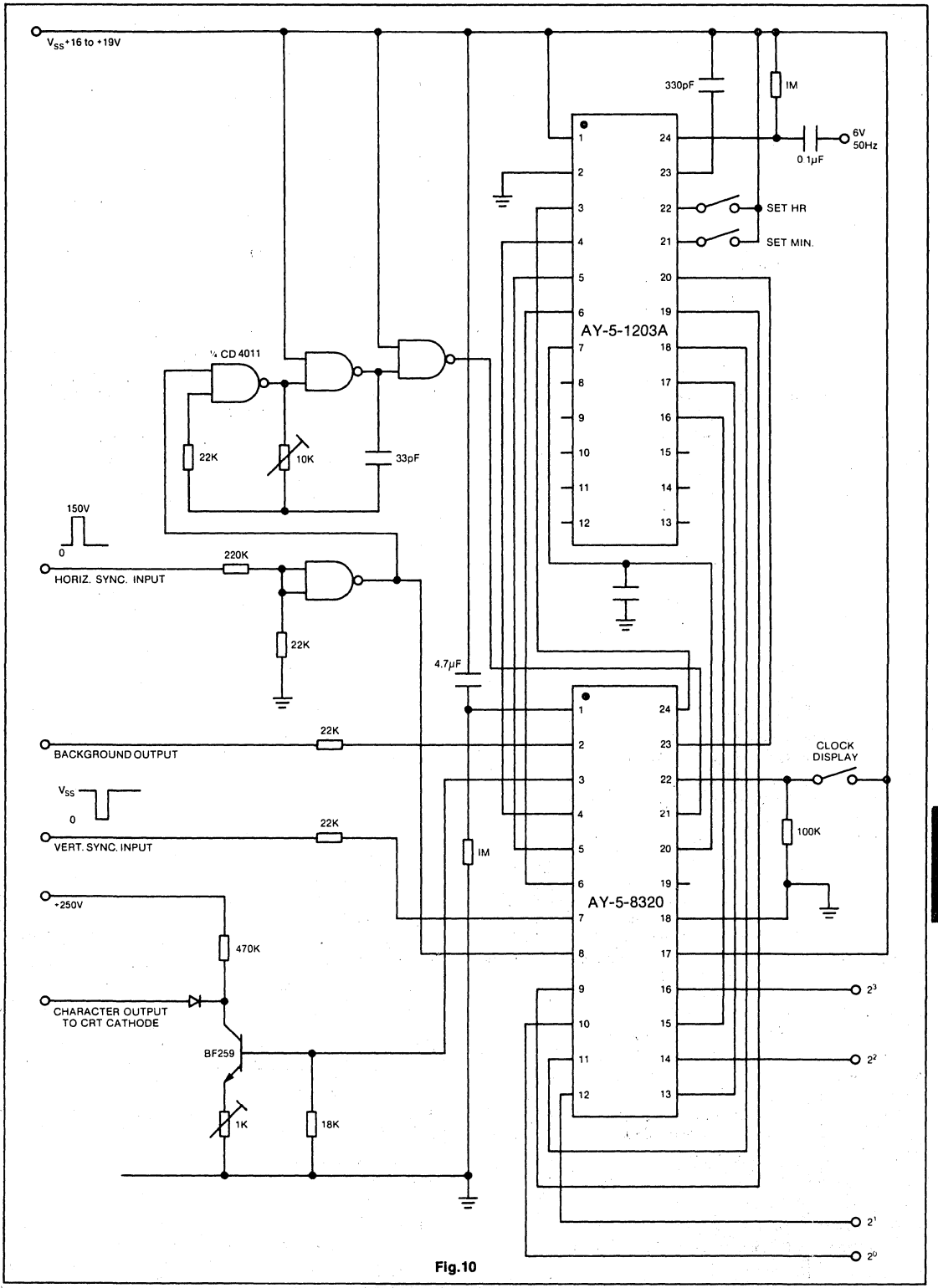

V_{SS} +16 to +19V
330pF
1M
6V
50Hz
0.1µF
SET HR
SET MIN.
AY-5-1203A
¼ CD 4011
22K
10K
33pF
150V
0
HORIZ. SYNC. INPUT
220K
22K
4.7µF
22K
BACKGROUND OUTPUT
V_{SS}
0
22K
VERT. SYNC. INPUT
1M
CLOCK
DISPLAY
100K
AY-5-8320
+250V
470K
CHARACTER OUTPUT
TO CRT CATHODE
BF259
1K
18K
2^3
2^2
2^1
2^0

Fig.10

Electronic On-Screen TV Tuning Scale

FEATURES

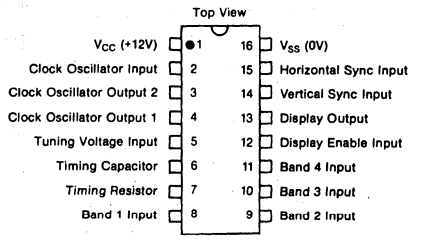
- Electronic tuning scale for 4 bands
- Mask programmable for Band or Channel number display
- Mask programmable for display position
- 12V operation compatible with GI digital tuning systems

DESCRIPTION

The AY-3-8331 is designed to provide an electronic on-screen tuning scale for varactor tuned TV sets. A horizontal line of variable length shows the tuning voltage and a scale is provided to aid tuning. Four bands are provided, band number or optional channel number being displayed. The band or channel number display may be mask programmed as desired within the limitation of 3 blocks of 5 x 7 dots (see Fig. 2). The graticule may also be programmed as required.

PIN CONFIGURATION

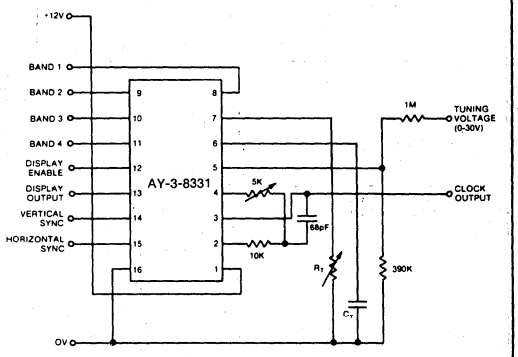
16 LEAD DUAL IN LINE



PIN FUNCTIONS

Name	Function
V_{CC}	Positive supply (+12V ± 10%)
V_{SS}	Ground
Horizontal Sync Input	Negative sync pulse from TV set
Vertical Sync Input	Negative sync pulse from TV set
Clock Input	1.1MHz master clock which fixes display horizontal position.
Clock Output 1	Intermediate clock output
Clock Output 2	Output of on-chip oscillator synchronized by Horizontal Sync. May be used to drive AY-5-8320 Display Circuit.
Tuning Voltage Input	Tuning voltage from Varactor diodes. Length of tuning bar is proportional to this voltage.
Timing Capacitor	Connect timing capacitor from this pin to V_{SS}.
Timing Resistor	Connect adjustable timing resistor from this pin to V_{SS}.
Band 1 Select Input	Connect to V_{SS} to select required band, either channel number or band number information will be displayed.
Band 2 Select Input	
Band 3 Select Input	
Band 4 Select Input	
Display Output	Positive going output of video information.
Display Enable Input	Connect to V_{SS} to enable display

SYSTEM DIAGRAM



ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to ground pin ..... -0.3 to +20V
Storage temperature range ..... -65°C to +150°C
Ambient operating temperature range .....0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +12V ± 10%
T_A = 0°C to +70°C
Clock frequency = 1.1MHz

Characteristics	Min	Typ**	Max	Units	Conditions
Inputs					
Logic '0'	0	—	+4	V	
Logic '1'	+8	—	Vcc	V	
Analog Input	0	—	+9	V	
Display Output					
Logic '0'	—	—	0.5	V	I_{sink} = 1mA
Logic '1'	V_{CC} -1	—	—	V	I_{source} = 1mA
$T_{\overline{on}}$, $T_{\overline{off}}$	—	—	200	nsec	
Power Supply Current	—	10	—	mA	

**Typical values are at +25°C and nominal voltages.

ENTER-TAINMENT

AY-3-8331 DISPLAY DIAGRAMS

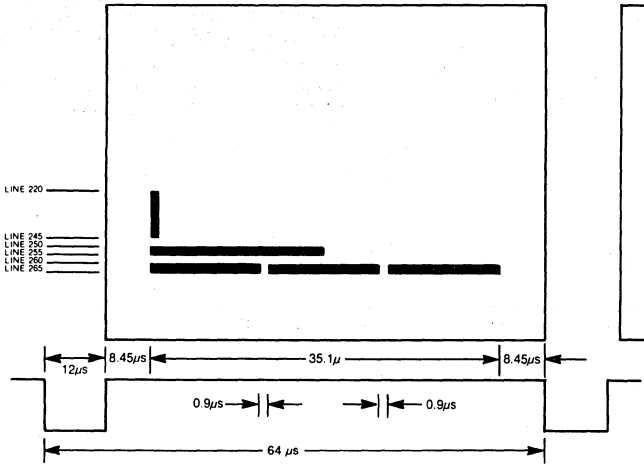


Fig. 1a BAND 1 DISPLAY

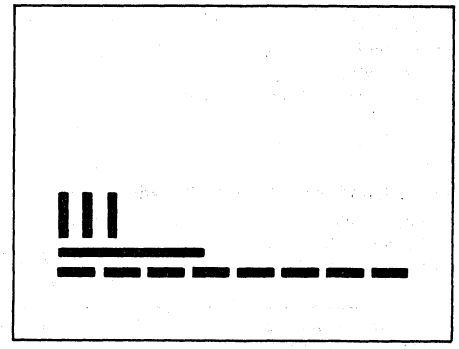


Fig. 1b BAND 2 DISPLAY

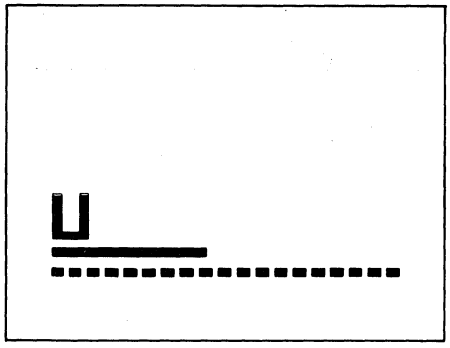


Fig. 1c BAND 3 DISPLAY

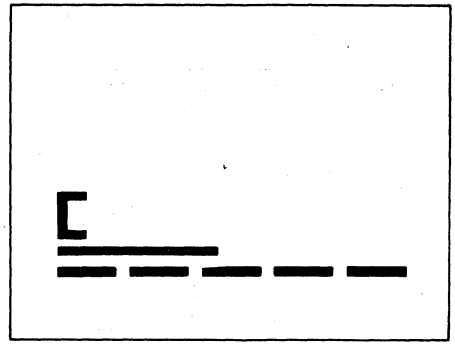


Fig. 1d BAND 4 DISPLAY

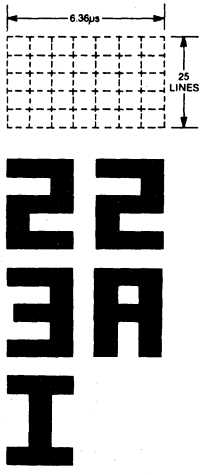


Fig. 2 TYPICAL CHARACTER FORMATS

ENTER-TAINMENT

Remote Control

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
R/C SYSTEM I	30 channel discrete frequency ultrasonic transmitter.	AY-5-8450	7-52
	16 channel discrete frequency ultrasonic receivers.	AY-5-8460	7-54
R/C SYSTEM II	264 command PCM infrared transmitter.	AY-3-8470	7-58
	264 command PCM infrared receiver.	AY-3-8475	7-64

30 Channel Remote Control Transmitter

FEATURES

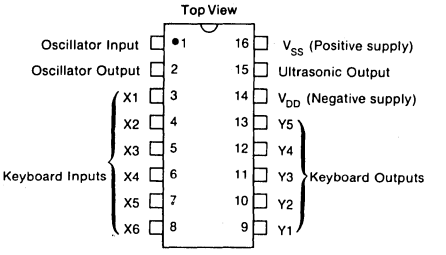
- 30 channels 346.4Hz spacing in the range 34-44kHz
- P-channel 9V battery operation
- 4.4336MHz TV crystal master oscillator
- 5 × 6 matrix keyboard input
- Low standby current drain (15μA max.)
- Compatible with AY-5-8460 receiver

DESCRIPTION

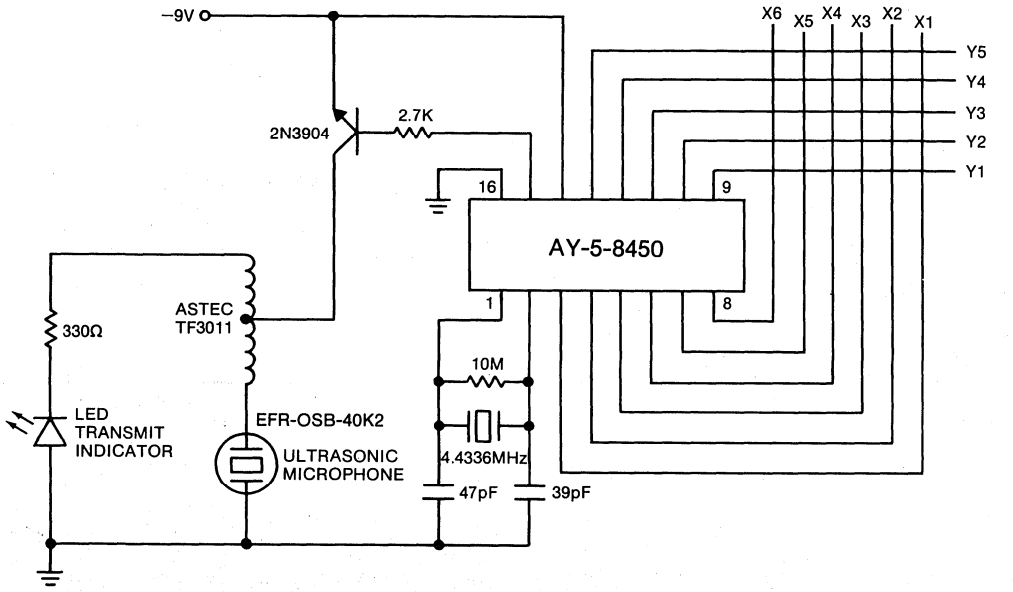
The AY-5-8450 allows the transmission of 30 commands using 30 different ultrasonic frequencies in the range 33.945 to 43.990kHz. It is designed for battery operation and uses a low cost TV crystal as the master oscillator. When inactive the circuit is in a standby mode having a current drain of less than 15μA. As soon as a key is depressed the main circuit is powered up and transmission commences.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



SYSTEM DIAGRAM



ENTER-TAINMENT

PIN FUNCTIONS

Pin No.	Name	Function
1	Oscillator Input	The Quartz crystal network is connected to these pins.
2	Oscillator Output	
3	X1	The keys are in the form of an XY matrix. As soon as a key closure is detected the chip is powered up and the keyboard is scanned at 3kHz. When it has been determined what key has been pressed the appropriate frequency is transmitted. If more than one key is pressed the chip ceases to transmit.
4	X2	
5	X3	
6	X4	
7	X5	
8	X6	
9	Y1	
10	Y2	
11	Y3	
12	Y4	
13	Y5	
14	V_{DD}	Negative supply (-9V nom)
15	Ultrasonic output	Off until key pressed
16	V_{SS}	Positive supply (ground)

Keyboard Inputs: X1–X6

Keyboard Outputs: Y1–Y5

OUTPUT FREQUENCIES

Crystal = 4.4336MHz

Key	Matrix	Frequency (Hz)	Key	Matrix	Frequency (Hz)	Key	Matrix	Frequency (Hz)
1	X1 Y1	33944.89	11	X3 Y1	34637.65	21	X5 Y1	35330.40
2	X1 Y2	37062.28	12	X3 Y2	39833.29	22	X5 Y2	35676.78
3	X1 Y3	37408.66	13	X3 Y3	40179.67	23	X5 Y3	36023.15
4	X1 Y4	37755.03	14	X3 Y4	40526.05	24	X5 Y4	42604.31
5	X1 Y5	38101.41	15	X3 Y5	40872.42	25	X5 Y5	42950.68
6	X2 Y1	34291.21	16	X4 Y1	34984.02	26	X6 Y1	36369.53
7	X2 Y2	38447.97	17	X4 Y2	41218.80	27	X6 Y2	36715.91
8	X2 Y3	38794.16	18	X4 Y3	41565.18	28	X6 Y3	43297.06
9	X2 Y4	39140.54	19	X4 Y4	41911.55	29	X6 Y4	43643.43
10	X2 Y5	39486.92	20	X4 Y5	42257.93	30	X6 Y5	43989.81

NOTE: The full key configuration/frequencies above are compatible with 30 channel receivers such as the GI SAA 1025. For operation with 16 channel receivers, such as the GI AY-5-8460/8461, only keyboard inputs X1 to X4 and keyboard outputs Y2 to Y5 are required.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... +0.3 to -12 Volts
Output current 10mA
Storage temperature range ..... -65°C to +150°C
Ambient operating temperature range ..... -10°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)
V_{SS} = 0V
V_{DD} = -7 to -10V
T_A = −10°C to 70°C

Characteristic	Min.	Typ	Max.	Units	Conditions
Clock Frequency	—	4.4336	—	MHz	See the Connection Diagram for external components
Key Contact Resistance:					
ON	—	—	100	Ω	
OFF	1	—	—	MΩ	
Key Capacitance	—	—	20	pF	
Output:					
On Resistance	—	—	600	Ω	To V_{SS}, V_{OUT} = -1V
Off Resistance	—	—	3	kΩ	To V_{DD}, V_{OUT} = V_{DD} +0.5V
Standby Current Drain	—	5	15	μA	
Operating Current Drain	—	12	15	mA	

ENTER-TAINMENT

16 Channel Remote Control Receiver

FEATURES

- 16 channels including 12 storbed (KB outputs), an on/off signal, one unstrobed output and 2 signals (up/down) for control of an analog function
- The 12 strobed outputs are in a 3 x 5 matrix format for direct parallel connection to a local keyboard
- On-chip oscillator using a 4.4336MHz TV crystal
- Compatible with AY-5-8450 or SAA 1024 transmitters

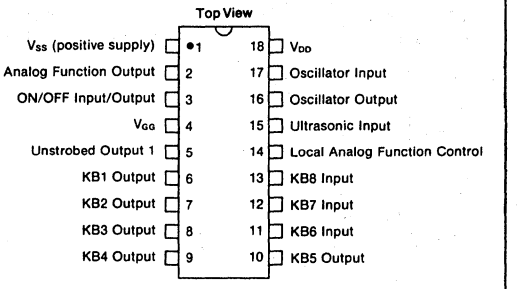
DESCRIPTION

The AY-5-8460 is a 16 channel ultrasonic remote control receiver designed to be compatible with the GI Omega TV and Stereomega Hi-Fi digital tuning systems, or any system which requires the use of a local keyboard in parallel with a remote control receiver. 12 of the received signals are output in a 1 of 5 code on lines KB1-5 upon application of the corresponding strobe on input lines KB6-8. This operation simulates the function of a mechanical 3 x 5 matrix keyboard. Additionally for other requirements, an on/off control and one unstrobed output is provided. The AY-5-8460 also recognizes two analog function controls to vary the mark/space ratio of an analog function output.

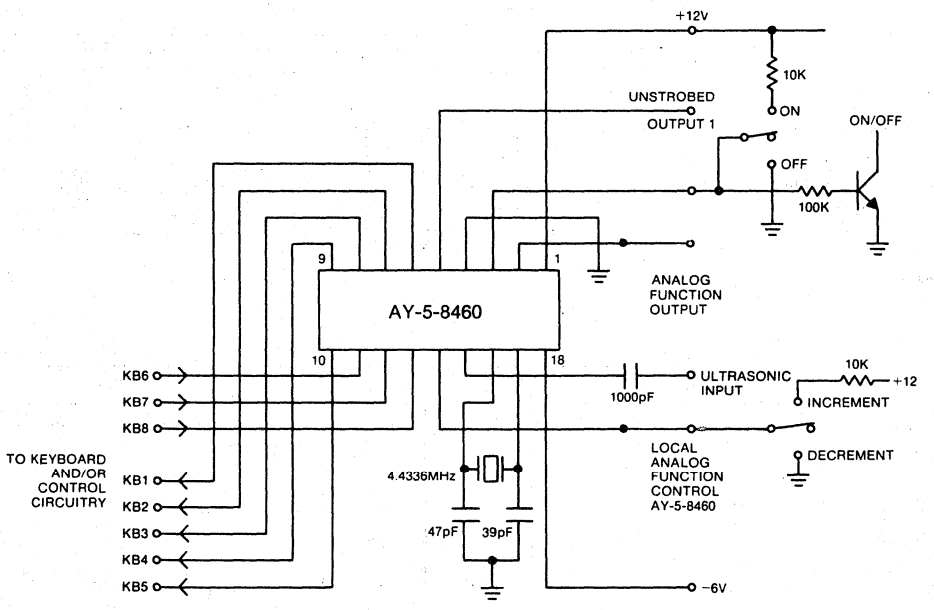
The AY-5-8460 can be operated by the AY-5-8450 remote control transmitter.

PIN CONFIGURATIONS

18 LEAD DUAL IN LINE
AY-5-8460



SYSTEM DIAGRAM



ENTERTAINMENT

Table 1 FREQUENCY ALLOCATIONS

Frequency Hz	Output Code
37,062	KB1/KB6
37,409	Unstrobed Output
37,755	On/Off Output
38,101	KB4/KB8
38,448	KB2/KB6
38,794	KB3/KB6
39,141	KB4/KB6
39,847	KB5/KB8

Frequency Hz	Output Code
39,833	KB5/KB6
40,180	KB1/KB7
40,526	KB2/KB7
40,872	Analog Function Down (AY-5-8460)
41,219	KB3/KB7
41,565	KB4/KB7
41,912	KB5/KB7
42,258	Analog Function Up (AY-5-8460)

PIN FUNCTIONS

Pin No.	Name	Functions
1	V_{SS}	Positive power supply.
2	Analog Function Output	This output is in the form of a pulse, the mark to space ratio of which can be changed in 125 steps from 1:126 to 126:1, the repetition frequency being 8.73kHz. The mark space ratio is incremented by one step about 115 msec after the start of an ultrasonic command, thereafter it is incremented every 46.2 msec. At power ON the output is normalized to a mark space ratio of 63:64. The output is also controlled by pin 14.
3	ON/OFF Output/Input	This output is toggled ON and OFF by reception of the corresponding ultrasonic command. At power up the output is set to the OFF state. When in the OFF state the Analog Function output is prevented from changing and the KB outputs are at logic '1'. The output may be turned ON by connecting it to V_{SS} via a 10kOhm resistor for 10μs, it may be turned OFF by connecting it to V_{GG}. The Ultrasonic command must be present for at least 0.7 sec to activate the output.
4	V_{GG}	This pin is externally maintained at $V_{DD}+(6V \pm 5\%)$, to serve as a ground reference for logic signals.
5	Unstrobed Output 1	This output is unstrobed and is at logic '0' for the duration of the corresponding ultrasonic command.
6	KB1 Output	A 3×5 matrix keyboard may be connected to the same pins. Maximum capacitance between intersecting matrix lines is 20pF.
7	KB2 Output	
8	KB3 Output	
9	KB4 Output	
10	KB5 Output	
11	KB6 Input	
12	KB7 Input	
13	KB8 Input	
14	Local Analog Function Control	This is a tristate input which provides local control of the Analog Function Output, pin 2. Connecting this pin to V_{SS} (V_{DD}) via a 10kOhm resistor causes the mark space ratio to increment (decrement). The input must be activated for 23msec. before the Output begins to change. This input has priority over the ultrasonic command for Analog Function Up/Down.
15	Ultrasonic Input	The ultrasonic signal should be capacitively coupled and be at least 500mV peak to peak. The first incoming pulse triggers a 23.1ms timer and after a delay of this period, two measurements of the ultrasonic signal are made over the following two 23.1ms periods. If the measurements produce a comparison an output is generated after a further pause of 46.2ms. The outputs are present for the duration of the ultrasonic command. During the complete receiving time the period of the ultrasonic signal is measured. If it is less than 18μsec or greater than 36μsec the signal is rejected and the receiver is set back to the start condition and a new measuring cycle commences. The input signals need not be completely accurate for satisfactory reception. At the lowest frequency an error of ±0.51% can be tolerated and at the highest ± 0.39%.
16	Oscillator Output	This is the output of the clock oscillator. One side of the crystal is connected to this pin.
17	Oscillator Input	This is the input of the clock oscillator. The other side of the crystal is connected to this pin.
18	V_{DD}	Negative power supply.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... +0.3 to -20 Volts
Storage temperature range ..... -65°C to +150°C
Ambient operating temperature range ..... 0°C to +70°C

*Exceeding these ranges could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = +12V ± 10%
V_{GG} = 0V
V_{DD} = V_{GG} — (6V ± 5%)
T_{amb} = 0°C to +70°C

Characteristic	Min.	Typ	Max.	Units	Conditions
Clock Oscillator Frequency	—	4.4336	—	MHz	
Ultrasonic Input					
Sensitivity	500	—	25	mVp-p	
Impedance	10	—	—	kΩ	
Inputs KB6-8					
Pull up resistance	—	—	200	kΩ	to V_{SS}
Logic '0'	—	—	V_{SS} -8	V	
Logic '1'	V_{SS} -1.5	—	—	V	
Analog Function Control Input (AY-5-8460)					
Increment Up	V_{SS}—1	—	V_{SS}	V	10K to V_{SS}
Increment Down	V_{GG}	—	V_{GG} +0.5	V	Short to V_{GG}
No Movement	—	—	—	—	Open Circuit
ON/OFF Input					
ON	V_{SS} -1	—	V_{SS}	V	Load 10K to V_{SS} & 100K to V_{GG}
OFF	V_{GG}	—	V_{GG} +0.5	V	Short to V_{GG}
Outputs KB1-5					
Logic '0'	V_{GG}	—	V_{GG} +0.5	V	Load 100K to V_{SS}
Logic '1'	V_{SS} -1	—	V_{SS}	V	
Unstrobed Outputs					
Logic '0'	V_{GG}	—	V_{GG} +0.5	V	Load 100K to V_{SS}
Logic '1'	V_{SS} -1	—	V_{SS}	V	
Analog Function Output (AY-5-8460)					
On Level	V_{SS} -1	—	V_{SS}	V	Load 68K to V_{GG}
Off Level	V_{GG}	—	V_{GG} +0.5	V	
Pulse Frequency	—	8.73	—	kHz	
ON/OFF Output					
Off	V_{GG}	—	V_{GG} +0.5	V	Load 100K to V_{GG}
On	V_{SS} -1	—	V_{SS}	V	
Supply Current	—	30	40	mA	V_{SS}—V_{DD} = 18V

ENTER-TAINMENT

Table 2

The table below illustrates the use of the AY-5-8460 R/C receiver with the AY-5-8450 R/C transmitter for the GI Omega TV and Stereomega Hi-Fi digital tuning systems.

R/C Transmitter AY-5-8450 Key/Matrix	Frequency (Hz)	R/C Receiver Output	Omega Function	Stereomega Function (Suggested Only)
2/X1 Y2	37,062	KB1/KB6	0	—
3/X1 Y3	37,409	Unstrobed Output 1	Recall	AM/FM Bandswitch
4/X1 Y4	37,755	On/Off Output	On/Off	On/Off
5/X1 Y5	38,101	KB4/KB8	Channel Down	Station #5
7/X2 Y2	38,448	KB2/KB6	1	—
8/X2 Y3	38,794	KB3/KB6	2	Search Stereo
9/X2 Y4	39,140	KB4/KB6	3	Search AM/FM
10/X2 Y5	39,487	KB5/KB8	Channel Up	Station #4
12/X3 Y2	39,833	KB5/KB6	4	Scan
13/X3 Y3	40,180	KB1/KB7	5	—
14/X3 Y4	40,526	KB2/KB7	6	—
15/X3 Y5	40,872	Analog Function Down	Volume Down	Volume Down
17/X4 Y2	41,219	KB3/KB7	7	Station #3
18/X4 Y3	41,565	KB4/KB7	8	Station #2
19/X4 Y4	41,912	KB5/KB7	9	Station #1
20/X4 Y5	42,258	Analog Function Up	Volume Up	Volume Up

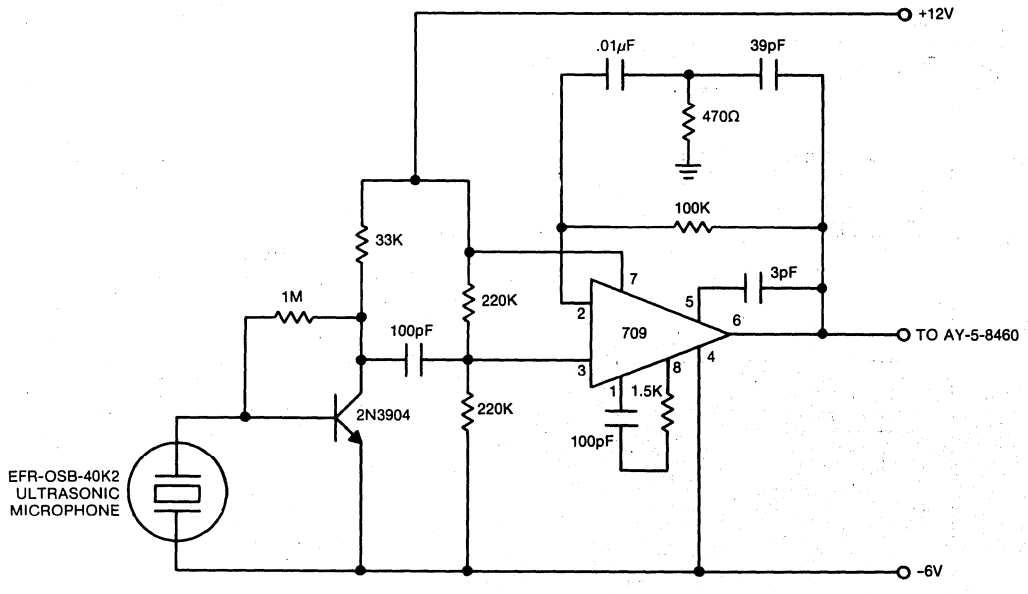


Fig.1 ULTRASONIC PREAMP

264 Command Infrared Remote Control Transmitter

FEATURES

- 256 Commands (possibly 32 commands by 3 bit address)
- Low Standby current (< 10μA)
- Low duty cycle (<8%)
- 6/9 Volt battery operation
- Simple RC defined on chip Oscillator
- 22 pin DIL package
- Single shot or continuous operation
- Transmission format ensuring error free reception

DESCRIPTION

The AY-3-8470 transmitter together with AY-3-8475 receiver, an infrared link and an amplifier, forms a complete remote control system. Control of standard functions of radios and televisions is possible together with TV games, Teletext and Viewdata applications.

Complementary MOS technology for this device allows low voltage battery operation with a very low standby current.

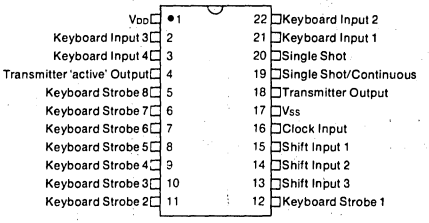
256 output commands are possible which can be simply activated by a standard 8 x 4 keypad together with 3 shift inputs.

A non critical, simple RC oscillator is used to fix the transmitter frequency.

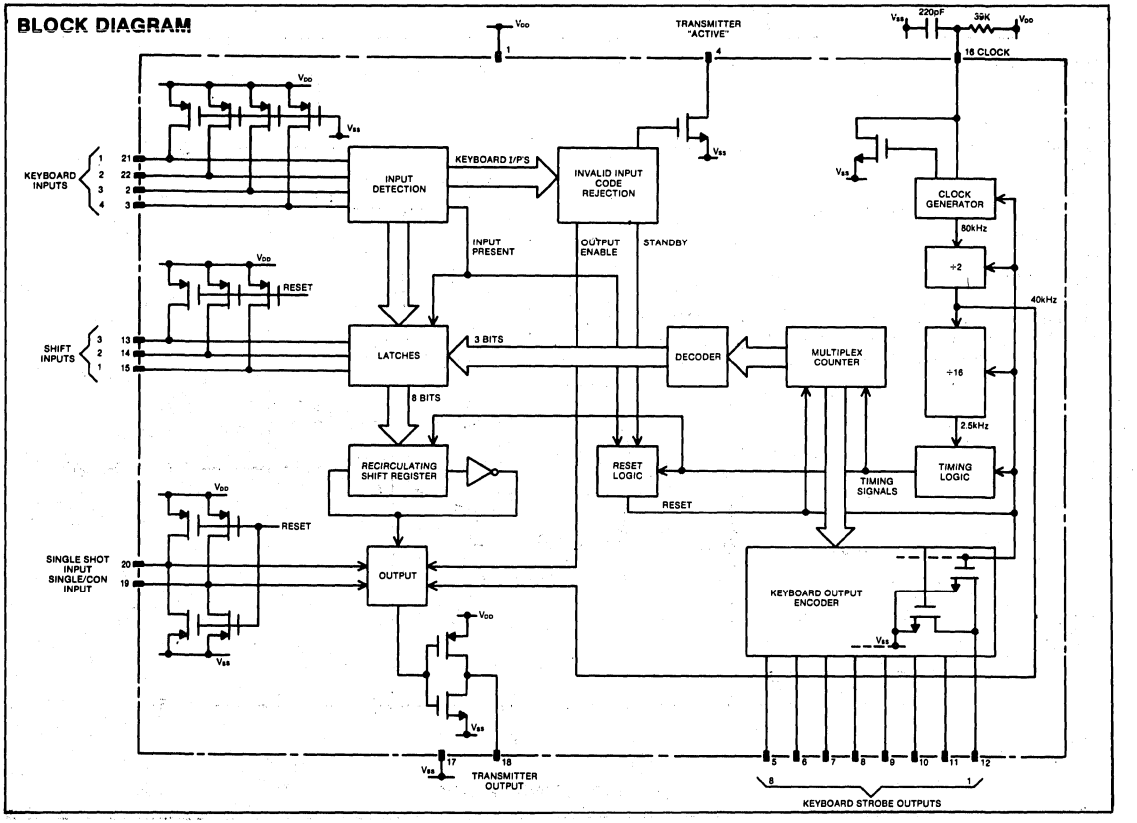
PACKAGE INFORMATION
PIN CONFIGURATION

22 PIN DUAL IN LINE

Top View



BLOCK DIAGRAM



ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... −0.3 to +12V
Ambient operating temperature ..... 0° C to 70° C
Storage temperature ..... −65° C to +150° C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

V_{SS} = 0 Volts
V_{DD} = +5.5 to +10 Volts
Temperature = 0° C to 70° C

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Clock Frequency (16)	F_C	55	80	105	kHz	V_{DD} = 5.5 to 10.0 V, T = 25° C C_C and R_C at typical values and C_C R_C tolerance ±5%
Resistor to V_{DD}	R_C	12	39	56	KΩ	
Capacitor to V_{SS}	C_C	—	220	—	pF	
Leakage to V_{SS}	—	—	—	10	μA	Clock "OFF" in 'standby' and V_{out} = V_{DD} = 10.0 Volts
Shift (13, 14, 15) ,Keyboard (2, 3, 21, 22) and Single Shot (19, 20) Input Thresholds						
Low Level	V_{IL}	V_{SS}	—	1.5	V	V_{DD} = 5.5 Volts
	V_{IL}	V_{SS}	—	2.5	V	V_{DD} = 10.0 Volts
High Level	V_{IH}	V_{DD}-1.5	—	V_{DD}	V	V_{DD} = 5.5 Volts
	V_{IH}	V_{DD}-2.5	—	V_{DD}	V	V_{DD} = 10.0 Volts
Pull Up to V_{DD}						
Low Level Source	I_{IL}	—	—	30	μA	V_{IN} = 1.5 Volts, V_{DD} = 5.5 Volts
	I_{IL}	—	—	120	μA	V_{IN} = 2.5 Volts, V_{DD} = 10.0 Volts
High Level	—	V_{DD}	—	—	V	I_{IH} = 2μA source
Transmitter Output (18)						
Low Level	V_{OL}	—	—	0.5	V	I_{OL} = 75μA sink
High Level	V_{OH}	V_{DD}-0.5	—	—	V	I_{OH} = 1.0mA source
Keyboard Strobe Outputs (5-12)						
Low Level	V_{OL}	—	—	0.5	V	I_{OL} = 150μA sink, V_{DD} = 5.5 Volts
	V_{OL}	—	—	1.5	V	I_{OL} = 600μA sink, V_{DD} = 10.00 Volts
Off Leakage to V_{SS}	—	—	—	2.0	μA	V_{OUT} = V_{DD} = 10.0 Volts
Transmitter 'Active' Output (4)						
Low Level	V_{OL}	—	—	1.5	V	I_{OL} = 1.5mA sink
Off Leakage to V_{SS}	—	—	—	10	μA	V_{OUT} = V_{DD} = 10.0 Volts
Single Shot (20), Single Shot/Continuous (19) Inputs						
Standby Pull Down to V_{SS}	V_{OL}	—	—	0.5	V	I_{OL} = 10μA sink
Supply Current V_{DD} (1)	I_{DD}	—	1	3	mA	V_{DD} = 10.0 Volts
Standby Current V_{DD} (1)	I_{DD}	—	5	20	μA	V_{DD} = 9.0 Volts, T = 25° C

NOTES: 1. Pull Ups are configured with Enhancement FET's.
2. Current from the device is defined as 'source' current, current into the device is 'sink' current.

ENTER-TAINMENT

PIN FUNCTIONS

Pin No.	Name	Function
1	V_{DD}	Positive Supply 5.5 to 10.0 Volts.
2	Keyboard Input 3	Together with Pins 3, 21, 22, these are the 4 keyboard inputs which under normal operations may only go active low one at a time.
3	Keyboard Input 4	
4	Transmitter 'active' output	Output goes low during a cycle in which a transmission is output.
5	Keyboard O/P 8	The 8 Keyboard Outputs are active low which strobe the Keyboard every transmission cycle (i.e. every 102.4ms for 80kHz clock). (See Fig. 1.) The outputs are open drain.
6	Keyboard O/P 7	
7	Keyboard O/P 6	
8	Keyboard O/P 5	
9	Keyboard O/P 4	
10	Keyboard O/P 3	
11	Keyboard O/P 2	
12	Keyboard O/P 1	
13	Shift 3	The Shift inputs correspond directly to the 3ms Bits of the output word. These inputs are active low.
14	Shift 2	
15	Shift 1	
16	Clock Input	Connect a resistor to V_{DD} and a capacitor to V_{SS} to determine the clock frequency.
17	V_{SS}	Connect to 0 Volts.
18	Transmitter Output	This output is in the form of a high going pulse stream at half clock rate modulated by the output code. (See Fig. 1).
19	Single/Continuous Select	With this input low, Pin 19 high, and Shift 3 low, single shot is selected.
20	Single Shot I/P	Connection low puts chip into single shot mode for all commands.
21	Keyboard Input 1	
22	Keyboard Input 2	

OPERATION

Standby

Standby mode is entered when power is applied to the chip. In this mode the 'clock' is inhibited, 'pull ups' are inactive (except Keyboard inputs), and all the Keyboard outputs are low (active).

Any key depression will now be immediately recognized, the chip will come out of standby and the 'all Keyboard outputs active' condition will be removed.

Keyboard outputs now strobe the keyboard and detect which key is depressed. At the end of a complete keyboard scan the relevant output is transmitted. Keyboard scans continue and the relevant outputs transmitted, until a full keyboard scan occurs detecting no key depression, the chip then reverts to standby.

Invalid Inputs

Invalid inputs occur due to multiple key depressions, they are:

(a) More than one Keyboard input active during a single keyboard output strobe time.

(b) More than one keyboard input active during different keyboard output strobe times within a 'full' keyboard scan.

The above inputs are rejected as invalid and no output code is transmitted although the chip remains active scanning the keyboard until it:

(a) receives a valid input which can be transmitted or

(b) it detects no keys pressed and reverts to standby.

Output Code

Figure 1 shows a typical output code sequence and the relevant strobe timings.

The output code takes the form of an 8 bit word followed by its inverse so ensuring a 'secure' infrared link. The infrared receiver being able to distinguish this 'data' from spurious inputs.

An example of the data is shown below. Note the L.S. Bit is transmitted first.

e.g. 0 0 1 1 0 1 0 0 (LSB) INVERSE 1 1 0 0 1 0 1 1 (LSB) TRUE

Each '0' bit is comprised of 32 pulses and each '1' bit 48 pulses. The complete command consists of 16 bursts of 32 or 48 pulses. The pulses have a nominal period of 25μs (i.e. 40kHz repetition rate). A burst takes 1.6ms and 16 bursts 25.6ms. During the 76.8ms the transmitter is inactive.

Output Code Derivation —'the 8 bit word'

Figure 2 identifies the binary output codes associated with the 'basic' keyboard matrix.

Binary codes can be expanded up to 255 by means of the shift inputs. The table Figure 3 shows the states of these inputs for relevant output codes.

Single Shot Operation

In this mode the code is transmitted only once after a key 'ON' is detected. The key must now be released, the chip enters standby mode and is then ready for a further key depression. Commands can be entered up to a rate of 5 per second.

An application for this mode of operation would be for transmitting page numbers for the General Instrument Teleview System.

The following table Fig. 4 shows the Single Shot modes of operation.

Keyboard Implementations

Figure 5 shows how diodes can be employed to expand the basic 8 x 4 matrix to 128 keys. The further Shift input expands the matrix to 256 commands.

Figure 6 shows how a simple 8 way switch can be used to enable 256 commands from the basic 8 x 4 matrix.

Transmitter

The circuit of Figure 6, employs 3 transmitting diodes pulsed at approximately 300mA, giving a range of up to 20 mete s. Average battery current for transmission is around 20mA with a standby current of only 20μA.

ENTER-TAINMENT

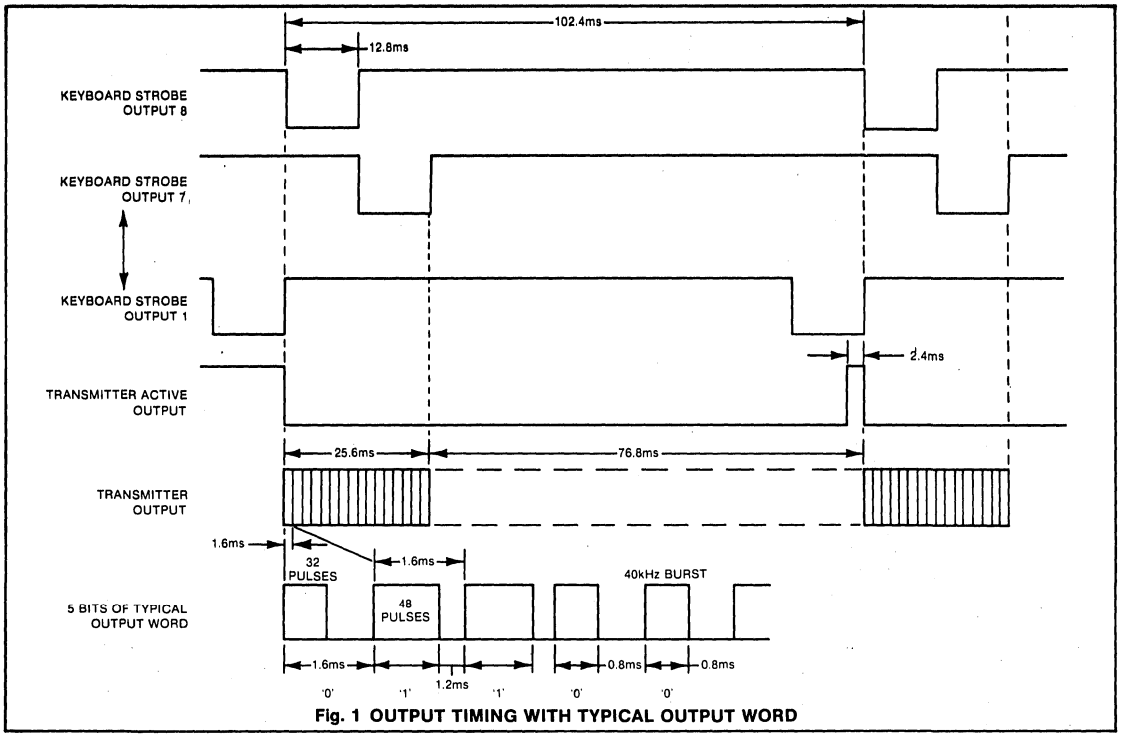
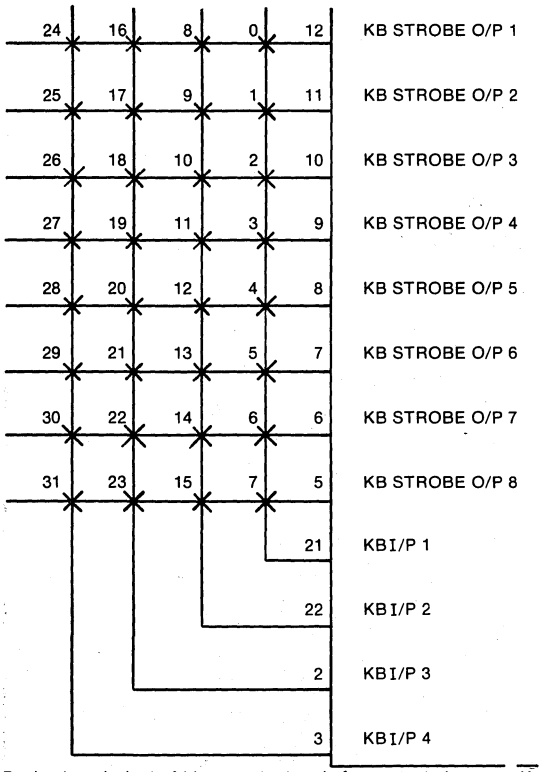


Fig. 1 OUTPUT TIMING WITH TYPICAL OUTPUT WORD



Decimal equivalent of binary output code for contact closure at X.

Fig. 2 MATRIX FORMAT

Shift Input 3 (13)	Shift Input 2 (14)	Shift Input 1 (15)	Output Codes
H	H	H	0 to 31
H	H	L	32 to 63
H	L	H	64 to 95
H	L	L	96 to 127
L	H	H	128 to 159
L	H	L	160 to 191
L	L	H	192 to 223
L	L	L	224 to 255

H signifies High Level
L signifies Low Level

Fig. 3 SIGNIFICANCE OF SHIFT INPUTS

Single Shot Input (20)	Single Shot/ Continuous (19)	Mode
H	H	Continuous on all Codes.
L	'Don't care'	Single Shot on all Codes.
H	L	Codes 0 to 127 continuous. Codes 128 to 255 Single shot.

NOTE: During Standby Single Shot Input (20) and Single Shot/ Continuous Input (19) are pulled low internally.

Fig. 4 SINGLE SHOT MODES OF OPERATION

ENTER-TAINMENT

Code Allocations

Transmitted Code*	Receiver Functions (Using the AY-3-8475)
0	Program 1
1	Program 2
2	Program 3
3	Program 4
4	Program 5
5	Program 6
6	Program 7
7	Program 8
8	Program 9
9	Program 10
10	Program 11
11	Program 12
12	Program 13
13	Program 14
14	Program 15
15	Program 16
16	Volume Increase

Transmitted Code*	Receiver Functions (Using the AY-3-8475)
17	Volume Decrease
18	Color Increase
19	Color Decrease
20	Brightness Increase
21	Brightness Decrease
22	Spare Increase
23	Spare Decrease
24	Normalize
25	Mute
26	ON/OFF to OFF
27	Spare 1 On
28	Spare 1 Off
29	Spare 1 Toggle
30	Spare 2 On
31	Spare 2 Off
32-47	Program 17-32
48-255	Spare

*Decimal equivalent of 8 bit binary word listed for convenience.

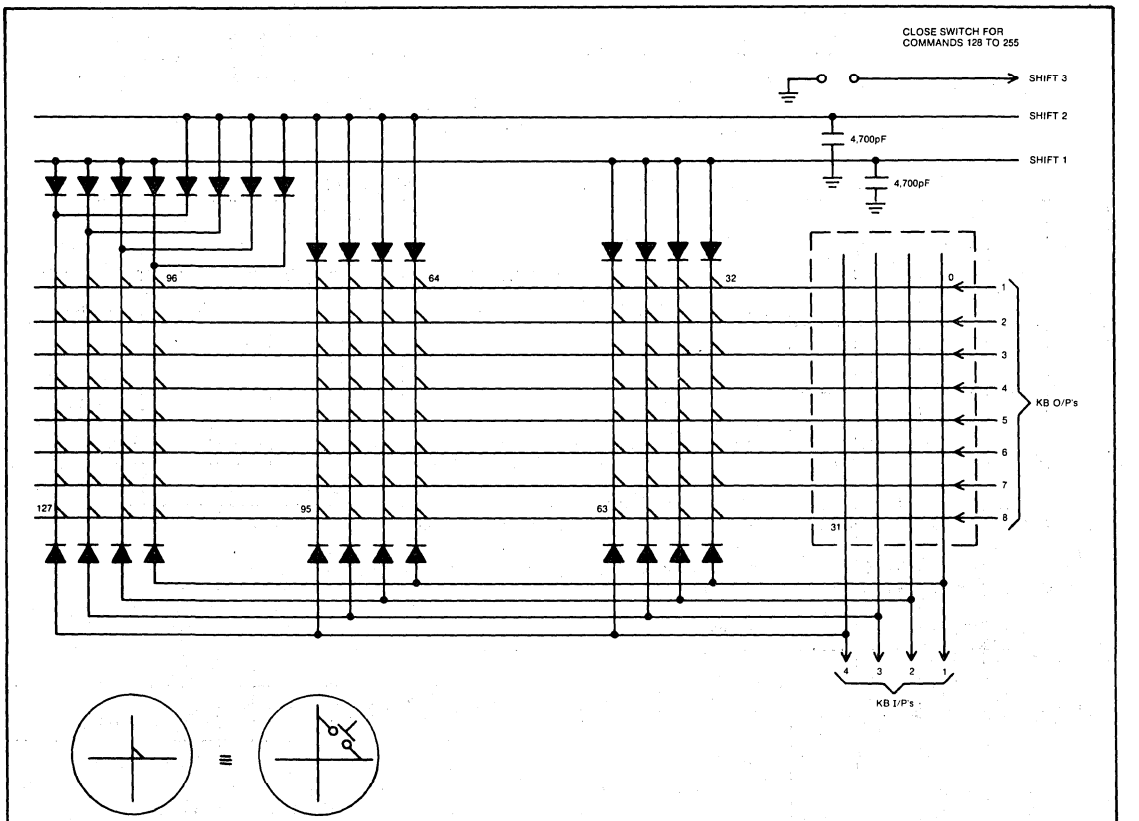


Fig. 5 USE OF DIODES TO EXPAND KEYBOARD TO 128 COMMANDS

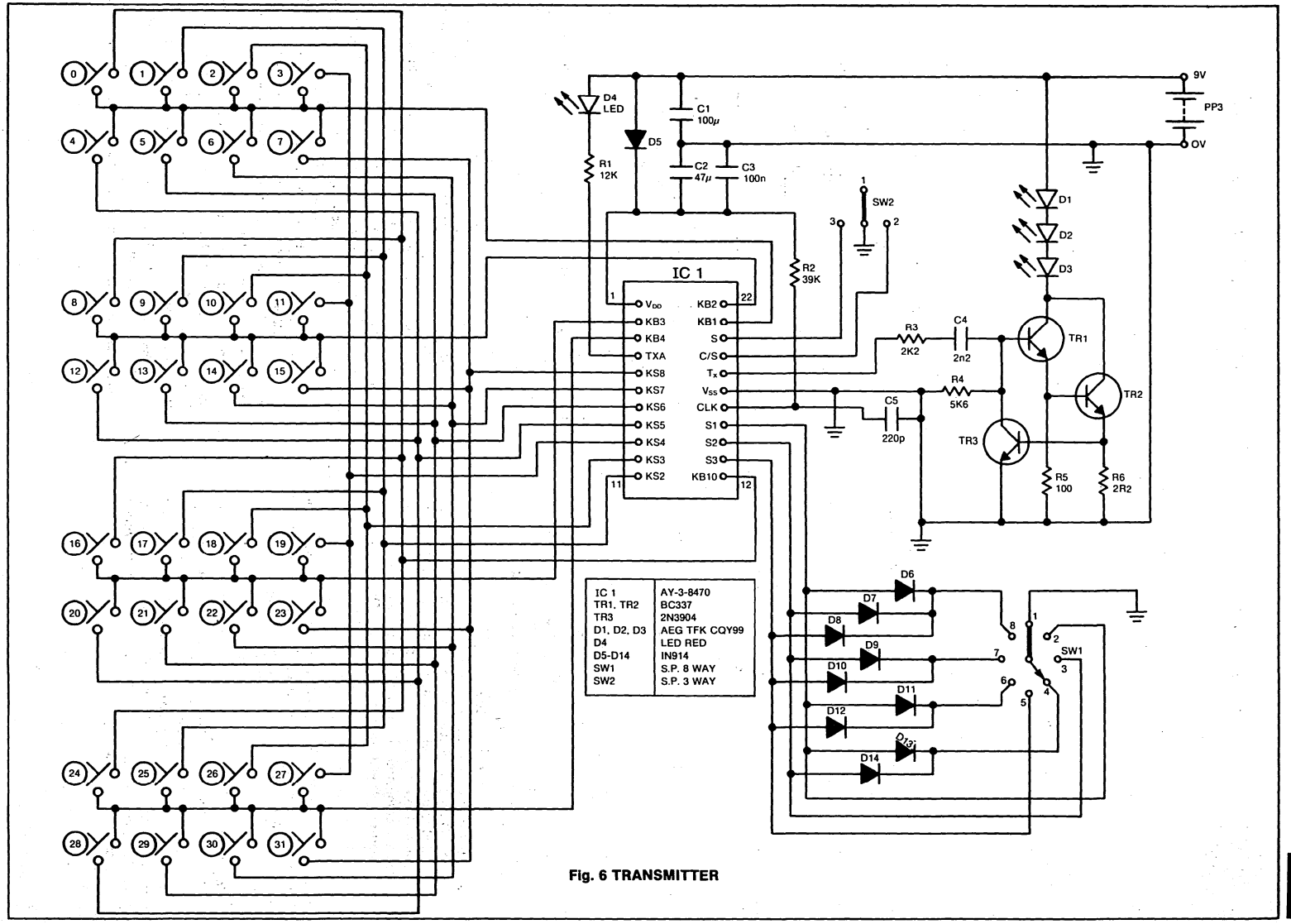


Fig. 6 TRANSMITTER

264 Command Infrared Remote Control Receiver

FEATURES

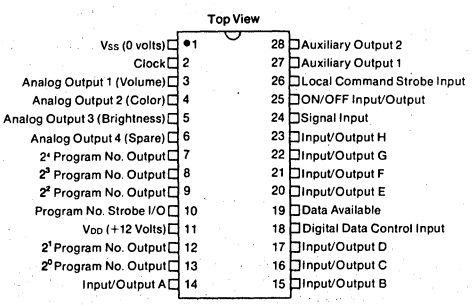
- 256 Commands
- Latched program number outputs
- 32 Programs
- 4 Analog Channels—62 step
- ON/OFF facility
- Normalize command on analog functions (except volume)
- 2 Auxiliary ON/OFF outputs (one with toggle facility)
- Local control of all 256 commands
- CPU Databus interface
- Direct Interface with General Instrument Teleview System
- Direct Interface with Economega TV and Radio Tuning Systems
- Command fully error checked ensuring secure link

DESCRIPTION

The AY-3-8475 receiver together with the AY-3-8470 transmitter forms a complete 256 command infrared remote control system. Applications include both radios and television. Control of normal TV functions is possible together with Teletext/Viewdata. Direct interface is possible with the Economega electronic tuning systems.

PIN CONFIGURATION

22 Pin Dual in Line



OPERATION

All operations, repetition rates, set-up times and resolutions are related to the "Clock" Frequency of 2.5MHz unless otherwise stated.

Power On

When power is applied to the chip a power on reset is generated and outputs are as follows: NOTE: power on to reset delay about 3μs.

(a) Program Number Outputs set to 1 (00000) and Program No. Strobe goes low for approximately 50ms.
(b) Analog outputs set to a mark space ratio of 32:31.
(c) ON/OFF I/O set to OFF.
(d) Auxiliary Outputs set to OFF.
(e) Data Available set low.
(f) Input/Outputs A-H set low. Note this data will only be presented to the output pins under control of the Digital Data Control input.

Any program command or a local ON command will turn on the ON/OFF output. It will remain on until an 'OFF' command is received.

Normalization

The Normalize command sets analog outputs 2, 3 and 4 (color, brightness and Spare), to a mark space ratio of 32:31. Analog Output 1 (Volume) is not affected by the normalize command.

Muting

Analog Output 1 (Volume) is set low when a mute command is received. It is returned to its previous mark space ratio by:

(a) A further mute command.
(b) Reception of any program command.
(c) Switching on the ON/OFF output.
(d) Reception of either the Volume increase, or Volume decrease commands.

For a remote mute command the command is repeated every 100ms as long as the transmitter remains active. Only one mute command is actioned. The transmitter must cease transmitting for at least 0.5 secs before a further mute command can be received, to toggle the function.

Signal Input

Figure 1 shows a typical command input from the IR Transmitter. A Valid input takes the form of an 8 'bit' word followed by its inverse. The L.S. Bit 'arrives' first:

e.g.

INVERSE								TRUE							
0	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1
						LSB								LSB	

Each '0' bit is comprised of 32 pulses and each '1' bit of 48 pulses. The complete command therefore consists of 16 bursts of 32 or 48 pulses. The pulses have a nominal period of 25μs (i.e. 40kHz repetition rate). A burst takes 1.6ms and 16 bursts 25.6ms. During the remaining 76.8ms the transmitter is inactive.

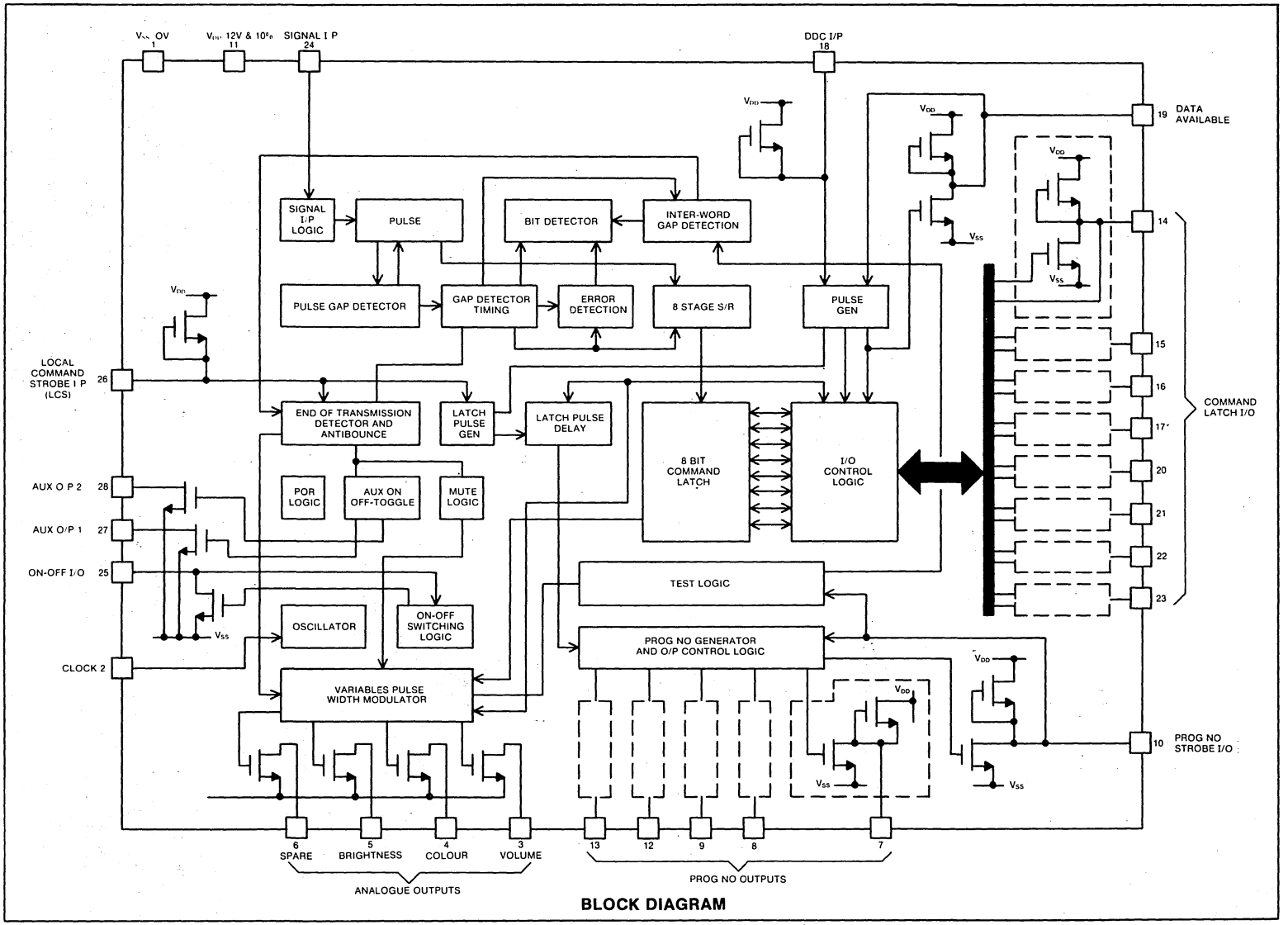
The receiver will decode input frequencies in the range 30kHz to 50kHz for its specified operating range of Clock Frequencies. The mark space ratio of the input waveform is not critical, however the mark or space interval should be at least 2μs.

The receiver has an error margin of ±8 pulses in each burst i.e. a '0' will be decoded if 25-40 pulses are received and a '1' will be decoded if 41-56 pulses are received.

The receiver 'looks for' a valid data bit i.e. a burst of pulses. The decoder synchronizes to this valid data bit and then looks for further 'bits' and inter-bit 'gaps'. If a sequence of an 8 bit word occurs, followed by its inverse then this is decoded as a command. Any erroneous bits or their inverses cause the decoder to reset and await resynchronization.

Command data outputs A-H correspond directly to the 8 'bit' word.

ENTERTAINMENT



BLOCK DIAGRAM

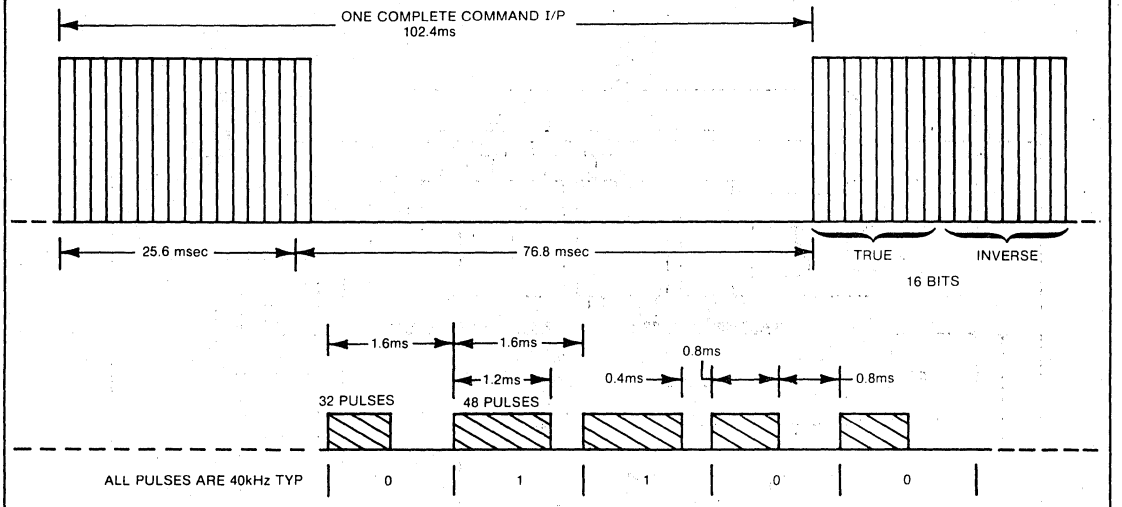


Fig. 1 EXAMPLE INPUT FORMAT

COMMAND DECODING

Transmitted code and Output code (A-H)*	Receiver Functions	Transmitted code and Output code (A-H)*	Receiver Functions
0	Program 1	25	Mute
1	Program 2	26	ON/OFF to OFF
2	Program 3	27	Spare 1 On
3	Program 4	28	Spare 1 Off
4	Program 5	29	Spare 1 Toggle
5	Program 6	30	Spare 2 On
6	Program 7	31	Spare 2 Off
7	Program 8	32	Program 17
8	Program 9	33	Program 18
9	Program 10	34	Program 19
10	Program 11	35	Program 20
11	Program 12	36	Program 21
12	Program 13	37	Program 22
13	Program 14	38	Program 23
14	Program 15	39	Program 24
15	Program 16	40	Program 25
16	Volume Increase	41	Program 26
17	Volume Decrease	42	Program 27
18	Color Increase	43	Program 28
19	Color Decrease	44	Program 29
20	Brightness Increase	45	Program 30
21	Brightness Decrease	46	Program 31
22	Spare Increase	47	Program 32
23	Spare Decrease	48-255	Spare
24	Normalize		

*Decimal equivalent of 8 bit binary word is listed for convenience.

Command 'Outputs' appear approximately 120μs after the last bit of the 16 bit word has been input to the receiver. Analog commands may be up to a maximum of 180μs. For the case of Local commands the outputs appear approximately 16μs after the 20ms debounce strobe. Analog commands may be up to a maximum of 70μs.

Analog Outputs

The Analog outputs are variable mark space ratio outputs at a frequency of typically 20kHz. The mark space ratio defines the analog level and can be varied from 1:62 to 62:1. Power on reset sets the outputs to mark space of 32:31. Analog outputs 2 to 4 can also be set to 32:31 with the Normalize command. Analog output 1 (Volume) can be muted.

Remote commands cause analog channels to increment or decrement at the transmitter repetition rate. For local commands the rate will be approximately ten steps per second.

Local Commands

Local Command Strobe input low converts I/O's A-H to input mode and after a debounce period of 20ms the local data is read in, decoded, and Data Available set to high. Input data must be 'valid' during the strobe time shown.

Local Command Strobe high outputs this new data on the I/O lines.

Analog functions decrement or increment approximately once every 100ms while the command is input.

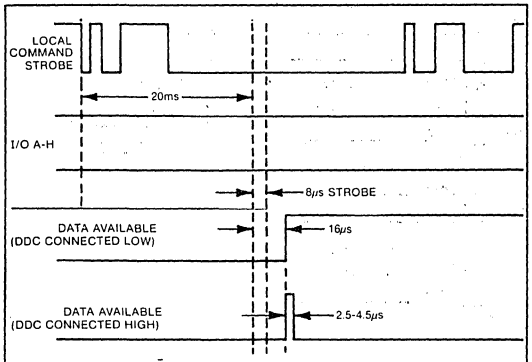


Fig. 2 LOCAL COMMAND TIMING

Program Strobe Output Timing

For the case where the Program Strobe I/O is not connected low externally, then on reception of a Program Command the strobe output will go low for approximately 50ms.

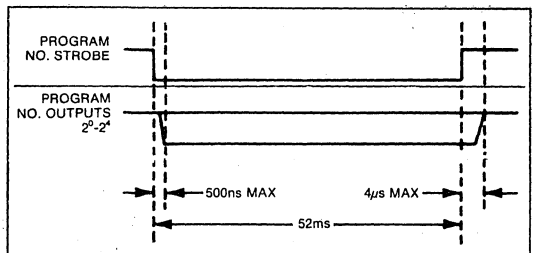


Fig. 3 PROGRAM STROBE TIMING

Interface with CPU Databus

The receiver interfaces directly with the General Instrument Teleview System, Teletext and Viewdata. Interface with any CPU is possible however.

(a) Remote Control has exclusive use of the data bus. Data Available I/O and Digital Data Control input are connected together. Data Available high signals the CPU, the CPU reads in the data and then pulls Data Available and Digital Data Control input low for a minimum of 3μs. Data Available is now reset low. If the CPU does not reply to the Data Available the next remote command received will reset Data Available low and then back again to high.

(b) The remote control outputs share a databus with other peripherals. Data Available to high signals the CPU, the CPU sets the Digital Data Control Input high which outputs the remote control data onto the bus. Data is now read and then the CPU resets Digital Data Control Input low which resets Data Available to low. If the CPU does not reply then the next remote transmission resets Data Available back to low and then high.

(c) With Digital Data Control input held high, Data is output on the bus permanently. At each command Data Available pulses high to act as a strobe for loading auxiliary latches.

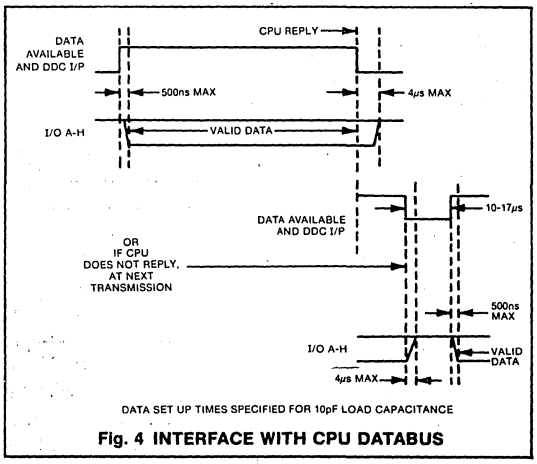


Fig. 4 INTERFACE WITH CPU DATABUS

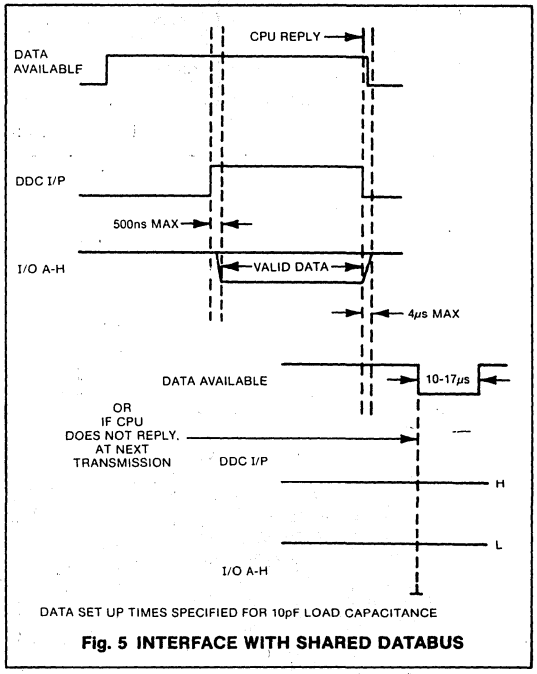


Fig. 5 INTERFACE WITH SHARED DATABUS

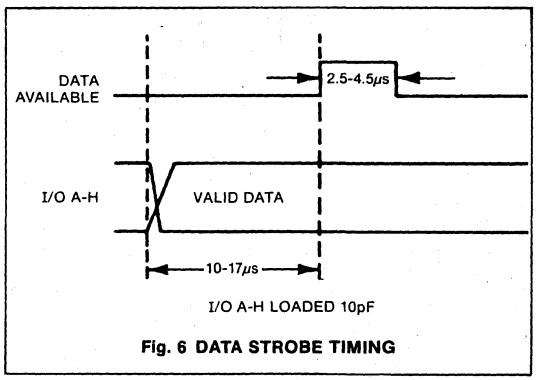


Fig. 6 DATA STROBE TIMING

ENTERTAINMENT

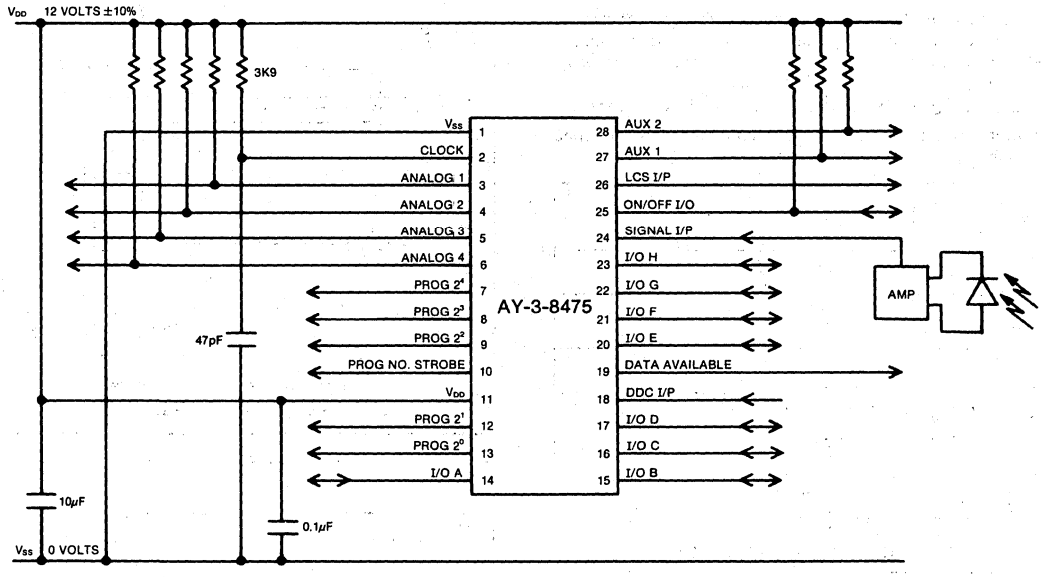


Fig. 7 BASIC SYSTEM SCHEMATIC

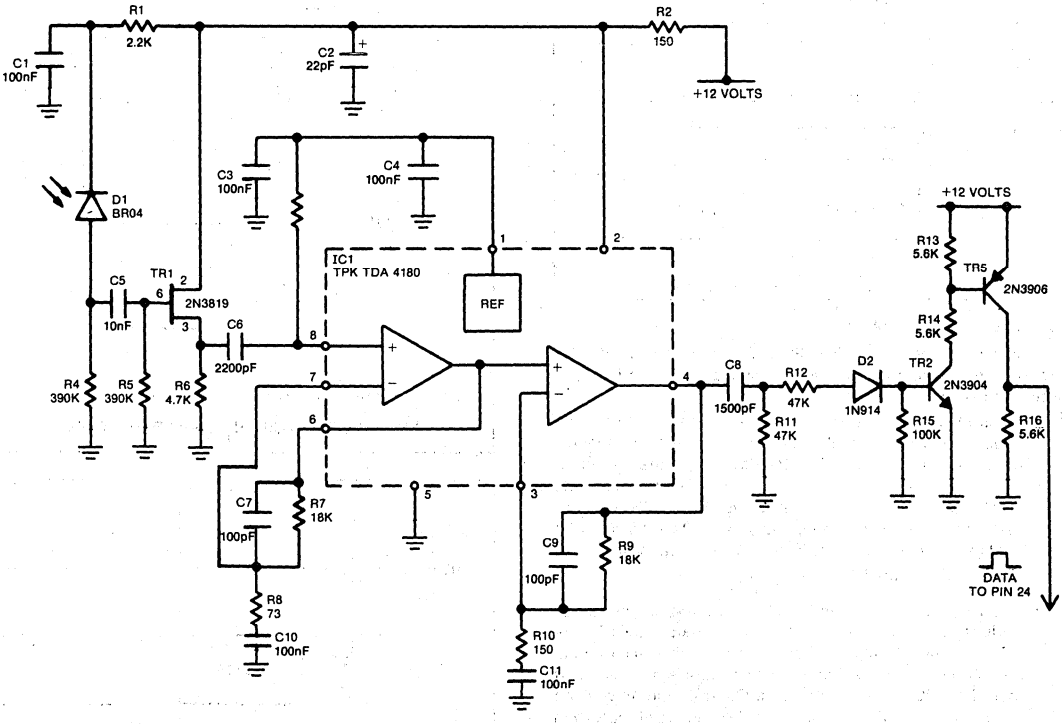


Fig. 8

ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... −3.0 to +16 Volts
Ambient operating temperature range ..... 0°C to +70°C
Storage temperature range ..... −65°C to +150°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{DD} = +12 Volts ±10% (10.8 to 13.2)
V_{SS} = 0 Volts
Operating temperature T_A = 0°C to +70°C

Characteristic	Min	Typ	Max	Units	Conditions
Clock (2)					
Frequency	1.875	2.5	3.125	MHz	±10% External components at typical values
External resistor to V_{DD}	1.0	3.9	—	KΩ	
External capacitor to V_{SS}	—	47	250	pF	
Digital Data Control (18) and Local Command Strobe (26) Inputs					
Low Level	V_{SS}	—	0.8	V	
High Level	2.0	—	V_{DD}	V	
Pull up to V_{DD}					
Low Level Source	—	—	200	μA	V_{IN} = 0.4 Volts
High Level	2.4	—	—	V	I_{SOURCE} = 30μA
Signal Input (24)					
Low Level	V_{SS}	—	0.8	V	
High Level	2.0	—	V_{DD}	V	
Leakage to V_{SS}	—	—	10	μA	$V_{IN} = V_{DD}$
Input/Output A-H (14-17 and 20-23)					
Input Low Level	V_{SS}	—	0.8	V	
Input High Level	2.0	—	V_{DD}	V	
Pull up to V_{DD}					
Low Level Source	—	—	200	μA	V_{IN} = 0.4 Volts
High Level	2.4	—	—	V	I_{SOURCE} = 30μA
Output Low Level	—	—	0.4	V	I_{SINK} = 2.0mA
Output High Level	As above Pull Up High Level				
Program No Outputs (7-9 and 12, 13)					
Low Level	—	—	0.4	V	I_{SINK} = 2mA
High Level	2.4	—	—	V	I_{SOURCE} ± 30μA
Outputs 'OFF' Pull Up to V_{DD}					
Low Level Source	—	—	200	μA	V_{IN} = 0.4 Volts
High Level	As above Output High Level				
Program No Strobe I/O (10)					
Input Low Level	V_{SS}	—	0.8	V	
Input High Level	3.0	—	V_{DD}	V	
Pull up to V_{DD}					
Low Level Source	—	—	200	μA	V_{IN} = 0.4 Volts
High Level	8	—	—	V	I_{SOURCE} = 30μA
Output Low Level	—	—	0.4	V	I_{SINK} = 2mA
Output High Level	As above Pull Up High Level				
Strobe Duration	40	52	70	ms	
Analog Outputs (3-6)					Open Drain
Frequency	15	20	25	kHz	
Low Level	—	—	0.4	V	I_{SINK} = 2mA
OFF Leakage to V_{SS}	—	—	10	μA	$V_{OUT} = V_{DD}$
Data Available Output (19)					
Low Level	—	—	0.4	V	I_{SINK} = 2mA
High Level	2.4	—	—	V	I_{SOURCE} = 30μA
Aux 1 and Aux 2 Outputs (27, 28)					Open Drain
Low Level	—	—	0.4	V	I_{SINK} = 2mA
OFF Leakage to V_{SS}	—	—	10	μA	$V_{OUT} = V_{DD}$
ON/OFF I/O (25)					
Input Low Level	V_{SS}	—	0.8	V	
Input High Level	3.0	—	V_{DD}	V	
Output Low Level	—	—	0.4	V	I_{SINK} = 2mA
OFF Leakage to V_{SS}	—	—	10	μA	$V_{OUT} = V_{DD}$
Supply Current V_{DD} (11)	—	—	40	mA	

NOTE: 'Pull Ups' are configured with Depletion FET's with Gate connected to Source. They have non-linear VI characteristics.

ENTER-TAINMENT

PIN FUNCTIONS

Pin No.	Name	Function
1	V_{SS}	0 Volts. Source/substrate connection.
2	Clock	Connect a resistor to V_{DD} and a capacitor to V_{SS}. Nominal frequency 2.5MHz.
3 4 5 6	Analog Output 1 Analog Output 2 Analog Output 3 Analog Output 4	Open drain pulse width modulated outputs. Mark space ratio variable from 1:62 to 62:1. Outputs increment one step for each command received. Increment rate approximately one step every 100ms for continuous commands.
7 8 9 12 13	2^4 Program No Output 2^3 Program No Output 2^2 Program No Output 2^1 Program No Output 2^0 Program No Output	Outputs under control of the Program StrobeI/O. Program 1 = 00000. With Program StrobeI/O connected low, latched program data is available.
10	Program Number StrobeI/O	Goes low for approximately 50ms when program data has been received. While low the Program Number Outputs are enabled. While high the Program Number outputs are all high. When this output is held low externally the Program Number outputs are permanently enabled.
11	V_{DD}	Positive power supply 12 Volts ±10%.
14 15 16 17 20 21 22 23	I/O A I/O B I/O C I/O D I/O E I/O F I/O G I/O H	256 Command data under the control of the Digital Data Control input. A is the LS Bit. Local commands may be entered on the A-H lines under control of the Local Command Strobe Input.
18	Digital Data Control Input	When high the 8 outputs A-H are enabled. This input also resets the Data Available output when taken low. When low outputs A-H are all high.
19	Data Available Output	This output is set high when new data is available. It remains high until reset by the Digital Data Control input going low. If the Digital Data Control input is permanently held high then Data Available output is a high going strobe pulse of typically 4μs.
24	Signal Input	This input should normally be low under no signal conditions. High going pulses are input when a remote command is triggered.
25	ON/OFFI/O	Open drain output used for switching 'ON' the television or radio, etc. This output is turned on by any one of the 32 program commands and turned off by the OFF command. The output can be latched on locally by connecting low for at least 128μs. When 'OFF' increment and decrement commands on the Analog channels are inhibited. Connect to 0 volts if not used.
26	Local Command Strobe Input	When low, I/O's A-H are in the input mode and the Signal Input is inhibited. Local commands may now be entered. When high are under control of the Digital Data Control input.
27 28	Auxiliary Output 1 Auxiliary Output 2	Open drain outputs, turned on or off as required. In addition Auxiliary Output 1 can be toggled. Remote toggle commands have to be spaced at least 0.5 secs apart similar to the Mute toggle, see later Muting.

Sound Generation

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
TOP OCTAVE GENERATORS	Generates a complete octave of musical frequencies.	AY-1-0212	7-72
		AY-3-0214	7-74
		AY-3-0215	7-74
LATCHING NETWORK	Establishes priority of 13 pedal latch inputs/outputs.	AY-1-1313	7-76
CHORD GENERATOR	Produces major, minor, 7th chords, walking bass.	AY-5-1317A	7-78
PIANO KEYBOARD	Electronically simulates piano keyboard operation.	AY-1-1320	7-82
FREQUENCY DIVIDERS	7 stage dividers.	AY-1-5050	7-86
PROGRAMMABLE SOUND GENERATORS	Generates programmable sound effects via a microcomputer compatible bus without the aid of external components.	AY-3-8910	7-88
		AY-3-8912	7-88
MICROCOMPUTER TUNES SYNTHESIZER	Produces musical tunes from pre-programmed microcomputer.	AY-3-1350	7-95

Top Octave Generators

FEATURES

- Wide Input Frequency Range. 250kHz to 1.5MHz
- Low Impedance Push-Pull Outputs
- Full Musical Scale In One Chip
- Zener Protected Input

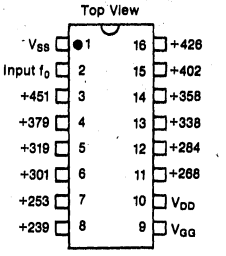
DESCRIPTION

The AY-1-0212 Top Octave Generator is a digital tone generator which produces, from a single input frequency, a full octave of twelve frequencies on twelve separate output terminals.

The AY-1-0212 consists of twelve divider circuits which divide the input by an exact integer to produce a chromatic scale of twelve notes. When used in conjunction with an oscillator and frequency dividers, a system may be configured which generates all the frequencies required by an electronic music synthesizer.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



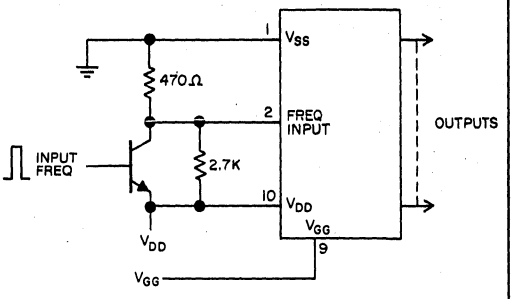
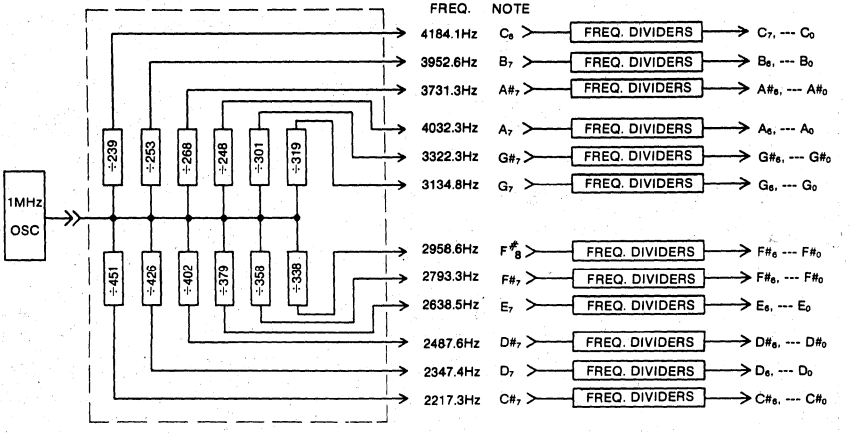


Fig. 1 TYPICAL INPUT BUFFER (IF REQUIRED)

ENTER-TAINMENT

BLOCK DIAGRAM / TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Voltages with respect to Vss .....-30V to +0.3V
Storage Temperature .....-55°C to +150°C
Operating Temperature (T_A) .....0°C to +70°C

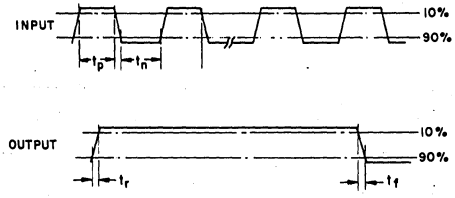
*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

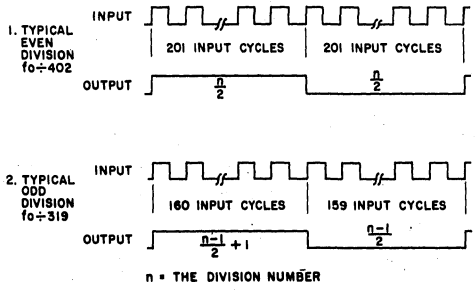
Standard Conditions (unless otherwise noted)
V_{SS} = GND
See Fig. 2 for V_{DD} and V_{GG} Operating Voltages

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Leakage	—	—	10	μA	at 27V
Input Positive Level	+0.3	—	−2.0	Volts	
Input Negative Level	−10.0	—	V_{DD}	Volts	
Output on Impedance to V_{DD}	—	—	3500	Ω	} 1.0V across the device with 17K load
Output on Impedance to V_{SS}	—	—	3500	Ω	} to -6V.
I_{GG} Supply Current	—	—	16	mA	
I_{DD} Supply Current	—	—	20	mA	
AC CHARACTERISTICS					
Input Frequency f_0	.25	—	1.5	MHz	See Fig. 3
Input Capacitance	—	5	10	pF	1MHz
Input Positive Level Width t_p	.33	—	—	μs	AY-1-0212
Input Negative Level Width t_n	.33	—	—	μs	AY-1-0212
Output Rise Time t_r	—	1	—	μs	no load
Output Fall Time t_f	—	1	—	μs	no load

** Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS





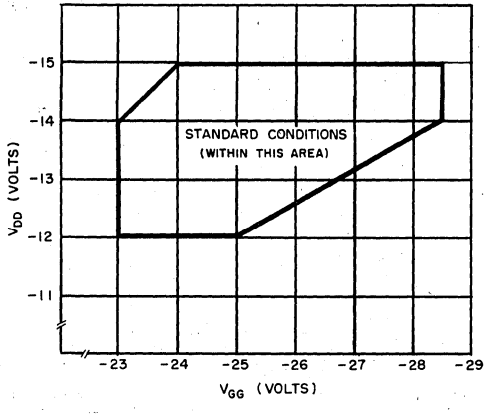


Fig. 2 OPERATING VOLTAGES

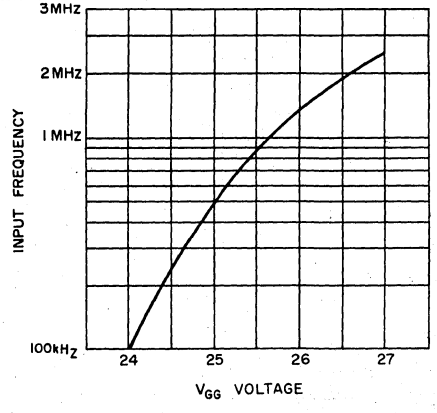


Fig. 3 TYPICAL FREQUENCY vs. V_{GG} VOLTAGE OPERATION

ENTER-TAINMENT

Master Frequency Generator/Top Octave Generator

FEATURES

- Wide input frequency range: 100kHz to 4.5MHz
- Single power supply
- Full musical scale on one chip
- Low impedance push-pull outputs
- Zener protected input
- AY-3-0214: 12 outputs — 50% Duty Cycle (Highest accuracy)
- AY-3-0215: 13 outputs — 50% Duty Cycle

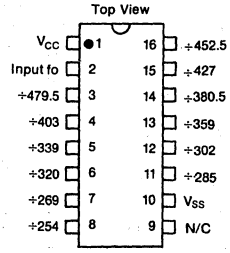
DESCRIPTION

The General Instrument M.F.G./T.O.G. is a digital tone generator which produces, from a single input frequency, 12 or 13 semitone outputs fully spanning the equal tempered scale. When used in conjunction with an oscillator and frequency dividers such as the General Instrument AY-1-5050, a system may be configured which generates all the frequencies required by an electronic music synthesizer.

PIN CONFIGURATION

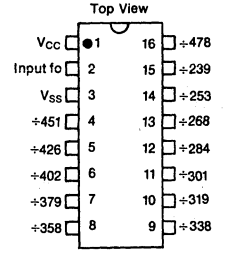
16 LEAD DUAL IN LINE

AY-3-0214



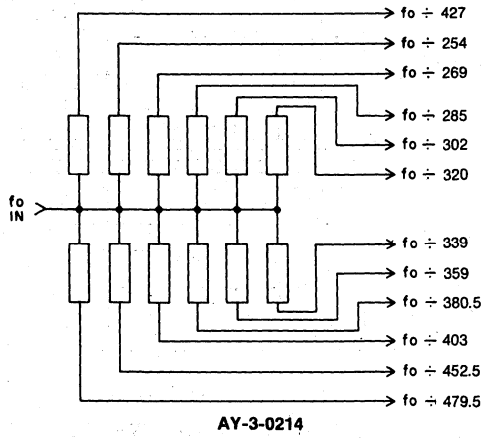
16 LEAD DUAL IN LINE

AY-3-0215

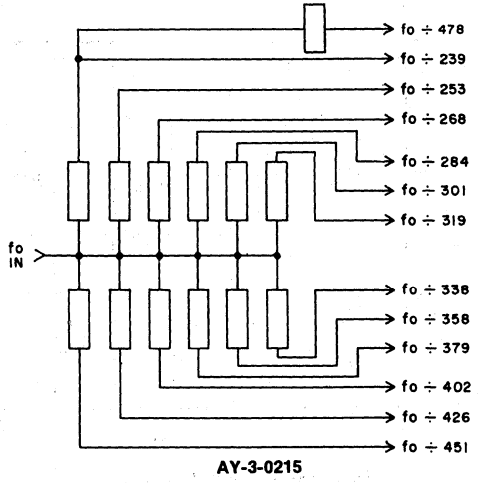


ENTER-TAINMENT

BLOCK DIAGRAMS



AY-3-0214



AY-3-0215

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... +20 to -0.3
Storage Temperature .....-55°C to +150°C
Operating Temperature (T_A) .....0°C to +50°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = GND
V_{CC} = +10V to +16V

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input					
Low	0.0	—	0.8	V	
High	V_{CC} −3.0	V_{CC}	V_{CC}	V	
Frequency	100	—	4500	kHz	
Rise Time	—	—	30	ns	4.5MHz
Fall Time	—	—	30	ns	4.5MHz
Duty Cycle	40	50	60	%	
Capacitance	—	—	10	pF	
Outputs					
High	V_{CC} −1.5	—	V_{CC}	V	0.25mA
Low	0.0	—	0.5	V	0.7mA
Fall Time	—	—	2.5	μs	20K & 500 pF to 16V
Rise Time	—	—	2.5	μs	20K & 500 pF to V_{SS} when V_{CC}=16V
Duty Cycle	—	50	—	%	
Supply current	—	—	120	mA	16V, 4.5MHz, 25°C

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS

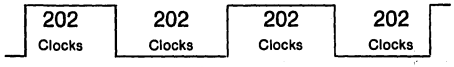


Fig.1 TYPICAL EVEN DIVISOR N = 404

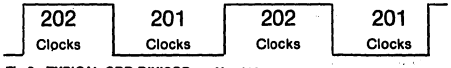


Fig.2 TYPICAL ODD DIVISOR N = 403

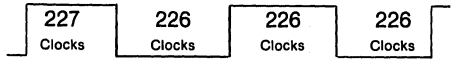
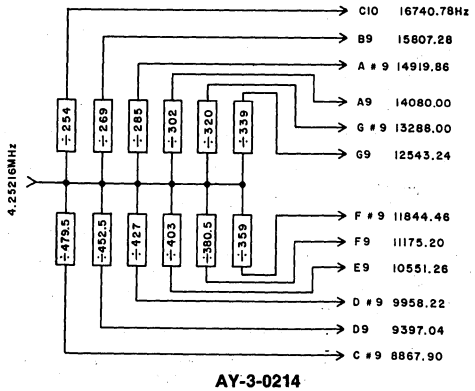


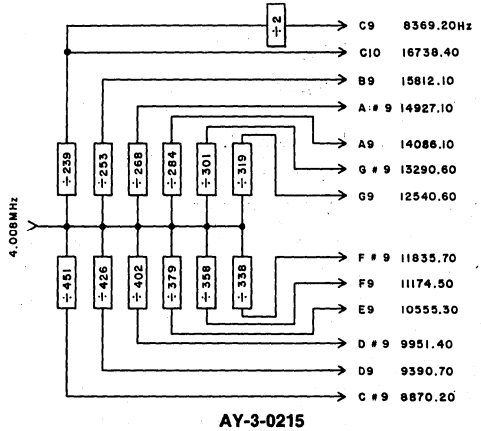
Fig.3 TYPICAL EVEN PLUS 0.5 DIVISOR N = 452.5

Fig.4 TYPICAL ODD PLUS 0.5 DIVISOR N = 479.5

TYPICAL APPLICATIONS



AY-3-0214



AY-3-0215

ENTER-TAINMENT

Priority Latching Network

FEATURES

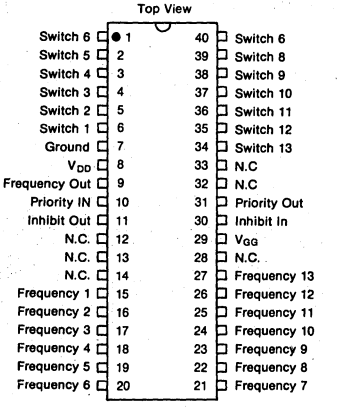
- Low Power Consumption
- Two or more units may be connected in tandem

DESCRIPTION

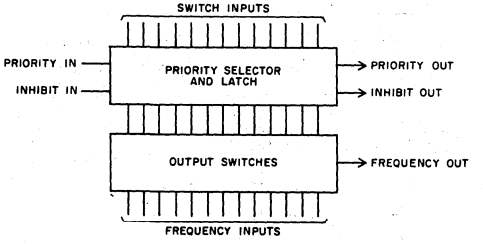
The AY-1-1313 Priority Latching Network is a LSI subsystem designed for use in electronic organ keyboard and pedal latching circuits. When any combination of one or more "switch" inputs is connected to logic "1" the output switch corresponding to the highest priority, or lowest number, input will close, connecting the selected frequency to the output frequency bus. The output switch will remain closed even if the input switch is released, and will remain closed until a new input switch closure occurs.

PIN CONFIGURATION

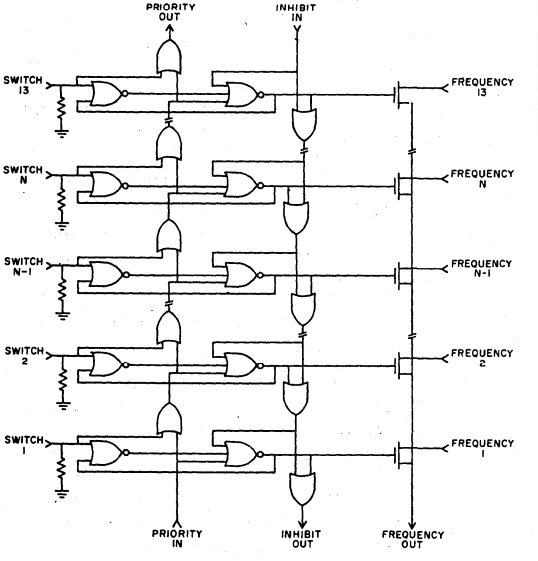
40 LEAD DUAL IN LINE



BLOCK DIAGRAM



LOGIC DIAGRAM



ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Voltages with respect to V_{SS} .....-30V to +0.3V
Storage Temperature .....-55°C to +150°C
Operating Temperature (T_A) .....-20°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

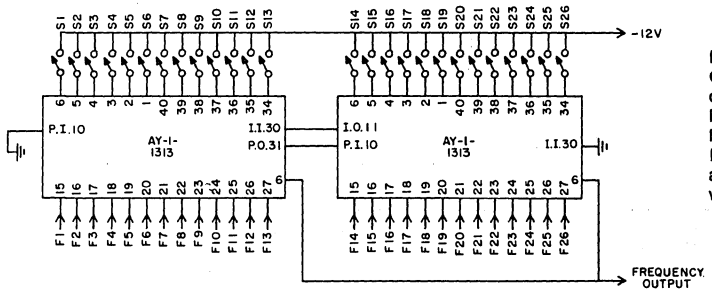
Standard Conditions (unless otherwise noted)

V_{DD} = -12±1V
V_{GG} = -27±1.5V
V_{SS} = GND

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Switch Inputs Impedance	15	—	80	kΩ	Measured to Ground
Priority and Inhibit Inputs Impedance	1	—	—	MΩ	Measured to Ground
Input Logic "0"	—	—	-2	V	
Input Logic "1"	-9	—	—	V	
Output Logic "0"	—	—	-2	V	R_L = 47K to V_{DD}
Output Logic "1"	-9	—	—	V	R_L = 47K to V_{DD}
Frequency Output Switch					
Impedance — "ON"	—	—	20	kΩ	
"OFF"	5	—	—	MΩ	
I_{DD} Supply Current	—	—	8	mA	
I_{GG} Supply Current	—	—	1	mA	

**Typical values are at +25°C and nominal voltages.

TYPICAL APPLICATION



For multiple unit operation, the Priority Output of the higher priority unit is connected to the Priority Input of the lower, and the Inhibit Input of the higher priority unit is connected to the Inhibit Output of the lower. The Priority and Inhibit Inputs must be grounded when not in use.

ENTER-TAINMENT

Chord Generator

FEATURES

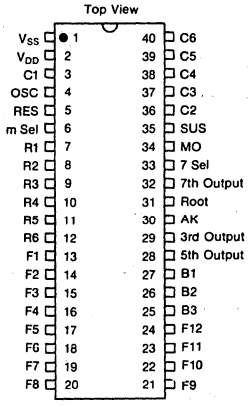
- ROOT, 3rd, 5th, 7th Chord Elements
- Additional output for special effects
- Sustain capability
- Top key priority
- Self-contained oscillator circuit
- Operated with single pole, single throw switch matrix

DESCRIPTION

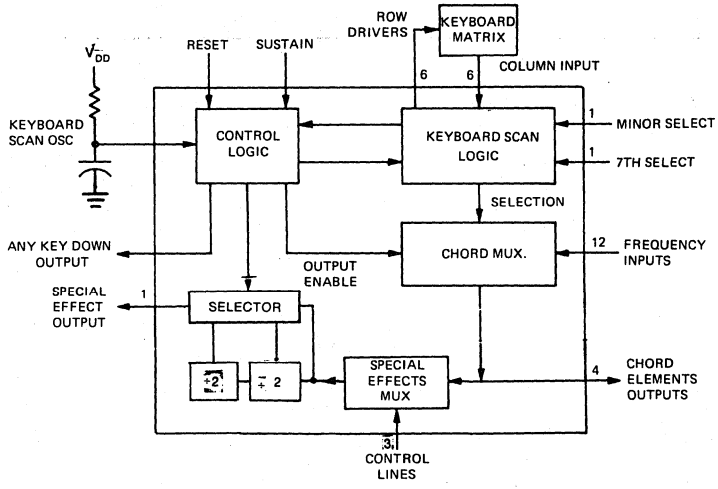
The AY-5-1317A is a P-Channel MOS IC which accepts twelve basic frequencies (one full octave) and outputs the notes necessary to form Major, Minor and Seventh chords. This is the only known standard chord generator IC that performs these functions. The chord elements (ROOT, 3rd, 4th, 5th, 6th, and 7th) can be multiplexed internally to perform special effects such as walking bass, rhythm arpegio, alternating bass, etc. The AY-5-1317A will operate in conjunction with and, through the KEY DOWN output, synchronize a rhythm generator such as the General Instrument AY-5-1315. The AY-5-1317A has a keyboard priority system with the C Major chord having the highest priority.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



ENTER-TAINMENT

PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	Ground (Vss)	Ground
2	Power Supply (V_{DD})	Negative Supply
3, 36-40	Column Inputs (C1-C6)	Column inputs from Keyboard Matrix
4	Oscillator Input (OSC)	R/C network connection for keyboard scan oscillator
5	Reset (RES)	A logic '1' (ground) will reset the keyboard scanner, and the memorized key
6	Minor Select (m Sel)	A Ground on this line changes the 3rd output from Major to Minor
7-12	Row Outputs (R1-R6)	Row outputs to Keyboard Matrix
13-24	Frequency Inputs (F1-F12)	These are the input lines for the 12 frequencies (one full octave B thru C) used to generate the chords.
25-27	Control Inputs (B3-B1)	These 3 lines will be internally latched and decoded to select either the ROOT, 3rd, 4th, 5th, 6th, or 7th frequency as the special effect output.
28	5th Output (5th)	This line will output the 5th frequency element of the selected chord.
29	3rd Output (3rd)	This line will output the 3rd frequency element of the selected chord. Minor 3rd will be provided if a Minor chord is selected. Major 3rd will be provided if a Major or 7th chord is selected.
30	Any Key Down (AK)	This line goes to a logic '1' whenever a chord selection key is depressed.
31	Root Output (Root)	This line will output the ROOT frequency element of the selected chord.
32	7th Output (7th)	This line will output the 7th frequency element of the selected chord if a 7th chord is selected otherwise the output is logic '0' (voltage).
33	7th Select (7 Sel)	A ground on this line turns the 7th output on.
34	Special Effect Output (MO)	This line will output one of the six frequency elements as programmed by the control lines B1-B3. The 7th chord element frequency will be provided independently of the chord selection.
35	Sustain (SUS)	A logic '1' on this line will activate the memory circuit which memorizes the last key played.

B1	B2	B3	Selection
0	0	0	No change from last selection.
0	0	1	ROOT
0	1	0	5th
0	1	1	3rd
1	1	1	7th
1	1	0	4th
1	0	1	6th

TRUTH TABLE FOR SPECIAL EFFECT OUTPUT

FREQUENCY OUTPUTS

Chord Selection	Root	3rd Minor	3rd Major	4th	5th	6th	7th
C	C (÷2)	D# (÷2)	E (÷2)	F (÷2)	G (÷2)	A (÷2)	A# (÷2)
C#	C# (÷2)	E (÷2)	F (÷2)	F# (÷2)	G# (÷2)	A# (÷2)	B (÷2)
D	D (÷2)	F (÷2)	F# (÷2)	G (÷2)	A (÷2)	B (÷2)	C (÷1)
D#	D# (÷2)	F# (÷2)	G (÷2)	G# (÷2)	A# (÷2)	C (÷1)	C# (÷1)
E	E (÷2)	G (÷2)	G# (÷2)	A (÷2)	B (÷2)	C# (÷1)	D (÷1)
F	F (÷2)	G# (÷2)	A (÷2)	A# (÷2)	C (÷1)	D (÷1)	D# (÷1)
F#	F# (÷4)	A (÷4)	A# (÷4)	B (÷4)	C# (÷2)	D# (÷2)	E (÷2)
G	G (÷4)	A# (÷4)	B (÷4)	C (÷2)	D (÷2)	E (÷2)	F (÷2)
G#	G# (÷4)	B (÷4)	C (÷2)	C# (÷2)	D# (÷2)	F (÷2)	F# (÷2)
A	A (÷4)	C (÷2)	C# (÷2)	D (÷2)	E (÷2)	F# (÷2)	G (÷2)
A#	A# (÷4)	C# (÷2)	D (÷2)	D# (÷2)	F (÷2)	G (÷2)	G# (÷2)
B	B (÷4)	D (÷2)	D# (÷2)	E (÷2)	F# (÷2)	G# (÷2)	A (÷2)

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} with respect to V_{SS} . . . . . −20V to +0.3V
Logic Input Voltages with respect to V_{SS} . . . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied —operating ranges are specified below.

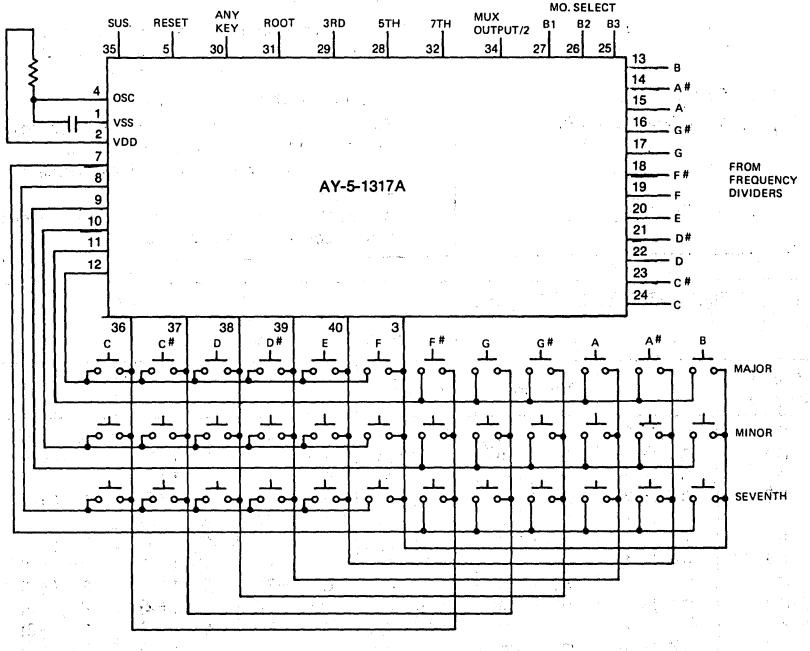
Standard Conditions (unless otherwise noted)

$V_{DD} = -15V \pm 3V$
$V_{SS} = 0V$ (substrate voltage)
Operating Temperature (T_A) = +25°C

Characteristic	Sym	Min	Typ**	Max	Conditions
Input Logic Levels					
Logic 0	VIL	V_{DD}	—	−8.5V	
Logic 1	VIH	−1.0V	—	+0.3V	
Input Capacitance	CIN	—	—	10 pF	
Note Outputs					
Logic 0	R_{OFF}	160kΩ	—	—	
Logic 1	R_{ON}	—	—	500Ω	
Row Drivers Output Impedance		—	750Ω	—	$V_{DD} = -15V$
Control Input		10kΩ	—	1000kΩ	
Keyboard Row Input Impedance		24kΩ	—	100kΩ	
Keyboard Scan Frequency		—	25kHz	—	500 pF, 750KΩ, $V_{DD} = -15V$

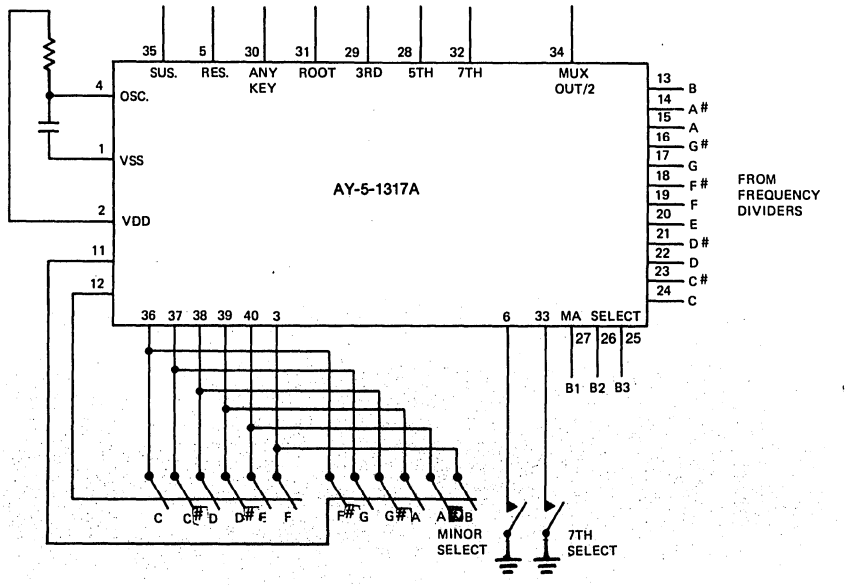
**Typical values are at +25°C and nominal voltages.

STANDARD INTERCONNECTION FOR A 3 x 12 KEY MATRIX



ENTER-TAINMENT

STANDARD INTERCONNECTION FOR A SINGLE ROW KEYBOARD WITH SEPARATE KEY FOR MINOR AND SEVENTH



Piano Keyboard Circuit

FEATURES

- 12 keys per package
- Loudness proportional to key press velocity
- Sustain input to give loud pedal operation

DESCRIPTION

The electronic piano chip when used in conjunction with standard divider circuits will make an instrument closely resembling a piano in operation and sound. The chip is arranged so that the loudness of the notes is proportional to the velocity of the keys as in an acoustical instrument. Additionally the notes are arranged to die away at a realistic rate. A sustain input is provided so that the operation of the loud pedal can be emulated.

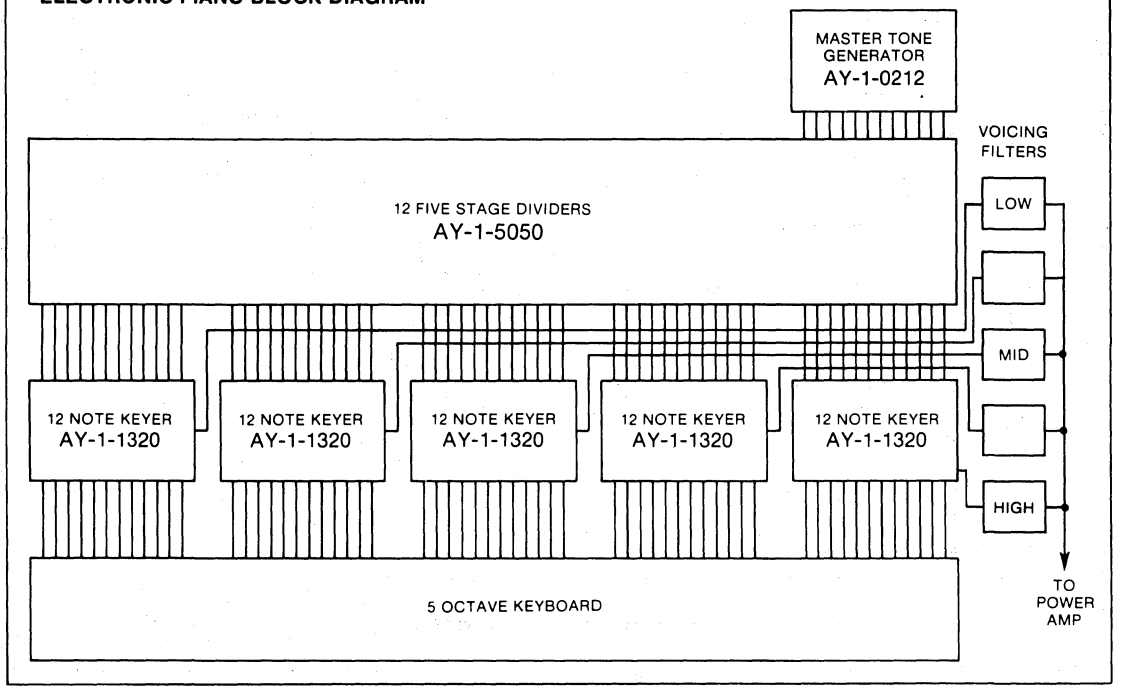
PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View

V_{SS} (GND)	1	40	Key 9 Input
Key 11 Input	2	39	Key 10 Input
Output 11	3	38	Key 12 Input
C1/11	4	37	Output 12
Output 9	5	36	C1/12
C1/9	6	35	Output 10
Output 7	7	34	C1/10
C1/7	8	33	Output 8
Key 7 Input	9	32	C1/8
Output 5	10	31	Key 8 Input
C1/5	11	30	Output 6
Key 5 Input	12	29	C1/6
Output 3	13	28	Key 6 Input
C1/3	14	27	Output 4
Output 1	15	26	C1/4
V_{GG}	16	25	Output 2
C1 1	17	24	C1/2
Sustain Input	18	23	Key 2 Input
Bias Input	19	22	Key 4 Input
Key 1 Input	20	21	Key 3 Input

ELECTRONIC PIANO BLOCK DIAGRAM



ENTER-TAINMENT

PIN FUNCTIONS

Name	Function
V_{SS}	Positive supply
V_{GG}	Negative supply (-25 to -29V)
$V_{BIAS\ 1}$	Bias supply to keying circuit (-27V nominal)
Sustain	When a logic '1' the outputs are damped with a time constant of 180 msec when the key is released. This input simulates the action of the loud pedal in a piano.
Key Inputs (1-12)	These inputs are switched from logic '0' to logic '1' by a break before make change over switch. During the transit the input is held at an intermediate logic level. The transit time determines the initial output level.
C1 (1-12)	The capacitor C1 connected to this pin establishes the key velocity time constant. 0.5μF gives a time constant of 18 msec.
Output (1-12)	This output provides an exponentially decaying DC level proportional to the amplitude of the desired note. The capacitor C2 determines the damper time constant. The resistor R1 together with C2 determines the undamped decay time constant. The DC level is chopped by external frequency dividers to generate the note.

OPERATION

In the rest condition with the key up capacitor C1 is charged to -12 Volts. When the key is depressed C1 is first disconnected and it starts to discharge through the 39K resistor with a time constant of 18 msec. And the end of the key travel the final voltage on C1 is transferred to the gate of T3 via T2. This causes C2 to be charged to V_{C1} + 4 Volts. The faster the key depression the larger the initial voltage on C2 and the louder the note.

The DC voltage on C2 is chopped via R1 and the divider circuit and the resulting square wave is fed to the voicing circuits and amplifiers. C2 slowly discharges through R1 to give the required exponential decay of note amplitude. When the key is released the 50K damping resistor is optionally connected across C2 to damp the notes with a 110 msec time constant.

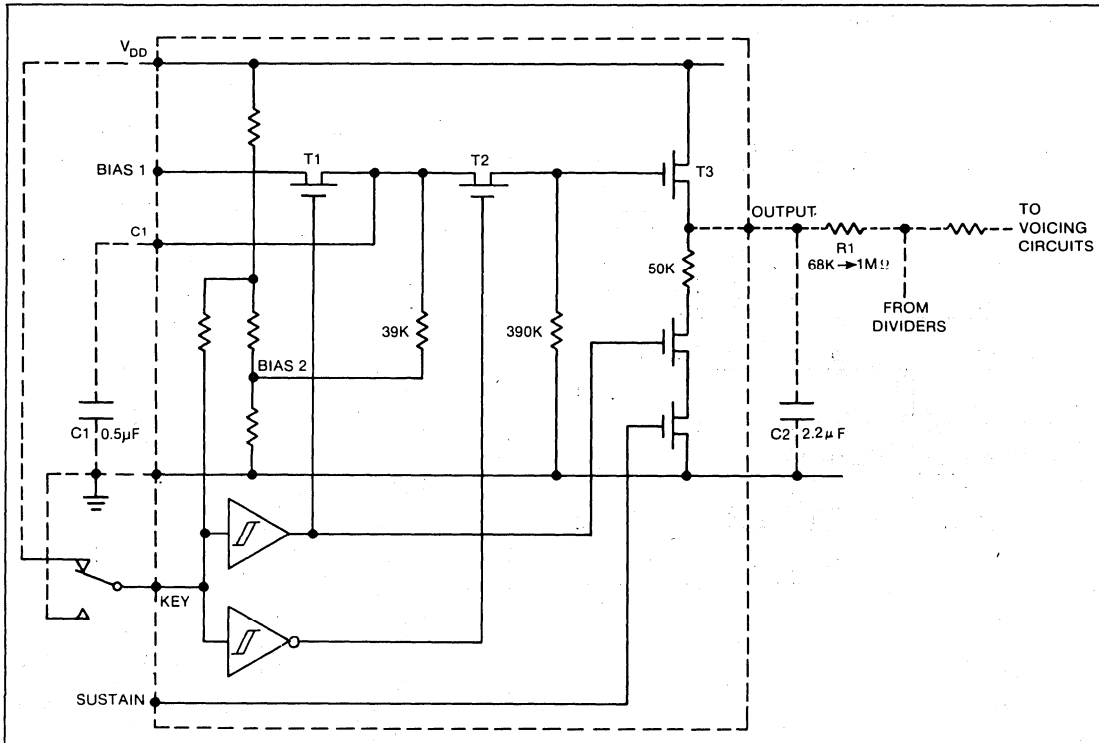


Fig.1 KEY CIRCUIT SCHEMATIC

ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... +0.3 to -30 Volts
Storage Temperature Range ..... -65°C to +150°C
Ambient Operating Temperature Range ..... 0°C to +70°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{GG} = -25 to -29 Volts
V_{SS} = 0V
$V_{BIAS\ 1} = V_{GG}$
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Min.	Typ**	Max	Units	Conditions
Key Input Logic '1'	-24	—	-29	V	Key up
Key Input Logic '0'	+0.3	—	-1	V	Key down
Key velocity time constant	—	18	—	ms	C1 = 0.5μF (Note 1)
Output peak amplitude	—	8	—	V p-p	(Note 2)
Output decay time constant	—	286-2486	—	ms	See Table 1
Damper time constant	—	110	—	ms	C2 = 2.2μF
Dynamic range	—	30	—	dB	
Power Supply Current I_{GG}	—	3	—	mA	
Power Supply Current I_{BIAS}	—	3	—	mA	

**Typical values are at +25°C and nominal voltages.

Note 1. The key transit time determines the initial amplitude of the note. The longer the time the softer the note. If the transit time is 18ms the amplitude will be approximately 37% of maximum. Capacitor C1 determines the time constant.

Note 2. This is the amplitude that would be obtained if the key transit time was zero.

Table 1 — TYPICAL COMPONENT VALUES/DECAY TIME
C2 = 2.2 μF Square wave chopper

Octave	R1 kΩ	R2 kΩ	Decay Time msec
C7-C6# 2093-1108Hz	68	470	286
C6-C5# 1046.4-554.2Hz	120	470	484
C5-C4# 523.2-277.1Hz	220	470	825
C4-C3# 261.6-138.6Hz	330	470	1155
C3-C2# 130.8-69.3Hz	680	470	1980
C2-C1# 65.4-43.6Hz	1000	470	2486

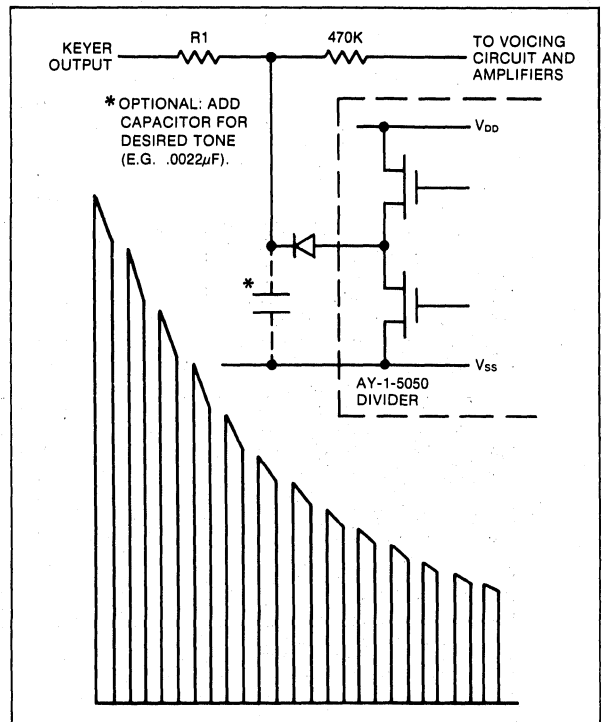


Fig.2 OUTPUT CIRCUIT AND WAVEFORMS

ENTER-TAINMENT

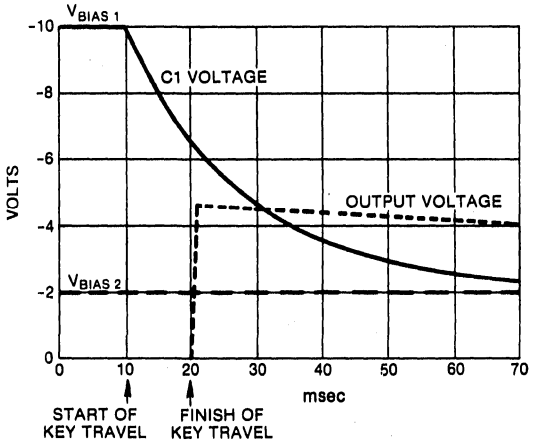


Fig.3 KEY VELOCITY WAVEFORMS

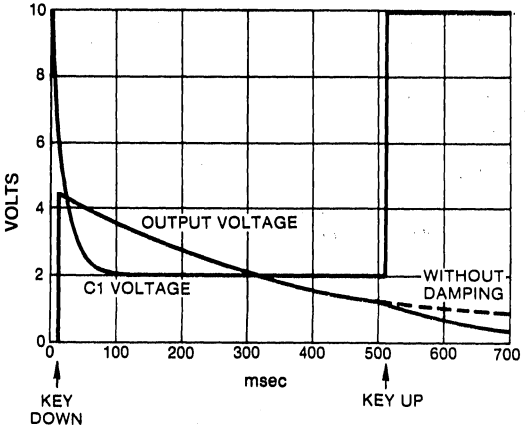


Fig.4 OUTPUT ENVELOPE DECAY WAVEFORM

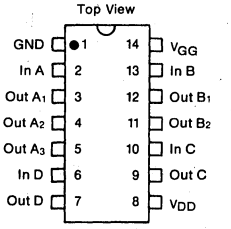
7-Stage Frequency Divider

FEATURES

- DC to 1 MHz operating frequency range
- Diode protection on all inputs
- Low output impedance in both states
- Configurations: 7-Stage Frequency Divider, 3+2+1+1

PIN CONFIGURATION

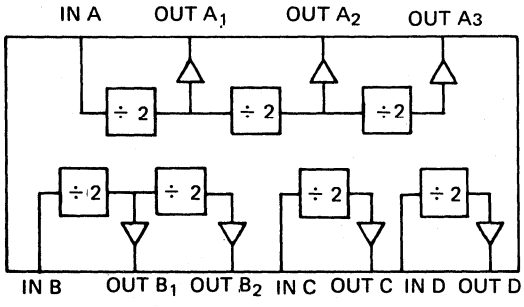
14 LEAD DUAL IN LINE



DESCRIPTION

The AY-1-5050, is constructed on a monolithic silicon chip using MTOS (Metal-Thick-Oxide-Silicon) P-Channel Enhancement Mode Field Effect Transistors. The inputs can be driven from a sine or square wave input.

BLOCK DIAGRAM



ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Drain Voltage	−30V to +0.3V
Gate Voltage	−30V to +0.3V
Data Input Voltage	−30V to +0.3V
Storage Temperature	−55°C to +150°C
Operating Temperature (T_A)	0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

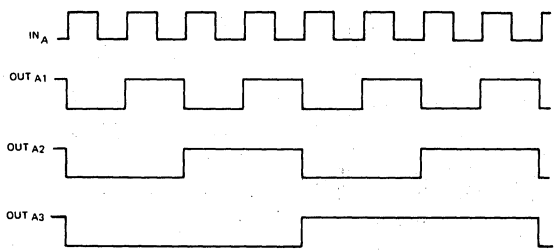
$V_{DD} = -13V \pm 1V$ $C_L = 10$ pF
$V_{GG} = -27V \pm 1V$ Operating Temperature (T_A) = +25°C
$R_L = 1M\Omega$

Characteristics	Min.	Typ**	Max	Units	Conditions
Data Input					
Logic "0" level	—	—	−2	V	
Logic "1" level	−10	—	—	V	
Data Input operating freq.	DC	—	1	MHz	Sine or square wave
Data Input Pulse width					
— "0" level	300	—	—	ns	
— "1" level	300	—	—	ns	
Input Leakage	—	—	5	μA	$V_{in} = -20VDC$
Output Parameters					
Logic "0" level	—	—	−1	V	
Logic "1" level	−11	—	—	V	
Drive Capability					
— "0" level	—	−1	−1.5	V	Sinking current = 0.5mA
— "1" level	−11	—	—	V	$R_L = 100K\Omega$.
— "1" level	−8	—	—	V	$R_L = 10K\Omega$.
Data output Rise and Fall time	—	0.6	—	μs	
Current Drain					
I_{GG}	—	3	—	mA	$V_{GG} = -27V$
I_{DD}	—	***	—		

**Typical values are at +25°C and nominal voltages.

*** V_{DD} is only used for the push-pull outputs therefore I_{DD} is equal to the sum of load currents. This separate V_{DD} enables tremulant to be introduced in the electronic organ application.

TIMING DIAGRAM



ENTER-TAINMENT

Programmable Sound Generator

FEATURES

- Full software control of sound generation
- Interfaces to most 8-bit and 16-bit microprocessors
- Three independently programmed analog outputs
- Two 8-bit general purpose I/O ports (AY-3-8910)
- One 8-bit general purpose I/O port (AY-3-8912)
- Single +5 Volt Supply

DESCRIPTION

The AY-3-8910/8912 Programmable Sound Generator (PSG) is a Large Scale Integrated Circuit which can produce a wide variety of complex sounds under software control. The AY-3-8910/8912 is manufactured in GI's N-Channel Ion Implant Process. Operation requires a single 5V power supply, a TTL compatible clock, and a microprocessor controller such as the GI 16-bit CP1600/1610 or one of GI's PIC 1650 series of 8-bit microcomputers.

The PSG is easily interfaced to any bus oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signalling and FSK modems. The analog sound outputs can each provide 4 bits of logarithmic digital to analog conversion, greatly enhancing the dynamic range of the sounds produced.

In order to perform sound effects while allowing the processor to continue its other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one effect is satisfied by the three independently controllable channels available in the PSG.

All of the circuit control signals are digital in nature and intended to be provided directly by a microprocessor/microcomputer. This means that one PSG can produce the full range of required sounds with no change in external circuitry. Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction with only the simplest electrical connections.

Since most applications of a microprocessor/PSG system would also require interfacing between the outside world and the microprocessor, this facility has been designed into the PSG. The AY-3-8910 has two general purpose 8-bit I/O ports and is supplied in a 40 lead package; the AY-3-8912 has one port and 28 leads.

ENTER-TAINMENT

PIN FUNCTIONS

DA7--DA0 (input/output/high impedance): pins 30--37 (AY-3-8910)
Data/Address 7--0: pins 21--28 (AY-3-8912)

These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG and to receive data from the PSG. In the data mode, DA7--DA0 correspond to Register Array bits B7--B0. In the address mode, DA3--DA0 select the register # ($0--17_8$) and DA7--DA4 in conjunction with address inputs $\overline{A9}$ and A8 form the high order address (chip select).

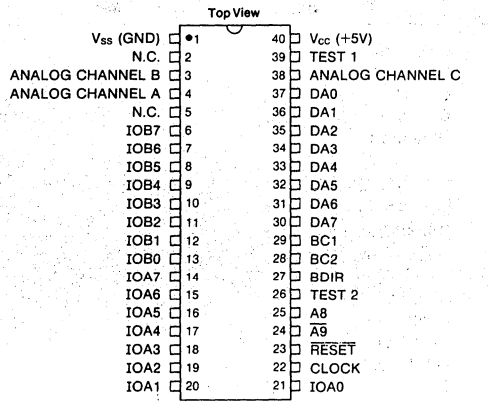
A8 (input): pin 25 (AY-3-8910)
pin 17 (AY-3-8912)
$\overline{\textbf{A9}}$ (input): pin 24 (AY-3-8910)
(not provided on AY-3-8912)

$\overline{\text{Address 9}}$, Address 8

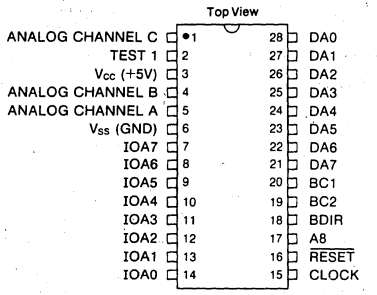
These "extra" address bits are made available to enable the positioning of the PSG (assigning a 16 word memory space) in a total 1,024 word memory area rather than in a 256 word memory area as defined by address bits DA7--DA0 alone. If the memory size does not require the use of these extra address lines they may be left unconnected as each is provided with either an on-chip pull down ($\overline{A9}$) or pull-up (A8) resistor. In "noisy" environments, however, it is recommended that $\overline{A9}$ and A8 be tied to an external ground and +5V, respectively, if they are not to be used.

PIN CONFIGURATIONS

40 LEAD DUAL IN LINE
AY-3-8910



28 LEAD DUAL IN LINE
AY-3-8912



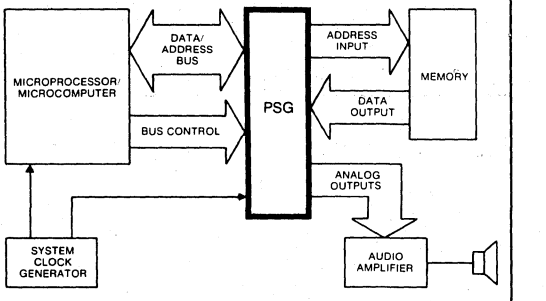


Fig. 1 SYSTEM BLOCK DIAGRAM

RESET (input): pin 23 (AY-3-8910)
pin 16 (AY-3-8912)

For initialization/power-on purposes, applying a logic "0" (ground) to the Reset pin will reset all registers to "0". The Reset pin is provided with an on-chip pull-up resistor.

CLOCK (input): pin 22 (AY-3-8910)
pin 15 (AY-3-8912)

This TTL-compatible input supplies the timing reference for the Tone, Noise and Envelope Generators.

BDIR, BC2, BC1 (inputs): pins 27,28,29 (AY-3-8910)
pins 18,19,20 (AY-3-8912)

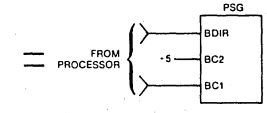
Bus DIRection, Bus Control 2,1

These bus control signals are generated directly by GI's CP1600 series of microprocessors to control all external and internal bus operations in the PSG. When using a processor other than the CP1600, these signals can be provided either by comparable bus signals or by simulating the signals on I/O lines of the processor. The PSG decodes these signals as illustrated in the following:

BDIR	BC2	BC1	CP1600 FUNCTION	PSG FUNCTION
0	0	0	NACT	INACTIVE. See 010 (IAB) below.
0	0	1	ADAR	LATCH ADDRESS. See 111 (INTAK) below.
0	1	0	IAB	INACTIVE. The PSG/CPU bus is inactive. DA7--DA0 are in a high impedance state.
0	1	1	DTB	READ FROM PSG. This signal causes the contents of the register which is currently addressed to appear on the PSG/CPU bus. DA7--DA0 are in the output mode.
1	0	0	BAR	LATCH ADDRESS. See 111 (INTAK) below.
1	0	1	DW	INACTIVE. See 010 (IAB) above.
1	1	0	DWS	WRITE TO PSG. This signal indicates that the bus contains register data which should be latched into the currently addressed register. DA7--DA0 are in the input mode.
1	1	1	INTAK	LATCH ADDRESS. This signal indicates that the bus contains a register address which should be latched in the PSG. DA7--DA0 are in the input mode.

While interfacing to a processor other than the CP1600 would simply require simulating the above decoding, the redundancies in the PSG functions vs. bus control signals can be used to advantage in that only four of the eight possible decoded bus functions are required by the PSG. This could simplify the programming of the bus control signals to the following, which would only require that the processor generate two bus control signals (BDIR and BC1, with BC2 tied to +5V):

BDIR	BC2	BC1	PSG FUNCTION
0	1	0	INACTIVE.
0	1	1	READ FROM PSG.
1	1	0	WRITE TO PSG.
1	1	1	LATCH ADDRESS.



ANALOG CHANNEL A, B, C (outputs): pins 4, 3, 38 (AY-3-8910)
pins 5, 4, 1 (AY-3-8912)

Each of these signals is the output of its corresponding D/A Converter, and provides an up to 1V peak-peak signal representing the complex sound waveshape generated by the PSG.

IOA7--IOA0 (input/output): pins 14--21 (AY-3-8910)
pins 7--14 (AY-3-8912)

IOB7--IOB0 (input/output): pins 6--13 (AY-3-8910)
(not provided on AY-3-8912)

Input/Output A7--A0, B7--B0

Each of these two parallel input/output ports provides 8 bits of parallel data to/from the PSG/CPU bus from/to any external devices connected to the IOA or IOB pins. Each pin is provided with an on-chip pull-up resistor, so that when in the "input" mode, all pins will read normally high. Therefore, the recommended method for scanning external switches, for example, would be to ground the input bit.

TEST 1: pin 39 (AY-3-8910)
pin 2 (AY-3-8912)

TEST 2: pin 26 (AY-3-8910)
(not connected on AY-3-8912)

These pins are for GI test purposes only and should be left open—do not use as tie-points.

V_{CC}: pin 40 (AY-3-8910)
pin 3 (AY-3-8912)

Nominal +5Volt power supply to the PSG.

V_{SS}: pin 1 (AY-3-8910)
pin 6 (AY-3-8912)

Ground reference for the PSG.

ARCHITECTURE

The AY-3-8910/8912 is a register oriented Programmable Sound Generator (PSG). Communication between the processor and the PSG is based on the concept of memory-mapped I/O. Control commands are issued to the PSG by writing to 16 memory-mapped registers. Each of the 16 registers within the PSG is also readable so that the microprocessor can determine, as necessary, present states or stored data values.

All functions of the PSG are controlled through its 16 registers which once programmed, generate and sustain the sounds, thus freeing the system processor for other tasks.

REGISTER ARRAY

The principal element of the PSG is the array of 16 read/write control registers. These 16 registers look to the CPU as a block of memory and as such occupy a 16 word block out of 1,024 possible addresses. The 10 address bits (8 bits on the common data/address bus, and 2 separate address bits A8 and $\overline{A9}$) are decoded as follows:

*$\overline{A9}$	A8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	1	0	0	0	0	0	0	0	0
THRU									
0	1	0	0	0	0	1	1	1	1
HIGH ORDER (Chip Select)						LOW ORDER (Register #)			

* $\overline{A9}$ is not provided on the AY-3-8912.

The four low order address bits select one of the 16 registers (R0--$R17_8$). The six high order address bits function as "chip selects" to control the tri-state bidirectional buffers (when the high order address bits are "incorrect", the bidirectional buffers are forced to a high impedance state). High order address bits $\overline{A9}$ A8 are fixed in the PSG design to recognize a 01 code; high order address bits DA7--DA4 may be mask-programmed to any 4-bit code by a special order factory mask modification. Unless otherwise specified, address bits DA7--DA4 are programmed to recognize only a 0000 code. A valid high order address latches the register address (the low order 4 bits) in the Register Address Latch/Decoder block. A latched address will remain valid until the receipt of a new address, enabling multiple reads and writes of the same register contents without the need for redundant re-addressing.

Conditioning of the Register Address Latch/Decoder and the Bidirectional Buffers to recognize the bus function required (inactive, latch address, write data, or read data) is accomplished by the Bus Control Decode block.

SOUND GENERATING BLOCKS

The basic blocks in the PSG which produce the programmed sounds include:

Tone Generators	produce the basic square wave tone frequencies for each channel (A,B,C)
Noise Generator	produces a frequency modulated pseudo random pulse width square wave output.
Mixers	combine the outputs of the Tone Generators and the Noise Generator. One for each channel (A,B,C).
Amplitude Control	provides the D/A Converters with either a fixed or variable amplitude pattern. The fixed amplitude is under direct CPU control; the variable amplitude is accomplished by using the output of the Envelope Generator.
Envelope Generator	produces an envelope pattern which can be used to amplitude modulate the output of each Mixer.
D/A Converters	the three D/A Converters each produce up to a 16 level output signal as determined by the Amplitude Control.

I/O PORTS

Two additional blocks are shown in the PSG Block Diagram which have nothing directly to do with the production of sound—these are the two I/O Ports (A and B). Since virtually all uses of microprocessor-based sound would require interfacing between the outside world and the processor, this facility has been included in the PSG. Data to/from the CPU bus may be read/written to either of two 8-bit I/O Ports without affecting any other function of the PSG. The I/O Ports are TTL-compatible and are provided with internal pull-ups on each pin. Both Ports are available on the AY-3-8910; only I/O Port A is available on the AY-3-8912.

ENTER-TAINMENT

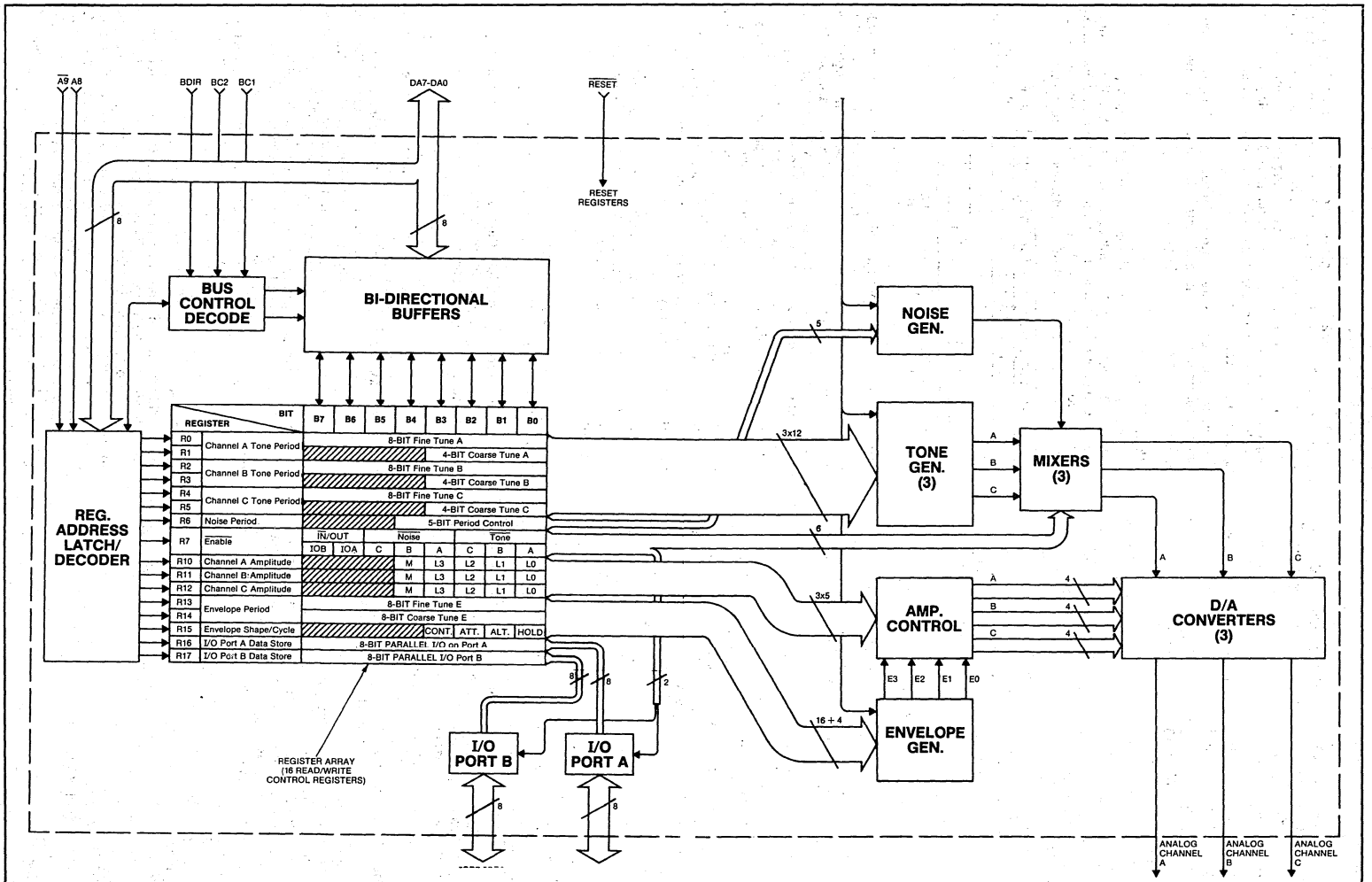


Fig. 2 PSG BLOCK DIAGRAM

OPERATION

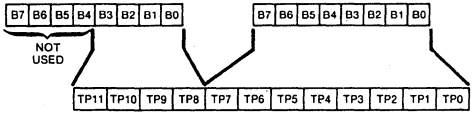
Since all functions of the PSG are controlled by the host processor via a series of register loads, a detailed description of the PSG operation can best be accomplished by relating each PSG function to the control of its corresponding register. The function of creating or programming a specific sound or sound effect logically follows the control sequence listed:

Operation	Registers	Function
Tone Generator Control	R0--R5	Program tone periods.
Noise Generator Control	R6	Program noise period.
Mixer Control	R7	Enable tone and/or noise on selected channels.
Amplitude Control	R10--R12	Select "fixed" or "envelope-variable" amplitudes.
Envelope Generator Control	R13--R15	Program envelope period and select envelope pattern

Tone Generator Control
(Registers R0, R1, R2, R3, R4, R5)

The frequency of each square wave generated by the three Tone Generators (one each for Channels A, B, and C) is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 12-bit Tone Period value. Each 12-bit value is obtained in the PSG by combining the contents of the relative Coarse and Fine Tune registers, as illustrated in the following:

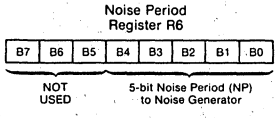
Coarse Tune Register	Channel	Fine Tune Register
R1	A	R0
R3	B	R2
R5	C	R4



12-bit Tone Period (TP) to Tone Generator

Noise Generator Control
(Register R6)

The frequency of the noise source is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 5-bit Noise Period value. This 5-bit value consists of the lower 5 bits (B4--B0) of register R6, as illustrated in the following:



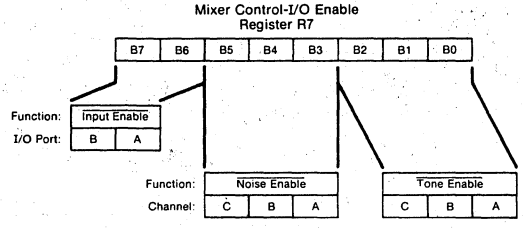
Mixer Control-I/O Enable
(Register R7)

Register 7 is a multi-function $\overline{\text{Enable}}$ register which controls the three Noise/Tone Mixers and the two general purpose I/O Ports.

The Mixers, as previously described, combine the noise and tone frequencies for each of the three channels. The determination of combining neither/either/both noise and tone frequencies on each channel is made by the state of bits B5--B0 of R7.

The direction (input or output) of the two general purpose I/O Ports (IOA and IOB) is determined by the state of bits B7 and B6 of R7.

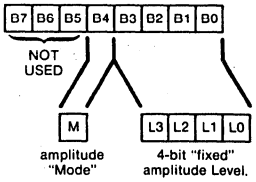
These functions are illustrated in the following:



Amplitude Control
(Registers R10, R11, R12)

The amplitudes of the signals generated by each of the three D/A Converters (one each for Channels A, B, and C) is determined by the contents of the lower 5 bits (B4--B0) of registers R10, R11, and R12 as illustrated in the following:

Amplitude Control Register #	Channel
R10	A
R11	B
R12	C

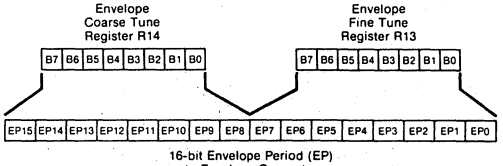


Envelope Generator Control
(Registers R13, R14, R15)

To accomplish the generation of fairly complex envelope patterns, two independent methods of control are provided in the PSG: first, it is possible to vary the frequency of the envelope using registers R13 and R14; and second, the relative shape and cycle pattern of the envelope can be varied using register R15. The following paragraphs explain the details of the envelope control functions, describing first the envelope period control and then the envelope shape/cycle control.

ENVELOPE PERIOD CONTROL (Registers R13, R14)

The frequency of the envelope is obtained in the PSG by first counting down the input clock by 256, then by further counting down the result by the programmed 16-bit Envelope Period value. This 16-bit value is obtained in the PSG by combining the contents of the Envelope Coarse and Fine Tune registers, as illustrated in the following:

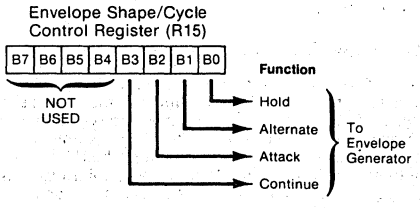


16-bit Envelope Period (EP) to Envelope Generator

ENVELOPE SHAPE/CYCLE CONTROL (Register R15)

The Envelope Generator further counts down the envelope frequency by 16, producing a 16-state per cycle envelope pattern as defined by its 4-bit counter output, E3 E2 E1 E0. The particular shape and cycle pattern of any desired envelope is accomplished by controlling the count pattern (count up/count down) of the 4-bit counter and by defining a single-cycle or repeat-cycle pattern.

This envelope shape/cycle control is contained in the lower 4 bits (B3--B0) of register R15. Each of these 4 bits controls a function in the envelope generator, as illustrated in the following:



ENTER-TAINMENT

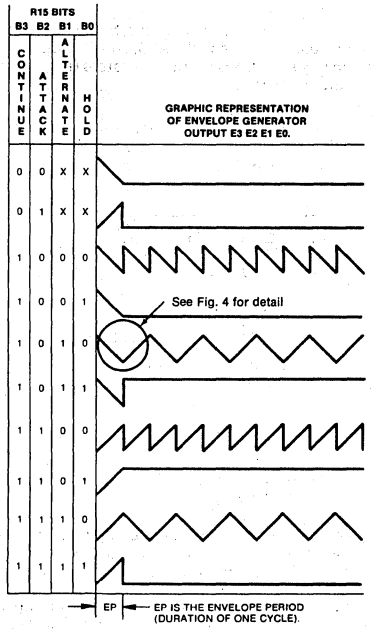


Fig. 3 ENVELOPE SHAPE/CYCLE OPERATION

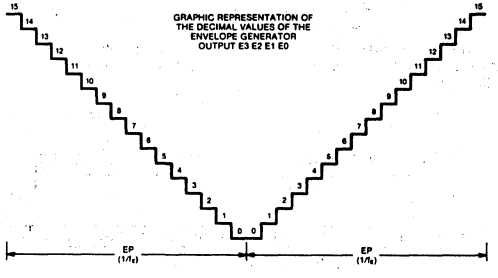


Fig. 4 DETAIL OF TWO CYCLES OF Fig. 3 (ref. waveform "1010" in Fig. 3)

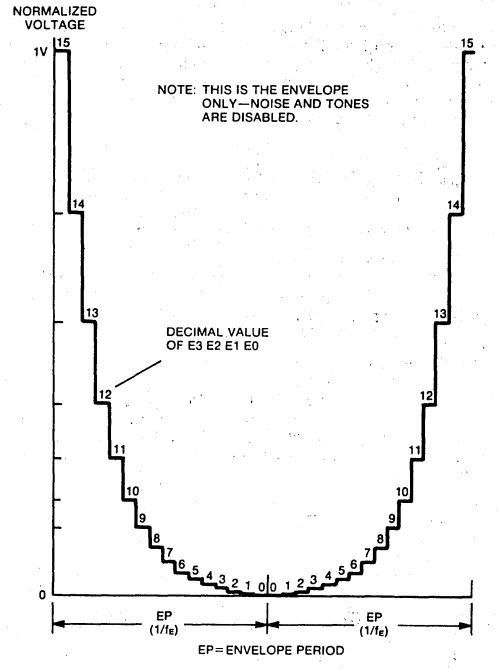


Fig. 5 D/A CONVERTER OUTPUT

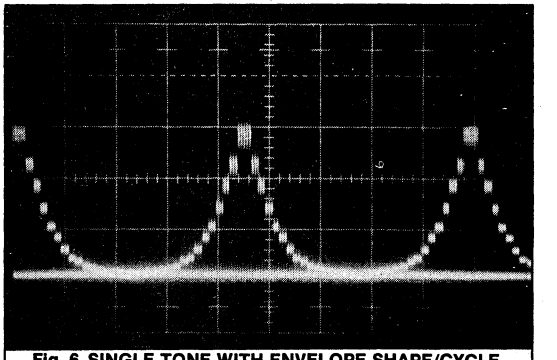


Fig. 6 SINGLE TONE WITH ENVELOPE SHAPE/CYCLE PATTERN 1010

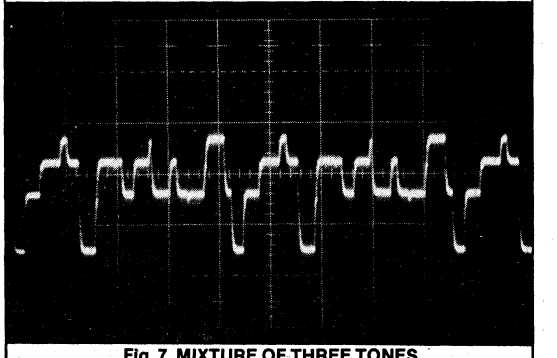


Fig. 7 MIXTURE OF THREE TONES WITH FIXED AMPLITUDES

I/O Port Data Store
(Registers R16, R17)

Registers R16 and R17 function as intermediate data storage registers between the PSG/CPU data bus (DA0--DA7) and the two I/O ports (IOA7--IOA0 and IOB7--IOB0). Both ports are available in the AY-3-8910; only I/O Port A is available in the AY-3-8912. Using registers R16 and R17 for the transfer of I/O data has no effect at all on sound generation.

D/A Converter Operation

Since the primary use of the PSG is to produce sound for the highly imperfect amplitude detection mechanism of the human ear, the D/A conversion is performed in logarithmic steps with a normalized voltage range of from 0 to 1 Volt. The specific amplitude control of each of the three D/A Converters is accomplished by the three sets of 4-bit outputs of the Amplitude Control block, while the Mixer outputs provide the base signal frequency (Noise and/or Tone).

ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +40°C
V_{CC} and all other input/output voltages with respect to V_{SS} ..... −0.3V to +8.0V

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5V ±5%
V_{SS} = GND
Operating Temperature = 0°C to +40°C

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
All Inputs						
Logic "0"	V_{IL}	0	—	0.6	V	
Logic "1"	V_{IH}	2.4	—	V_{CC}	V	
All Outputs (except Analog Channel Outputs)						
Logic "0"	V_{OL}	0	—	0.5	V	I_{OL} = 1.6mA, 20pF
Logic "1"	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 100μA, 20pF
Analog Channel Outputs	V_0	0	—	60	dB	Test circuit: Fig. 8
Power Supply Current	I_{CC}	—	45	75	mA	
AC CHARACTERISTICS						
Clock Input						
Frequency	f_C	1.0	—	2.0	MHz	Fig. 9
Rise Time	t_r	—	—	50	ns	Fig. 9
Fall Time	t_f	—	—	50	ns	Fig. 9
Duty Cycle	—	25	50	75	%	Fig. 9
Bus Signals (BDIR, BC2, BC1)						
Associative Delay Time	t_{BD}	—	—	50	ns	Fig. 9
Reset						
Reset Pulse Width	t_{RW}	500	—	—	ns	Fig. 10
Reset to Bus Control Delay Time	t_{RB}	100	—	—	ns	Fig. 10
A9, A8, DA7--DA0 (Address Mode)						
Address Setup Time	t_{AS}	400	—	—	ns	Fig. 11
Address Hold Time	t_{AH}	100	—	—	ns	Fig. 11
DA7--DA0 (Write Mode)						
Write Data Pulse Width	t_{DW}	500	—	10,000	ns	Fig. 12
Write Data Setup Time	t_{DS}	50	—	—	ns	Fig. 12
Write Data Hold Time	t_{DH}	100	—	—	ns	Fig. 12
DA7--DA0 (Read Mode)						
Read Data Access Time	t_{DA}	—	250	500	ns	Fig. 13
DA7--DA0 (Inactive Mode)						
Tristate Delay Time	t_{TS}	—	100	200	ns	Fig. 13

**Typical values are at +25°C and nominal voltages.

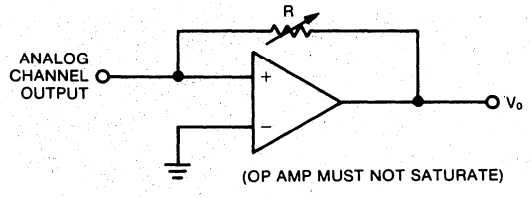


Fig. 8 ANALOG CHANNEL OUTPUT TEST CIRCUIT

ENTER-TAINMENT

TIMING DIAGRAMS

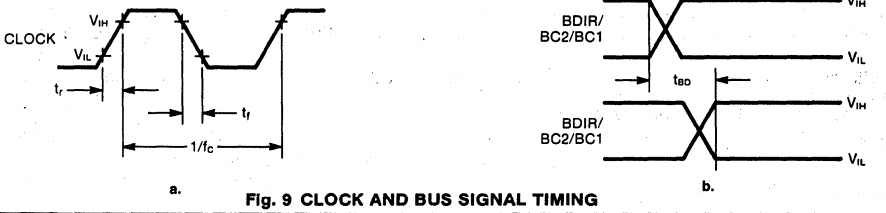


Fig. 9 CLOCK AND BUS SIGNAL TIMING

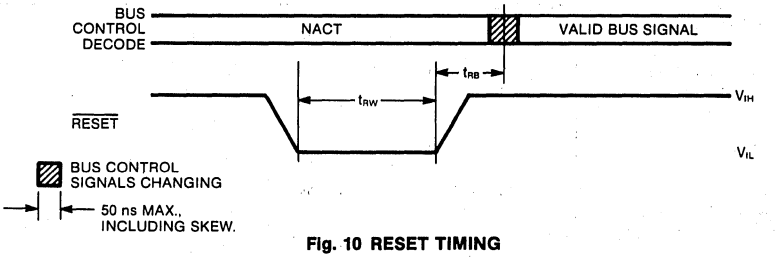
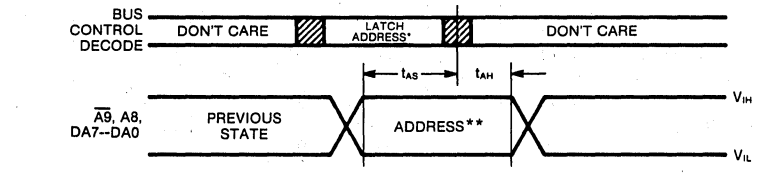


Fig. 10 RESET TIMING

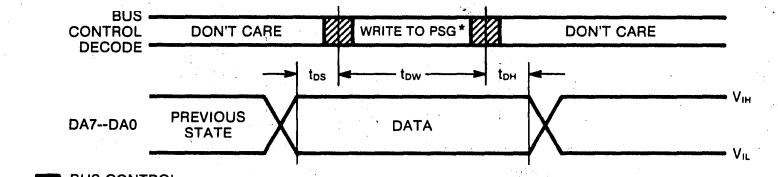


**REFER TO PARAGRAPH 2.1.1 FOR A DESCRIPTION OF "VALID" PSG ADDRESSING.

*ANY COMBINATION OF BDIR, BC2, BC1 WHICH DECODE "LATCH ADDRESS":

	BDIR	BC2	BC1
	0	0	1
or	1	0	0
or	1	1	1

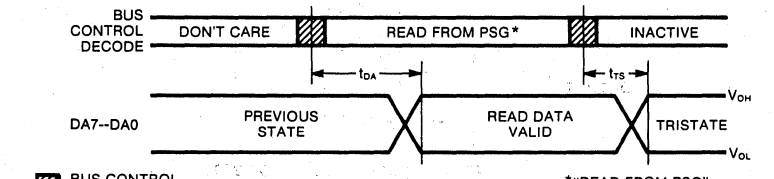
Fig. 11 LATCH ADDRESS TIMING



*"WRITE TO PSG":

BDIR	BC2	BC1
1	1	0

Fig. 12 WRITE DATA TIMING



*"READ FROM PSG":

BDIR	BC2	BC1
0	1	1

Fig. 13 READ DATA TIMING

ENTER-TAINMENT

Tunes Synthesizer

FEATURES

- 25 different tunes plus 3 chimes
- Mask programmable with customer specified tunes for toys, musical boxes, etc.
- Minimal external components
- Automatic switch-off signal at end of tune for power saving
- Envelope control to give organ or piano quality
- Sequential tune mode
- 4 door capability when used as doorchime
- Operation with tunes in external PROM if required
- Single supply (+5V) operation

DESCRIPTION

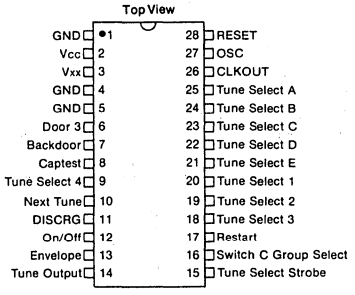
The AY-3-1350 is an N-Channel MOS microcomputer based synthesizer of pre-programmed tunes for applications in toys, musical boxes, and doorchimes. The standard device has a set of 25 different popular and classical tunes chosen for their international acceptance. In addition there are 3 chimes making a total of 28 tunes.

The chip is mask-programmable during manufacture enabling the quantity user to select his own music. The tunes chosen can be of different lengths and the number can be up to 28 (see later).

The device has multi-mode operation making it suitable for a wide variety of applications.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



TUNES

The standard AY-3-1350 contains the following tunes:

A0	Toreador	A1	John Brown's Body
B0	William Tell	B1	Clementine
C0	Hallelujah Chorus	C1	God Save the Queen
D0	Star Spangled Banner	D1	Colonel Bogey
E0	Yankee Doodle	E1	Marseillaise
A2	America, America	A3	O Sole Mio
B2	Deutschland Leid	B3	Santa Lucia
C2	Wedding March	C3	The End
D2	Beethoven's 5th	D3	Blue Danube
E2	Augustine	E3	Brahms' Lullaby
A4	Hell's Bells		
B4	Jingle Bells		
C4	La Vie en Rose		
D4	Star Wars		
E4	Beethoven's 9th		

Chime X Westminster Chime
Chime Y Simple Chime
Chime Z Descending Octave Chime

ENTER-TAINMENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

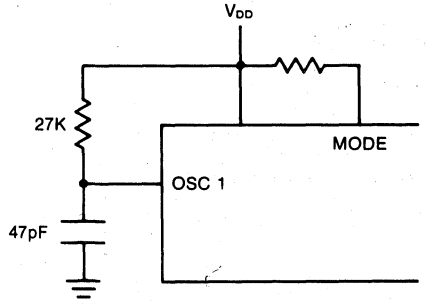
Storage Temperature ..... −55°C to +150°C
Voltage on any pin with respect to ground (Vss) ..... −0.3V to +10.0V

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)
Operating Temperature (T_A) = 0°C to +40°C

Characteristics	Sym	Min	Max	Units	Conditions
DC CHARACTERISTICS					
Primary Supply Voltage	V_{DD}	4.5	7.0	V	
Output Buffer Supply Voltage	V_{XX}	4.5	9.0	V	
Primary Supply Current	I_{DD}	—	55	mA	No load
Output Buffer Supply Current	I_{XX}	—	5	mA	No load
Logic Input Low Voltage	V_{IL}	−0.2	0.8	V	
Logic Input High Voltage (Note 2) (Except $\overline{RESET}$ and OSC when driven externally)	V_{IH_1}	2.4	V_{DD}	V	
Logic Input High Voltage ($\overline{RESET}$ and OSC)	V_{IH_2}	4.0	V_{DD}	V	
Logic Output High Voltage (Note 2)	V_{OH}	2.4		V	I_{OH} = 100μA
Logic Output Low Voltage	V_{OL}	—	0.45	V	I_{OL} = 1.6mA, V_{XX} = 4.5V
	—	—	0.90	V	I_{OL} = 5.0mA, V_{XX} = 4.5V
	—	—	0.50	V	I_{OL} = 5.0mA, V_{XX} = 9.0V
	—	—	0.90	V	I_{OL} = 10.0mA V_{XX} = 9.0V (Note 1)
AC CHARACTERISTICS					
Oscillator frequency variation for a fixed RC network	Δf	−20%	+20%		@ CLK OUT 167kHz (Note 3)
CLK OUT Output					
Period	t_{CY}	4	20	μs	
High Pulse Width	t_{CLKH}	¼ t_{CY}			
Low Pulse Width	t_{CLKC}	¾ t_{CY}			

NOTES: 1. Total I_{OL} for all registers must be less than 150mA under any conditions.
2. Except following pins which have open drain outputs/inputs: 6, 7, 8, 12 and 13.
3. Test circuit:



ENTER-TAINMENT

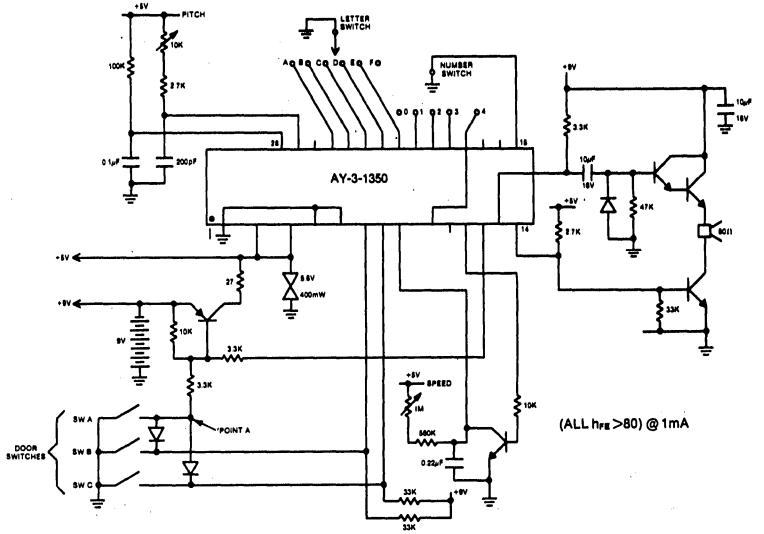


Fig. 1 SYSTEM DIAGRAM

OPERATION SUMMARY

Use of the AY-3-1350 can be split into three groups which are described in detail in separate sections later on:

ONE CHIP AY-3-1350 system generating 25 tunes plus 3 chimes which have been pre-programmed into the standard device.

ONE CHIP AY-3-1350 system generating any tunes desired. There can be any number of these. This involves a mask programming during manufacture so this is not suitable for small quantity production.

TWO CHIP AY-3-1350 plus PROM system generating any tunes desired as above, but using the standard device so that applications involving small quantities become feasible. (CMOS gate also required.)

ONE CHIP STANDARD AY-3-1350 SYSTEM

Typical Implementation

There are many ways to connect the standard device depending on the exact application. Figure 1 shows just one implementation of the device in a doorchime. This circuit gives access to all 25 tunes from switch A and one of 5 tunes from switch C as well as the descending active chime from switch B. The tune selected for switch B follows the tunes list given earlier according to the setting of the two tune select switches (A—E and 0—4). The tune selected from the switch C in Figure 1 is one of the five tunes A0 and E0 depending on the setting of the letter switch. For example, suppose the letter switch is a E and the number switch at 4 then the tunes given by the Figure 1 circuit will be:

Switch A: Beethoven's 9th (E4)
Switch C: Yankee Doodle (E0)
Switch B: Descending Octave Chime (Chime Z)

When the letter switch is in position F there will be chimes on all doors independent of the number switch setting as follows:

Switch A: Westminster Chime
Switch C: Simple Chime
Switch B: Descending Octave Chime

In Figure 1 there is virtually no power consumption in the standby condition (external transistor leakages only). When any door switch is activated the circuit powers up, plays a tune, and then automatically powers down again to conserve the battery, even if the operator keeps his finger on the push to the end of the tune. He must release it and re-press to play again with the circuit of Figure 1. Any of the door switches will pull point A to ground turning on the PNP transistor in the power supply line. This causes +5V to be applied to the AY-3-1350 and the first operation of the chip is to put ON/OFF (pin 12) to logic 0. This maintains the power through the PNP, even after the switch is released. The device can turn off its own power at the end of a tune by raising ON/OFF to logic 1.

Figure 1 shows only a typical one-chip implementation. Further options come from use of different switching and/or from use of the next tune facilities built into the chip. These will now be considered in turn.

Switching Options

In Figure 1 the Back-door Group Select pin (16) is not connected, and one of the five tunes A0 to E0 will play if the back-door push is activated. Other number groups can be chosen by connecting the Back-door Group Select pin as follows:

TABLE 2

Switch C Group Select pin (16) is connected to:	Switch C Tunes
no other pin	A0—E0
Tune Select 1 (pin 20)	A1—E1
Tune Select 2 (pin 19)	A2—E2
Tune Select 3 (pin 18)	A3—E3
Tune Select 4 (pin 9)	A4—E4

Which one of the five possible back-door tunes will be played depends on the current setting of the letter switch A—E.

The back-door group selection can be made by hard-wire connection for a permanent selection or a third switch can be added to give a back-door group selection feature in addition.

LED Direct Drive

Vxx drives the gate of the output buffer, allowing adjustment of drive capability:

Vxx	VOUT	ISINK (typ.)
5V	0.4V	2.5mA
5V	0.7V	4.2mA
10V	0.4V	5.8mA
10V	0.7V	10.0mA
10V	1.0V	14.1mA

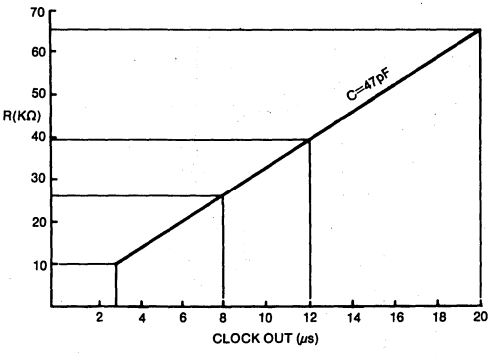


Fig. 2 TYPICAL OSCILLATOR RC CHART @ 25° C

Using the power-up circuit of Figure 1 the AY-3-1350 will have +5V supplied to it and latched within a few microseconds (depends on external components) from any bell-push closing. The device starts to operate when the RESET pin reaches logic 1 (about 10ms with components shown) but in fact the tune select switches are not interrogated until approximately 6 ms later. The total is sufficient for most bell-pushes to complete any bounce period and for a firm selection of tunes to be made.

Next Tune Facilities

At the end of playing a tune the example circuit of Figure 1 powers down because ON/OFF (pin 12) is raised to a logic 1 by the device at the end of a tune. The simplified flow diagram in Figure 5 shows that before the power down there is a test for connection between NEXT TUNE (pin 10) then RESTART (pin 17) with TUNESELECT 4 (pin 9). At these times NEXT TUNE (pin 10) then RESTART (pin 17), which are normally at logic 1, output a logic ϕ pulse. This is looked for at input TUNESELECT 4 (pin 9).

If neither is found the power down system is reached as in Figure 1.

A NEXT TUNE (pin 10)—TUNE SELECT 4 (pin 9) connection at the moment of test causes the next tune in the list to be played after a short pause (equal to a musical breve—the actual time depends on the setting of the tune speed control). The order of the tunes is A0 to E4 as given in the listing of standard AY-3-1350 tunes. If the last tune (E4) was played then the circuit will go on to play the first tune A0 (and then successive ones). Figure 5 shows this pictorially. The chimes are not included in the cycling sequence.

A RESTART (pin 17)—TUNESELECT 4 (pin 9) connection at the moment of test at the end of a tune causes the same selected tune to be played again. Figure 3 shows that in this case the tune sensing mechanism is passed through once more however, so the tune would be different second time if the switches were altered while the first tune was playing.

The connections referred to cannot be permanent because otherwise the circuit would never stop playing tunes. Figure 4 shows how transistors are used to make the connection in a practical application.

ONE CHIP CUSTOM TUNES SYSTEM

Customizing the Tunes

The AY-3-1350 has pre-programmed tunes, but the device is mask programmable during manufacture with any music required. A minimum of 1 tune to a maximum of 28 tunes can be incorporated. Examples as follows:

Tunes	Total No. of notes, all tunes together	Average notes per tune
1	252	252
2	251	126
5	248	50
10	243	24
20	233	12
25	228	9

(The general formula is Total No. of notes = 253—No. of tunes.)

As an indication, about 90 seconds of music can be incorporated.

All musical rests are counted as one note. Semiquavers, quavers, dotted quavers, crotchets, dotted crotchets, minims, dotted minims and semibreves can all be accommodated and the range is about 2½ octaves. The position of these octaves can be chosen by the user up to a maximum pitch of about A = 1760Hz. The tunes for incorporation in the device should be presented to General Instrument as normal music manuscript.

Applications for Customized Tunes

If the number of tunes is less than the number of switch positions then the circuit will automatically proceed directly to power down if this mode is being used, or will find the next available tune if in the sequential mode.

All the different facilities described in SECTION 2 are still available when user tunes are masked into the device.

For TOYS, sequential tune playing adds variety and reduces the number of switches required, keeping costs to a minimum.

For MUSICAL BOXES playing the same tune repeatedly preserves one of the traditional features.

TWO CHIP STANDARD AY-3-1350 PLUS PROM SYSTEM

Introduction

With the addition of an external ROM or PROM the standard AY-3-1350 will play almost any tune or tunes you desire. There could be 28 tunes averaging 8 notes each or one tune of up to 252 notes for example. In all about 1—2 minutes worth of music. General Instrument can later integrate the external tunes into the main synthesizer to give a one chip system.

Overall Coding Scheme

The external PROM should be 256 x 8 bits and of any static TTL compatible type.

It can have more words, but the tunes synthesizer will only use 256 x 8 bits at a time, e.g. if PROM type 2708 is used (1K x 8 bits), the two higher order address lines should be connected to ground or switches put on them to give 4 times the amount of music (see logic diagram Figure 6). The rest of this article will assume a 256 x 8 bit PROM, and the addresses will be referred to as 000 to 377. Octal notation is used throughout.

The PROM address 000 must contain data 377 and address 377 must contain data 125 which is a key to open up the external PROM features. All other addresses can contain tune data.

Each tune consists of a series of notes with one byte of PROM for each. Every tune must have a tune end marker byte 377 after the last note, and the final tune must have a byte 376 after the 377 end marker. The memory allocation is shown diagrammatically in Figure 5. Tunes can be of any length and there can be any number of them subject only to the memory limit (28 max.).

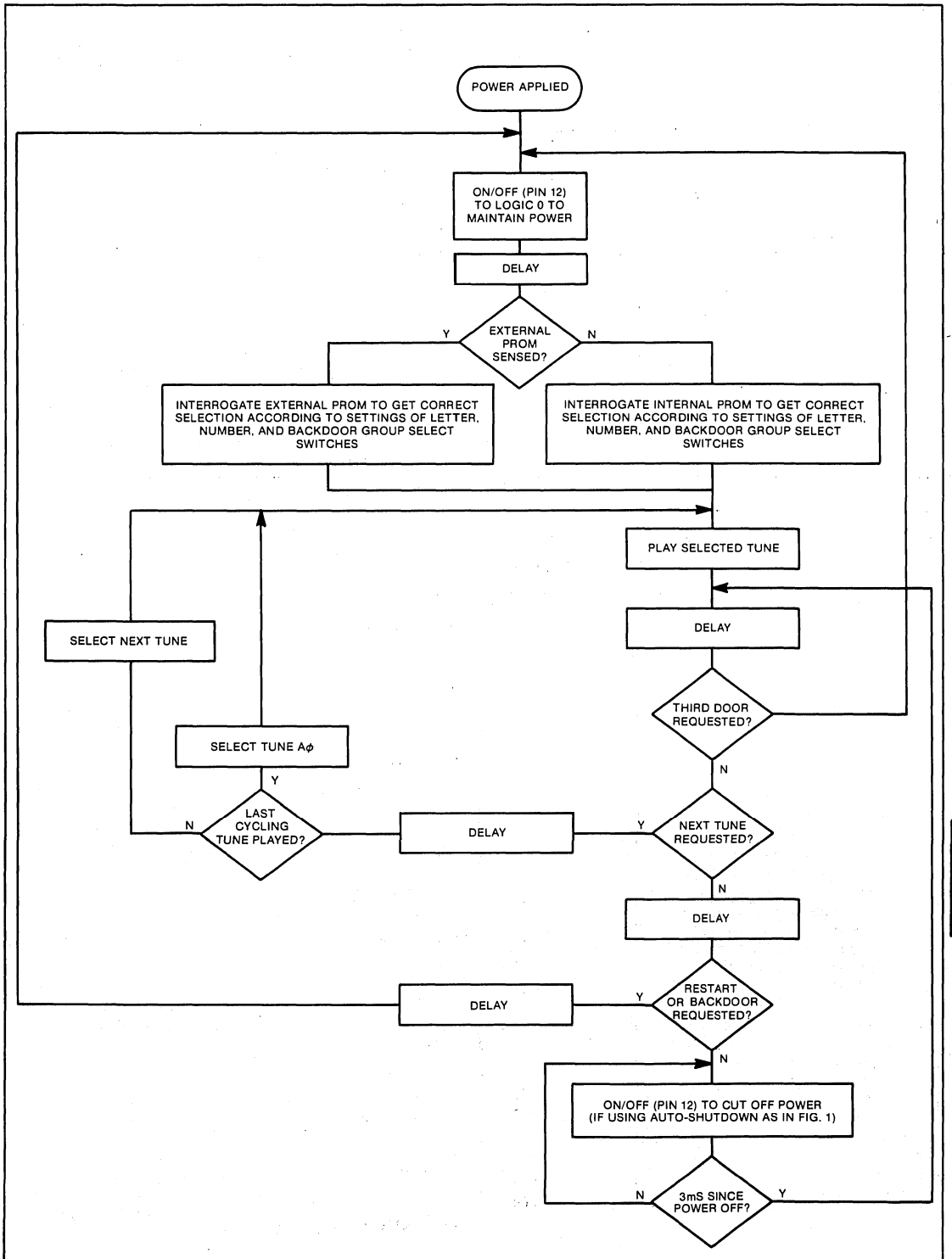
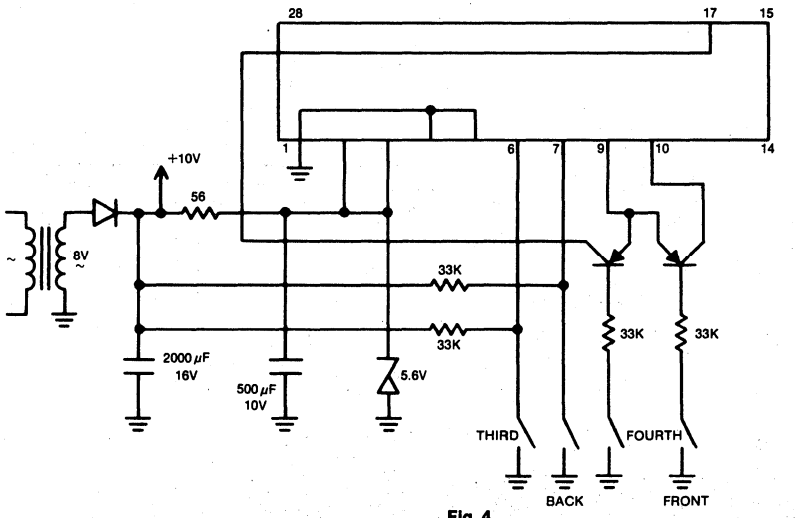


Fig. 3 SIMPLIFIED FLOW DIAGRAM

ENTER-TAINMENT



PIN	FUNCTION
6	DOOR 3
7	BACKDOOR
9	TUNESELECT 4
10	NEXT TUNE
17	RESTART

Fig. 4

PROM Memory Allocation

Address	DATA	
0	377	(tunes select timeslot)
		Tune 1
	377	(end of tune marker)
		Tune 2
	377	(end of tune marker)
		More tunes
		Last Tune
	377	(end of tune marker)
	376	(end of listing)
	000	Not used
	000	
	000	
	000	
377	125	(external ROM enable key)

Fig. 5

ENTER-TAINMENT

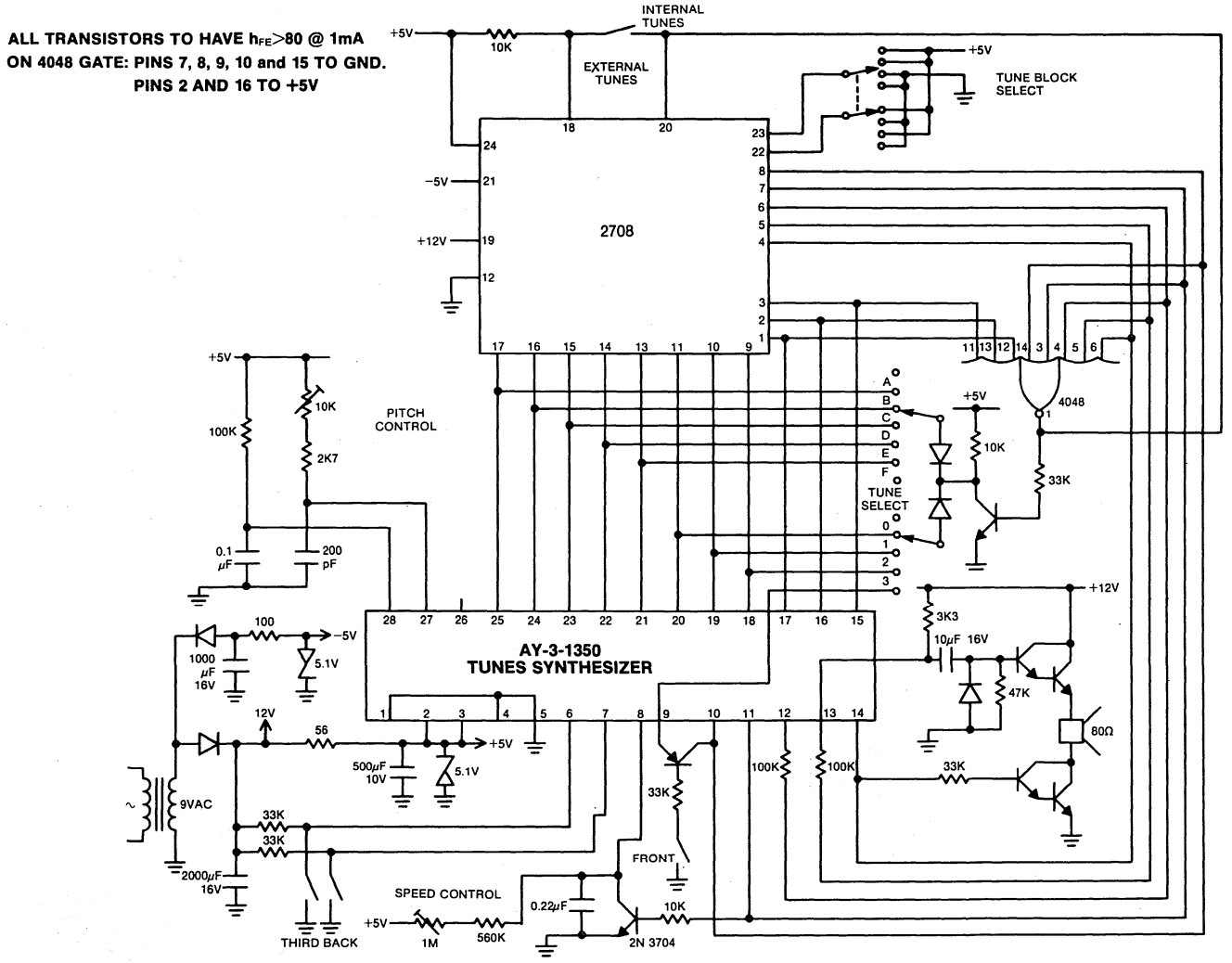


Fig. 6 PLAYING YOUR OWN TUNES WITH EXTERNAL PROM. (OR INTERNAL TUNES)

Consumer 8

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
			TV Games
BALL & PADDLE	Six selectable games for one or two players, with vertical paddle motion.	AY-3-8500 AY-3-8500-1	8-4
ROADRACE	One or two player games where racing skill in "traffic" generates the highest score.	AY-3-8603 AY-3-8603-1	8-19
WARFARE	One or two player games featuring subs, destroyers, cargo ships, and spaceships.	AY-3-8605 AY-3-8605-1	8-22
WIPEOUT	One or two player games where players "wipe out" objects by controlling a ball in the play area.	AY-3-8606 AY-3-8606-1	8-27
SHOOTING GALLERY	Twelve games for one or two players using external photocell rifles for shooting.	AY-3-8607 AY-3-8607-1	8-36
SUPERSPORT	Ten selectable games for one or two players, with vertical and horizontal paddle motion.	AY-3-8610 AY-3-8610-1	8-42
COLOR PROCESSOR	Adds color to the "8600" series dedicated TV Game circuits.	AY-3-8615	8-53
MOTOR CYCLE	One player cycle game with variable skill selection.	AY-3-8765	8-54
			Clocks
4 DIGIT	12/24 hour clocks with features for most clock/timing applications.	AY-5-1202A AY-5-1203A AY-5-1224A	8-60 8-60 8-63
4 DIGIT CLOCK RADIO	12/24 hour clock, 24 hour alarm, sleep timer, battery standby.	CK3300	8-65
			Appliances
CLOCK/TIMERS	24 hour programmable, repeatable on/off time switch with 4 digit clock.	AY-5-1230 AY-5-1231 AY-5-1232	8-78 8-78 8-78
DIGITAL THERMOMETER	Digital Thermometer and temperature controller.	AY-3-1270	8-82
			Counters/DVMs
3½ DIGIT DVM	DVM logic utilizing dual ramp integration.	AY-5-3507	8-94
3¾ DIGIT DVM	DVM logic utilizing single ramp integration.	AY-5-3500	8-99
4 DIGIT COUNTER/ DISPLAY	Counts, stores, and decodes 4 decades to 7-segment outputs.	AY-5-4007 AY-5-4007A AY-5-4007D	8-103 8-103 8-103
FLUORESCENT DISPLAY DRIVER	Direct drive to fluorescent display stores and siplay with internal max clock.	AY-5-4121 AY-5-4221	8-109 8-109

GENERAL INSTRUMENT

TV Games

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
BALL & PADDLE	Six selectable games for one or two players, with vertical paddle motion.	AY-3-8500 AY-3-8500-1	8-4
ROADRACE	One or two player games where racing skill in "traffic" generates the highest score.	AY-3-8603 AY-3-8603-1	8-19
WARFARE	One or two player games featuring subs, destroyers, cargo ships, and spaceships.	AY-3-8605 AY-3-8605-1	8-22
WIPEOUT	One or two player games where players "wipe out" objects by controlling a ball in the play area.	AY-3-8606 AY-3-8606-1	8-27
SHOOTING GALLERY	Twelve games for one or two players using external photocell rifles for shooting.	AY-3-8607 AY-3-8607-1	8-36
SUPERSPORT	Ten selectable games for one or two players, with vertical and horizontal paddle motion.	AY-3-8610 AY-3-8610-1	8-42
COLOR PROCESSOR	Adds color to the "8600" series dedicated TV Game circuits.	AY-3-8615	8-53
MOTOR CYCLE	One player cycle game with variable skill selection.	AY-3-8765	8-54

Ball & Paddle

FEATURES

- Full **COLOR** operation with AY-3-8515.
- 6 Selectable Games—Tennis, soccer, squash, practice and two rifle shooting games
- 625 Line (AY-3-8500) and 525 Line (AY-3-8500-1) versions
- Automatic Scoring
- Score display on T.V. Screen, 0 to 15
- Selectable Bat Size
- Selectable Rebound Angles
- Selectable Ball Speed
- Automatic or Manual Ball Service
- Action Sounds
- Shooting Forwards in Soccer Game
- Visually defined area for all Ball Games.

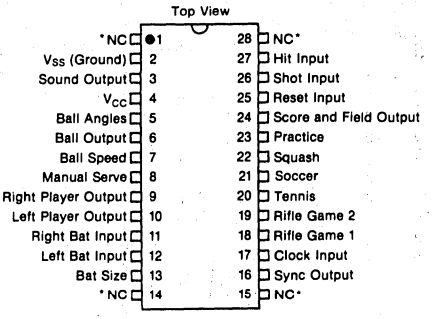
DESCRIPTION

The AY-3-8500 and AY-3-8500-1 circuits have been designed to provide a TV 'games' function which gives active entertainment using a standard domestic television receiver.

The circuit is intended to be battery powered and a minimum number of external components are required to complete the system.

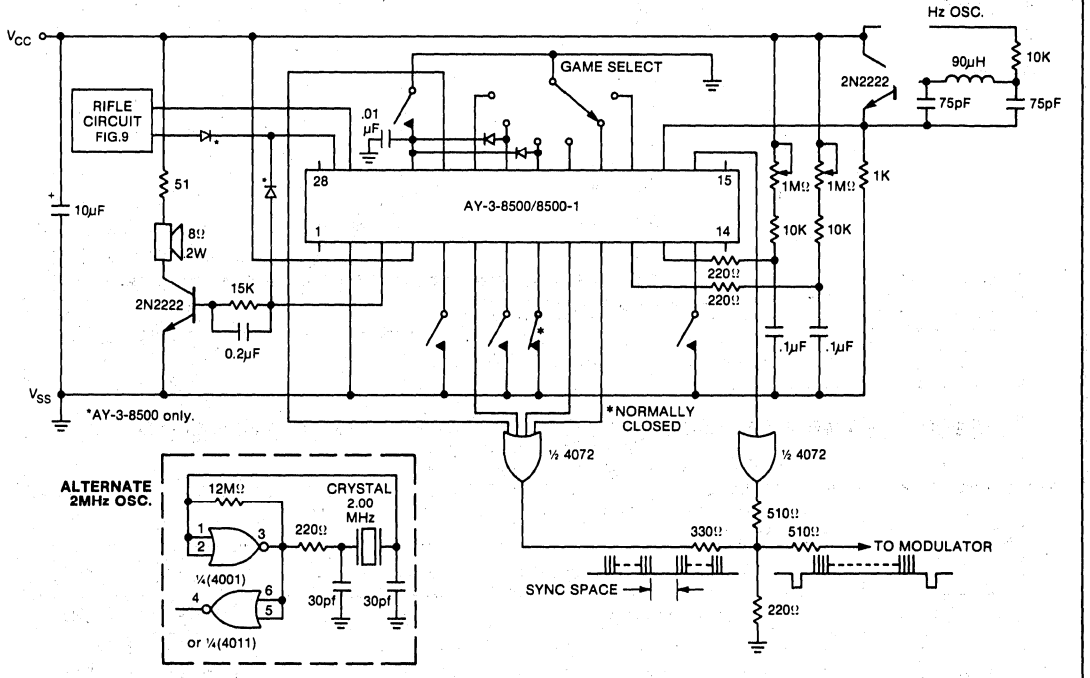
PIN CONFIGURATION

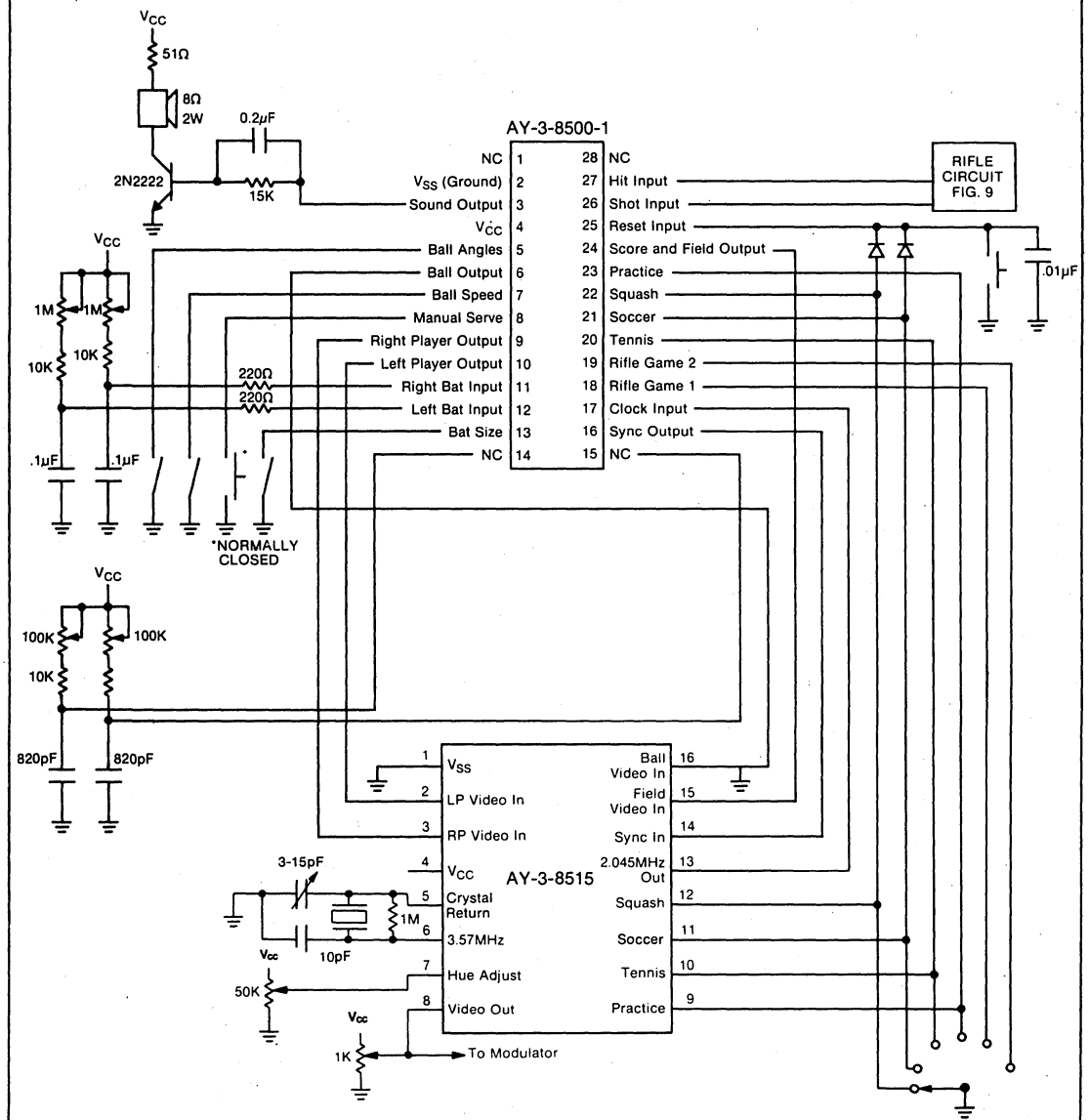
28 LEAD DUAL IN LINE



*Do not use as tie point.

SYSTEM DIAGRAM 1: BLACK AND WHITE IMPLEMENTATION





SYSTEM DIAGRAM 2: AY-3-8500-1 FULL COLOR IMPLEMENTATION USING AY-3-8515 COLOR CONVERTER CIRCUIT

CONSUMER

PIN FUNCTIONS (Pin numbers in parentheses)

Vss (2)
Negative supply input, nominally 0V(GND).

Sound Output (3)
The hit (32ms pulse/976Hz tone), boundary reflection (32ms pulse/488Hz tone) and score (32ms pulse/1.95KHz tone) sounds are output on this pin.

Vcc (4)
Positive supply input.

Ball Angles (5)
This input is left open circuit (Logic '1') to select two rebound angles and connected to Vss (Logic '0') to select four rebound angles. When two angles are selected they are ± 20°, when four are selected they are ±20° and ±40°. See Fig. 11.

Ball Output (6)
The ball video signal is output on this pin.

Ball Speed (7)
When this input is left open-circuit, low speed is selected (1.3 seconds for ball to traverse the screen). When connected to Vss (Logic '0'), the high speed option is selected (0.65 seconds for ball to traverse the screen).

Manual Serve (8)
This input is connected to V_{SS} (Logic '0') for automatic serving. When left open circuit (Logic '1') the game stops after each score. The serve is indicated by momentarily connecting this input to V_{SS}.

Right Player Output/Left Player Output (9,10)
The video signals for the right and left players are output on separate pins.

Right Bat Input/Left Bat Input (11,12)
An R-C network connected to each of these inputs controls the vertical position of the bats. Use a 10K resistor in series with each pot.

Bat Size (13)
This input is left open circuit (Logic '1') to select large bats and connected to V_{SS} (Logic '0') to select small bats. For a 19" T.V. screen, large bats are 1.9" and small bats are 0.95" high.

Sync Output (16)
The T.V. vertical and horizontal sync signals are output on this pin. See Fig. 1.

Clock Input (17)
The 2MHz master timing clock is input to this pin. The exact frequency is 2.012160 ± 1%.

Rifle Game 1, Rifle Game 2, Tennis, Soccer, Squash, Practice (18 thru 23)
These inputs are normally left open circuit (Logic '1') and are connected to V_{SS} (Logic '0') to select the desired game.

Score and Field Output (24)
The score and field video signal is output on this pin.

Reset (25)
This input is connected momentarily to Vss (Logic '0') to reset the score counters and start a new game. Normally left open circuit.

Shot Input (26)
This input is driven by a positive pulse output of a monostable to indicate a "shot".

Hit Input (27)
This input is driven by a positive pulse output of a monostable which is triggered by the shot input if the target is on the sights of the rifle.

NOTE: The "Shot" and "Hit" inputs have on-chip pull-down resistors to Vss. All other inputs (except the "Bat" inputs) have on-chip pull-up resistors to Vcc.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... -0.3 to +12V
Storage Temperature Range ..... -20°C to +70°C
Ambient Operating Temperature Range ..... 0°C to +40°C

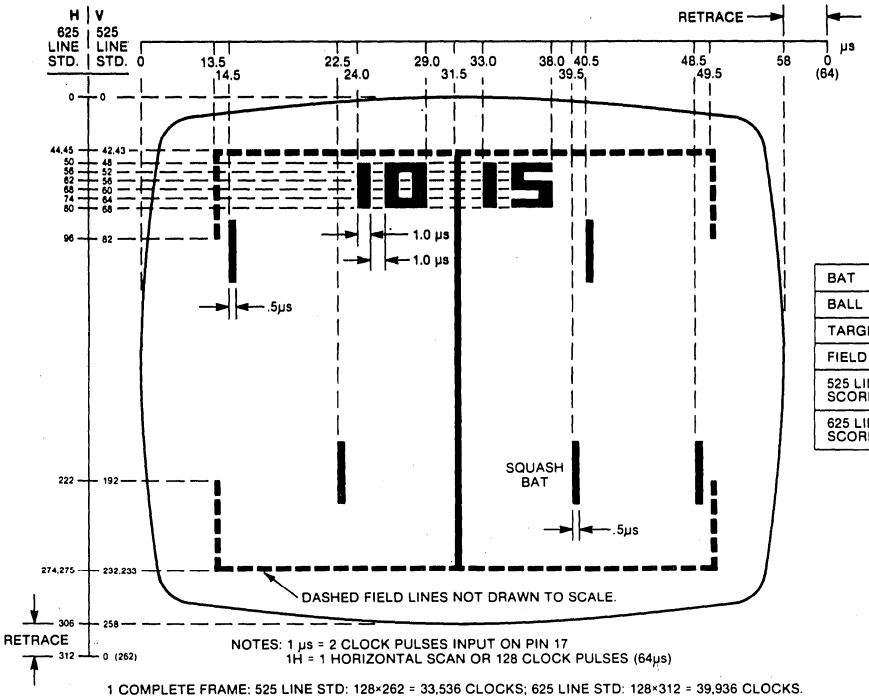
*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +6 to +7V
V_{SS} = 0V
Operating Temperature (T_A) = 0°C to +40°C

Characteristics at 25°C and Vcc = +6 Volts	Min	Typ	Max	Units	Conditions
Clock Input					Maximum clock source impedance
Frequency	1.99	2.01	2.03	MHz	of 1K to V_{CC} or V_{SS}.
Logic '0'	0	—	0.5	Volts	
Logic '1'	V_{CC}-2	—	V_{CC}	Volts	
Pulse Width — Pos.	—	200	—	ns	
Pulse Width — Neg.	—	300	—	ns	
Capacitance	—	10	—	pF	V_{IN} = 0V, F = 1MHz
Leakage	—	100	—	μA	
Control Inputs					Max. contact resistance of 1K to V_{SS}
Logic '0'	0	—	0.5	Volts	
Logic '1'	V_{CC}-2	—	V_{CC}	Volts	
Input Impedance	—	1.0	—	MΩ	Pull up to V_{CC}
Rifle Input	—	1.0	—	MΩ	Pull down to V_{SS}
Outputs					
Logic '0'	—	—	1.0	Volt	Iout = 0.5mA
Logic '1'	V_{CC}-2	—	—	Volts	Iout = 0.1mA
Power Supply Current	—	40	60	mA	at V_{CC} = +7V

CONSUMER



	H	V
BAT	0.5μs	14/28 lines
BALL	1.0μs	5 lines
TARGET	2.5μs	14 lines
FIELD	0.5μs	2 lines
525 LINE SCORE	5.0μs	20 lines
625 LINE SCORE	5.0μs	30 lines

Fig.1 LOCATION OF DATA OUTPUT PULSES

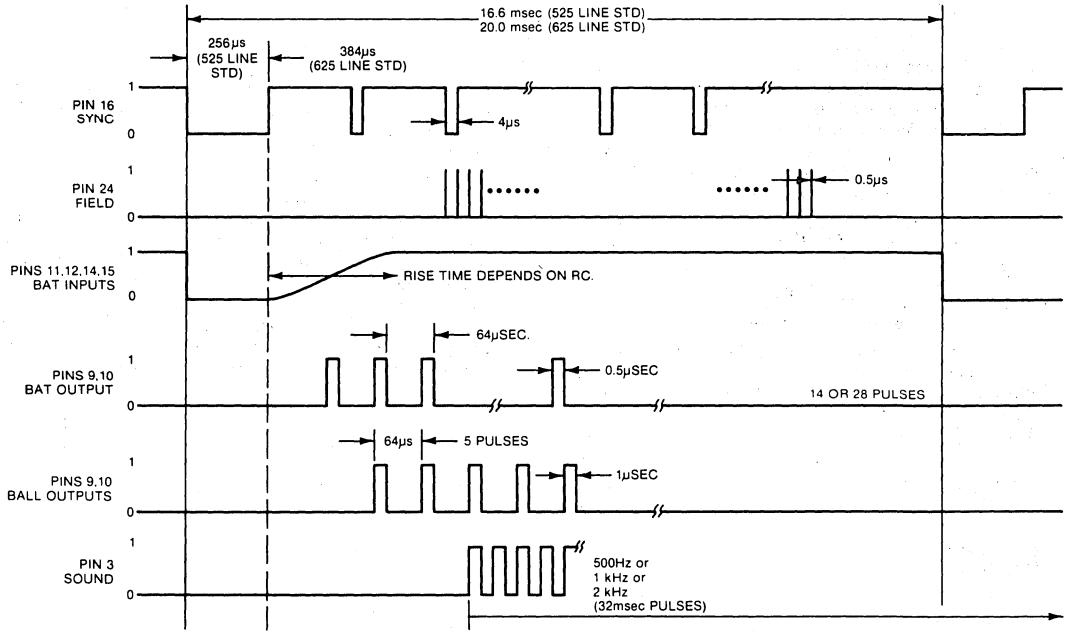


Fig.2 TIMING DIAGRAM

CONSUMER

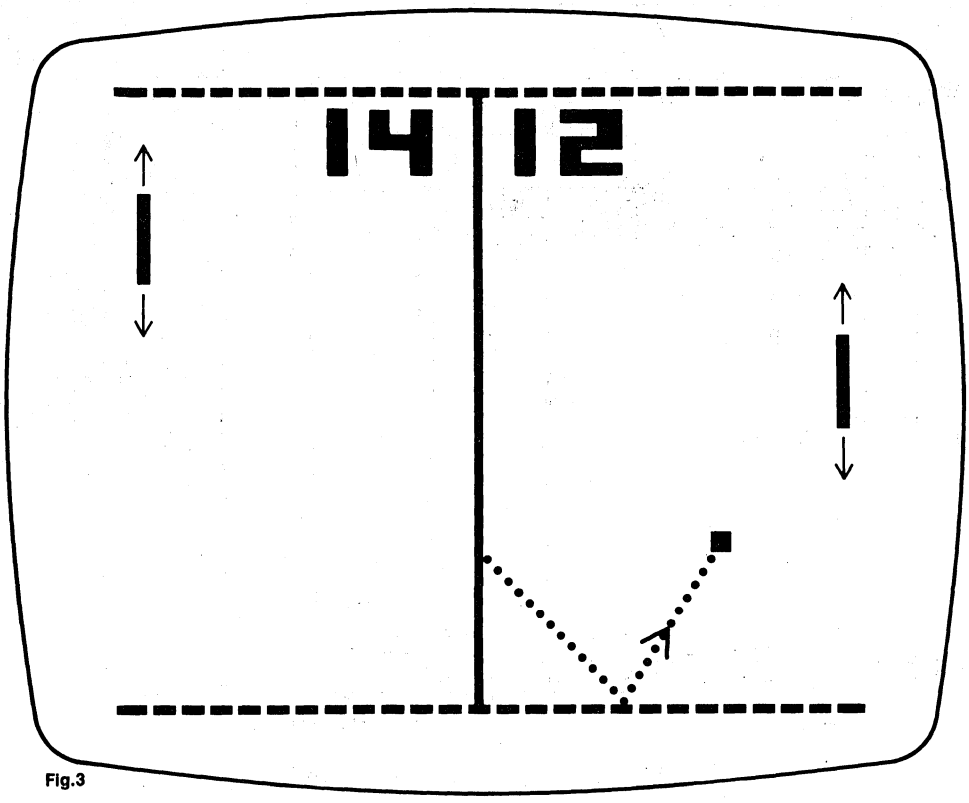


Fig.3

Tennis

With the tennis game the picture on the television screen would be similar to Figure 3 with one 'bat' per side, a top and bottom boundary and a center net. The individual scores are counted and displayed automatically in the position shown. The detail of the game will depend upon the selection of the options. Considering the situation where small bats are used and all angles, after the reset has been applied, the scores will be 0, 0 and the ball will serve arbitrarily to one side at one of the angles. If the ball hits the top or bottom boundary it will assume the angle of reflection and continue in play. The player being served must control his bat to intersect the path of the ball. When a 'hit' is detected by the logic, the section of the bat which made the hit is used to determine the new angle of the ball.

To expand on this, all 'bats' or 'players' are divided logically into four adjacent sections of equal length. When using the four angle option it is the quarter of bat which actually hits which defines the new direction for the ball.

The direction does not depend upon the previous angle of incidence. With the two angle option the top and bottom pairs of the bats are summed together and only the two shallower angles are used to program the new direction for the ball.

The ball will then traverse towards the other player, reflecting from the top or bottom as necessary until the other player makes his 'hit'. This action is repeated until one player misses the ball. The circuitry then detects a 'score' and automatically increments the correct score counter and updates the score display. The ball will then serve automatically towards the side which has just missed. This sequence is repeated until a score of 15 is reached by one side, whereupon the game is stopped. The ball will still bounce around but no further 'hits' or 'scores' can be made. While the game is in progress, three audio tones are output by the circuit to indicate top and bottom reflections, bat hits and scores.

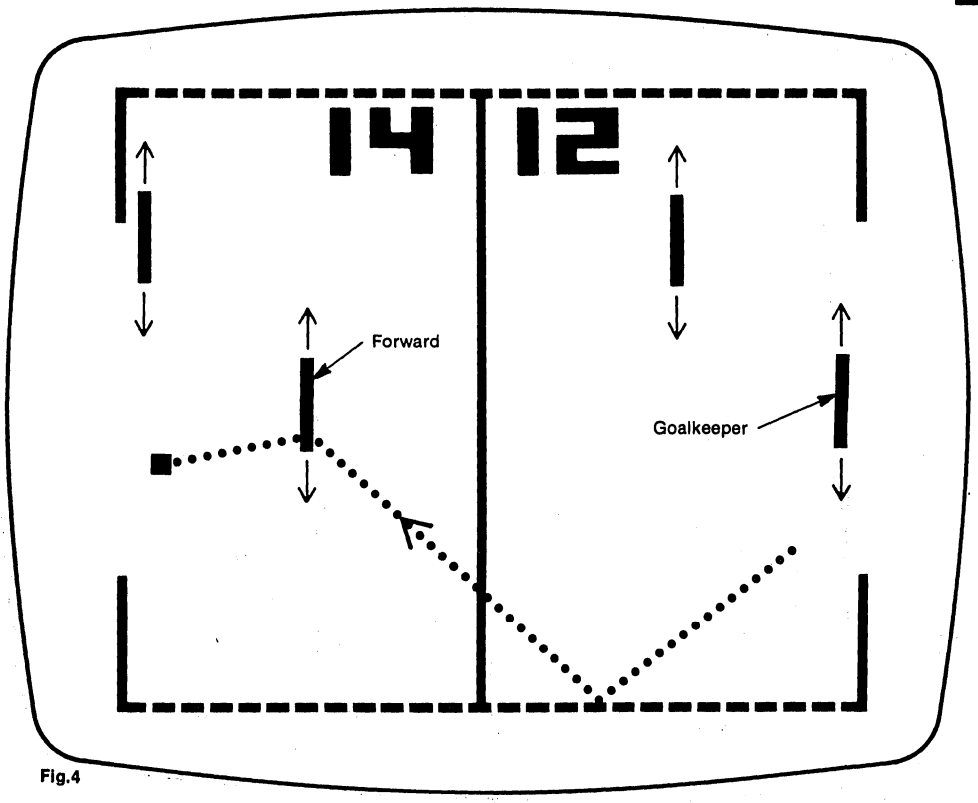


Fig.4

Soccer

The "soccer" type game is shown in Figure 4. With this game each participant has a 'goalkeeper' and a 'forward'. The layout is such that the 'goalkeeper' is in his normal position and the 'forward' is positioned in the opponent's half of the playing area.

When the game starts, the ball will appear travelling from one goal line towards the other side. If the opponent's forward can intercept the ball, (Figure 4a), he can 'shoot' it back towards the goal. If the ball is missed it will travel to the other half of the playing area and the first team's forward will have the opportunity of intercepting the ball and redirecting it forward at a new angle according to the 'player' section which is used (Figure 4b). If the ball is 'saved' by the 'goalkeeper' or it reflects back from the end boundary, the same forward will have the opportunity to intercept the outcoming ball and divert it back towards the 'goal'.

A 'score' is made in the "soccer" game by 'shooting' the ball through the defined goal area. The scoring and game control is done automatically as for the tennis game. The same audio signals are used to add atmosphere to the game.

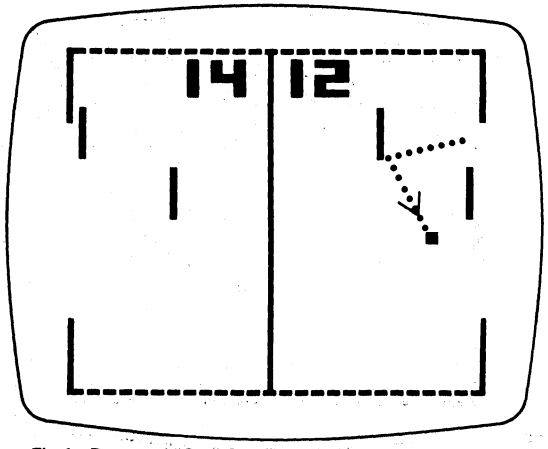


Fig.4a Return of "Goal Save"

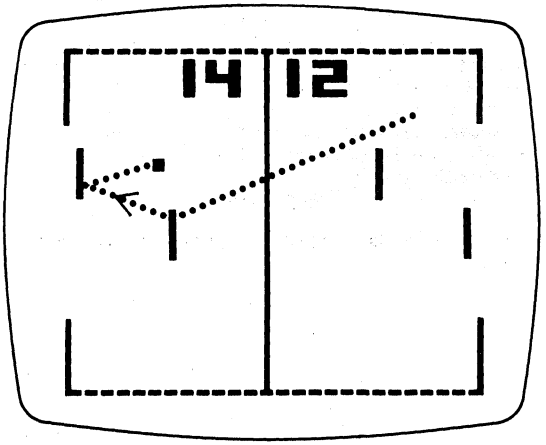


Fig.4b "Shooting" Forward

CONSUMER

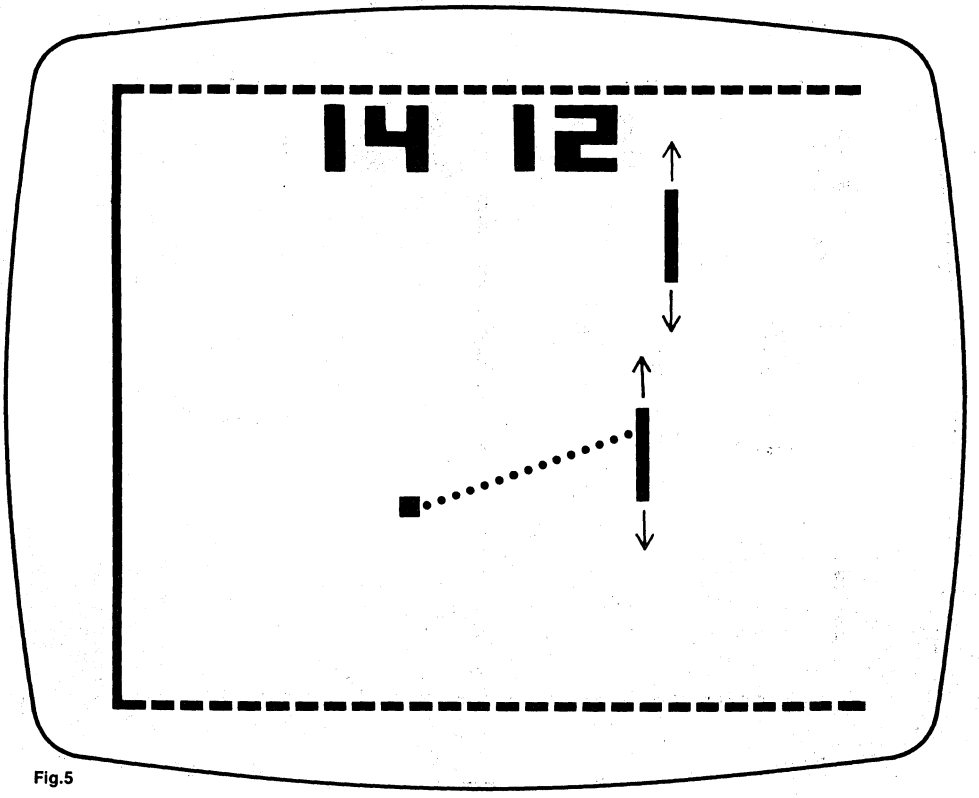


Fig.5

Squash

This game is illustrated in Fig. 5. There are two players who alternately hit the ball into the court. The right hand player is the one that hits first; it is then the left hand player's turn. Each player is enabled alternately to ensure that the proper sequence of play is followed.

Practice

This game is similar to squash except that there is only one player. See Fig. 6.

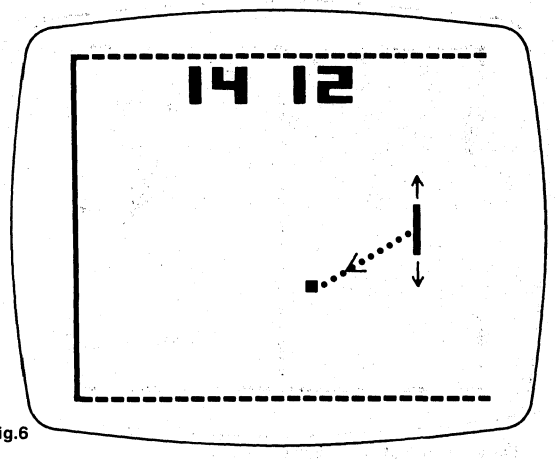


Fig.6

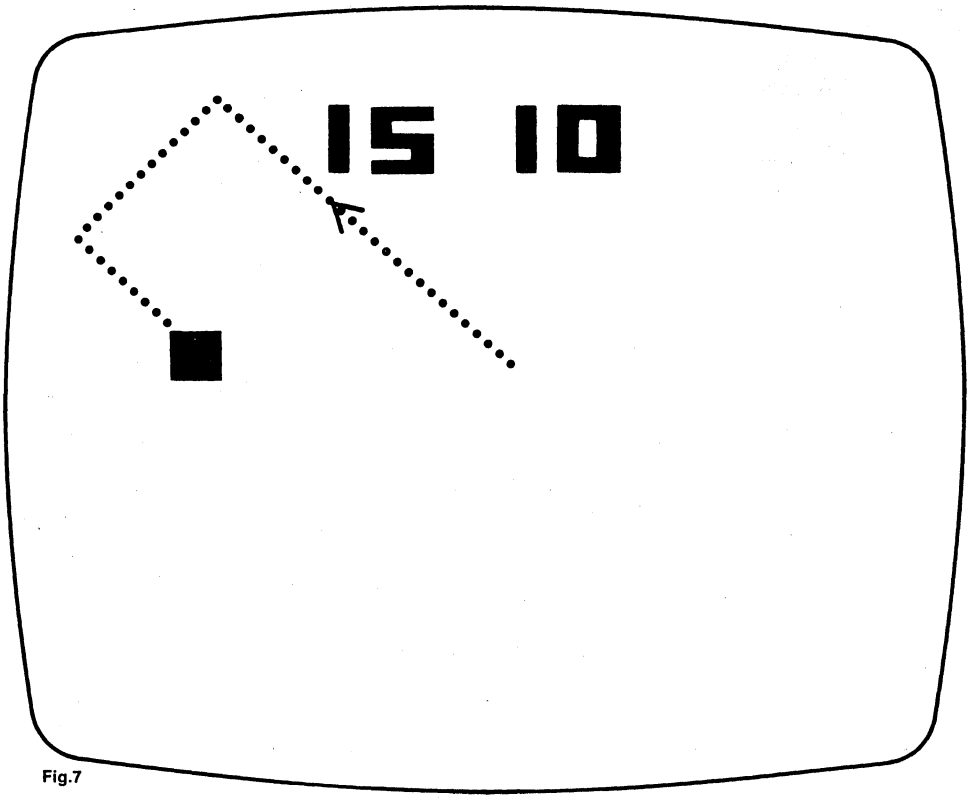


Fig.7

Rifle Game No. 1

This game is illustrated in Fig. 7. It has a large target which bounces randomly about the screen. A photocell in the rifle is aimed at the target. When the trigger is pulled, the shot counter is incremented and, if the rifle is on target, the hit counter is incremented, a hit noise is generated and the target is blanked for a short period. After 15 shots the score appears but the game can still continue without additional scoring.

Rifle Game No. 2

In this game illustrated in Fig. 8, the ball traverses the screen from left to right under control of the manual serve button. Otherwise the game is as described for Rifle Game No. 1.

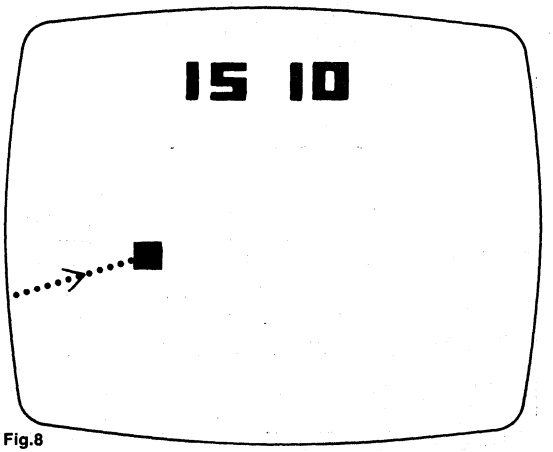


Fig.8

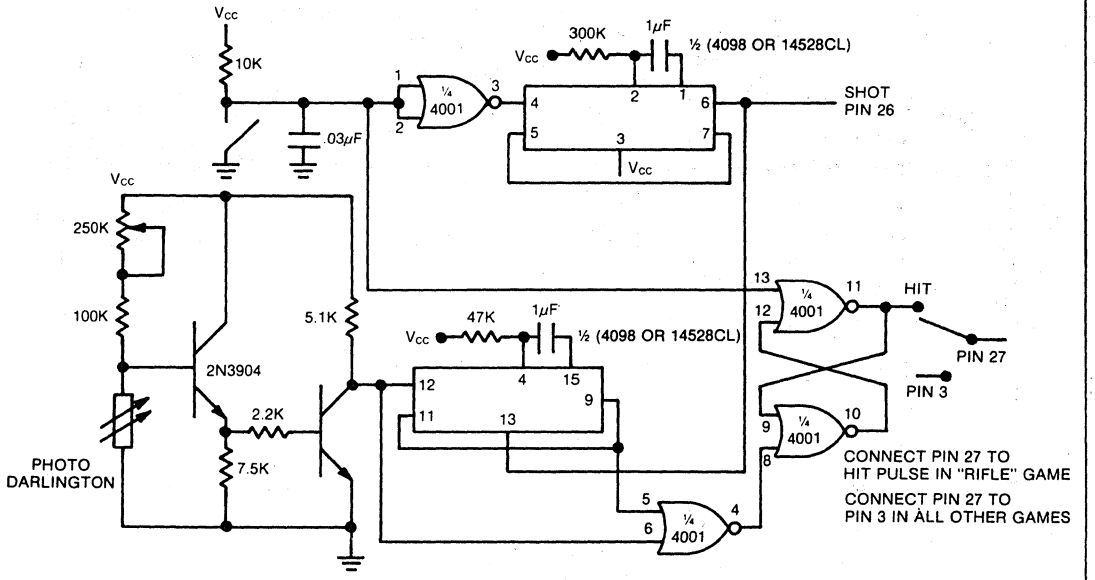


Fig.9 RIFLE INTERFACE

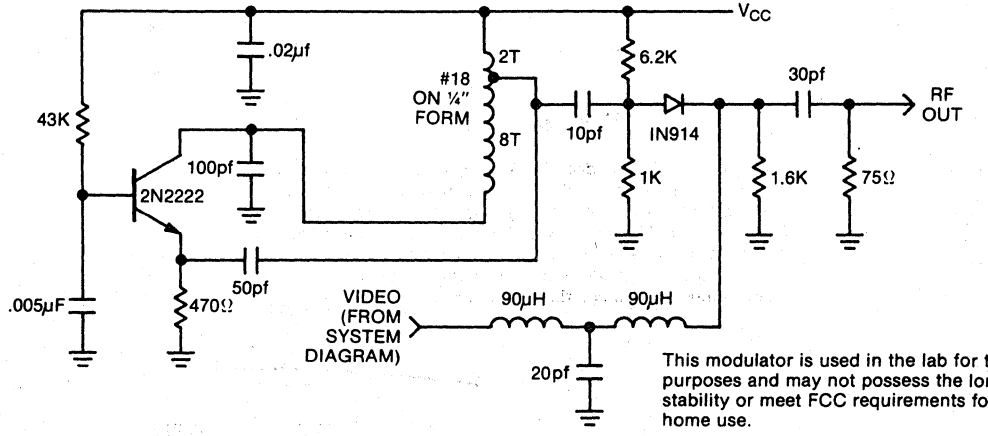


Fig.10 VHF MODULATOR

	Horizontal	Vertical
Slow	± .5μs	2 angles ± 1 line 4 angles ± 3 lines
Fast	± 1μs	2 angles ± 2 lines 4 angles ± 5 lines

Fig.11 ANGULAR MOTION

CONSUMER

RANDOM BALL SPEED/RANDOM ANGLES

To enhance the excitement and challenge of the various games, this option provides random variations of the ball speed and random changes in the ball rebound angle as the games are being played.

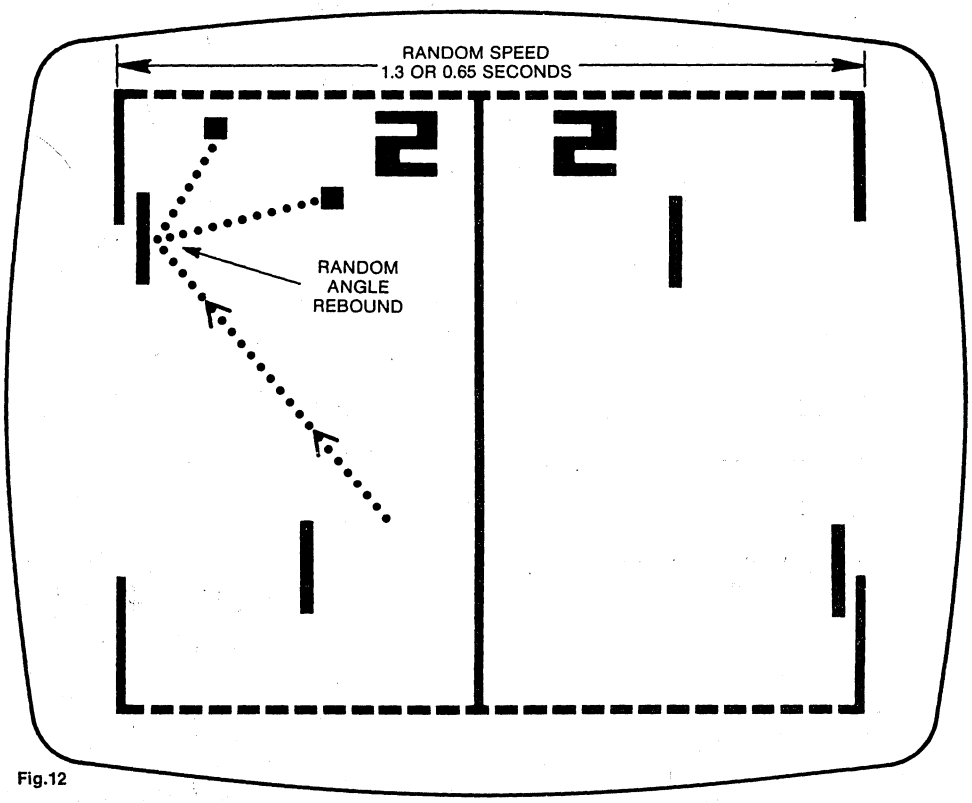


Fig.12

Soccer

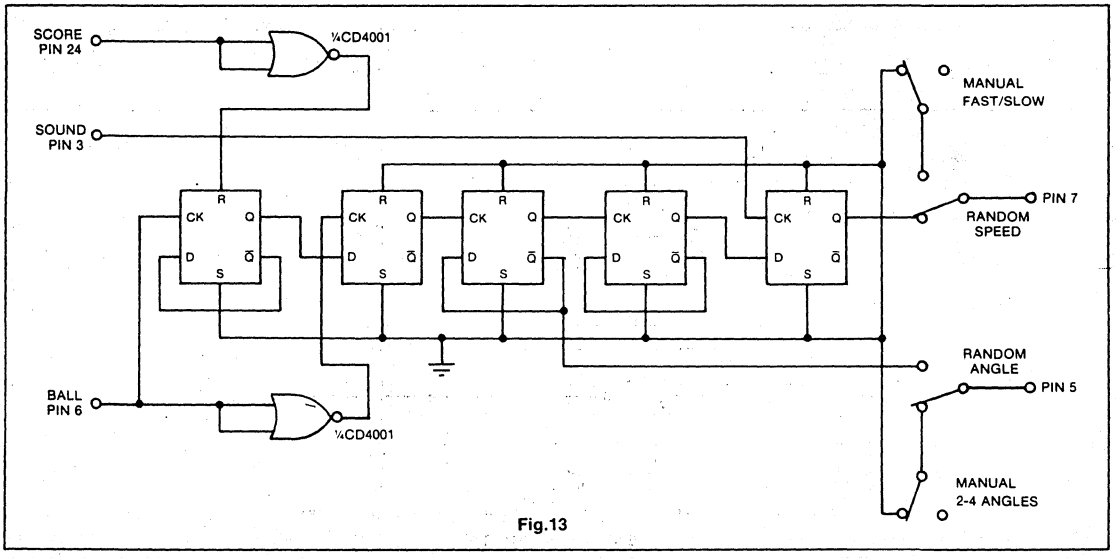


Fig.13

BLACK AND WHITE BATS/GRAY BACKGROUND

This option provides an added factor for player team recognition. The field or court is produced as a gray background with the bats in black and white. This option is particularly helpful for the squash game where the players are positioned close together.

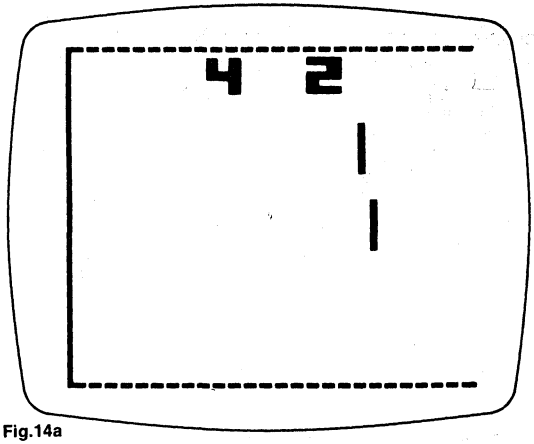


Fig.14a

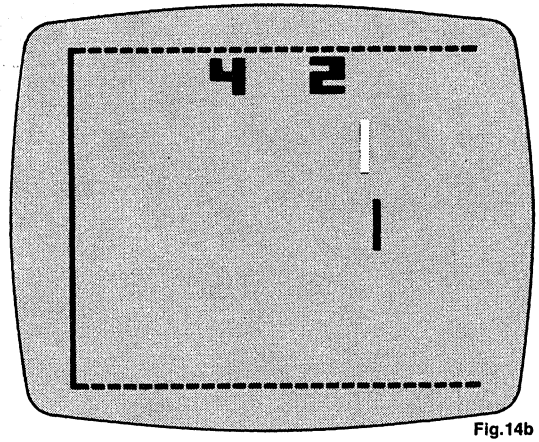


Fig.14b

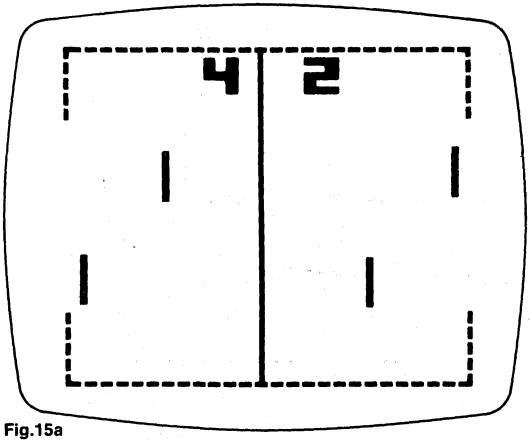


Fig.15a

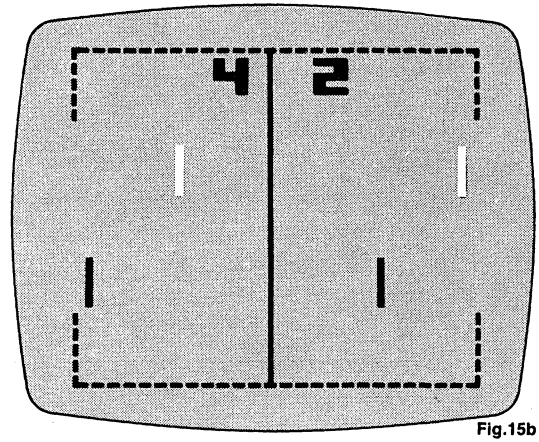
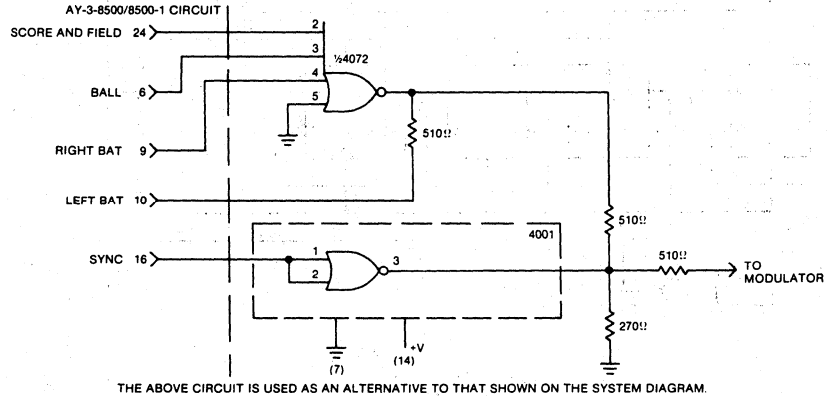


Fig.15b

CONSUMER



THE ABOVE CIRCUIT IS USED AS AN ALTERNATIVE TO THAT SHOWN ON THE SYSTEM DIAGRAM.

Fig.16 GRAY BACKGROUND

FOUR PLAYER CONFIGURATION

With this option, the basic two player tennis game can be expanded to true four player doubles. Each player is capable of playing the full width of the court.

A variation of this option allows for a three player handicap game with two players against one.

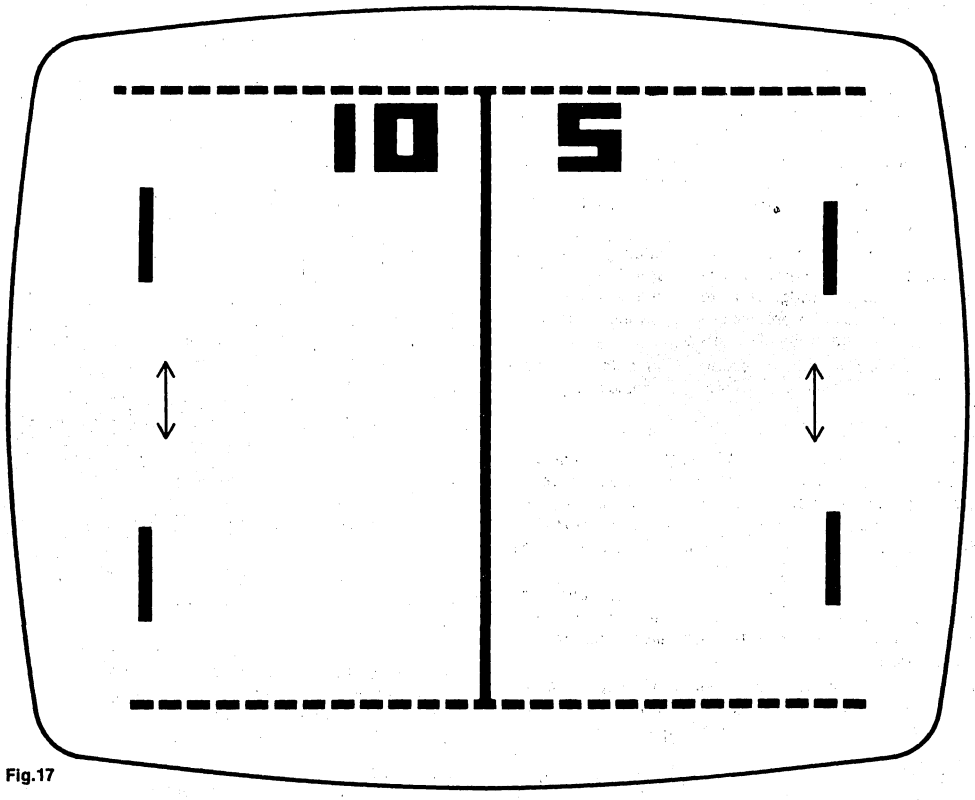


Fig.17

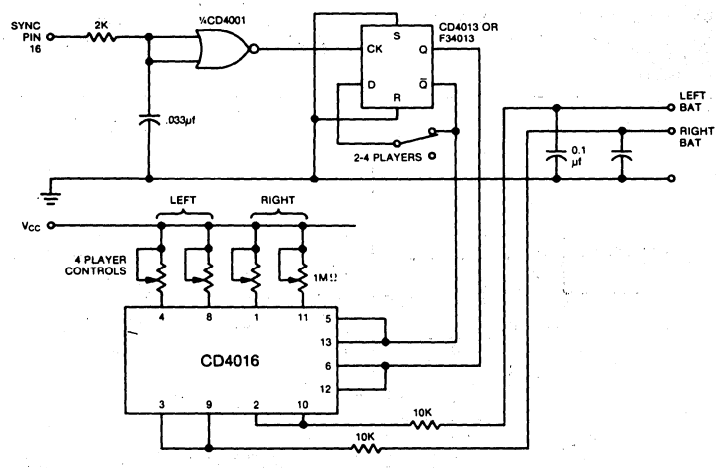


Fig.18

CONSUMER

GIMINI 8600 Series TV Games

The Gimini 8600 Series games consist of a set of single chip TV game integrated circuits which are all compatible with the AY-3-8615 Color Processor chip. This series consists of AY-3-8603/8603-1 Roadrace, AY-3-8605/8605-1 Warfare, AY-3-8606/8606-1 Wipeout, AY-3-8607/8607-1 Rifle, AY-3-8610/8610-1 Supersport, and AY-3-8765 Motorcycle chips. Circuit descriptions giving detailed information on each game chip are in the following pages of this section.

The TV games may be configured as dedicated games when packaged with the color processor and peripheral circuitry. When packaged as individual cartridges, able to be connected to a main console containing the color processor and peripheral circuitry, the game becomes programmable by its user.

The following block diagram shows a programmable game configuration which can be combined to provide a dedicated game if desired.

DESCRIPTION

The console consists of a resident AY-3-8615 game/color processor, an R.F. video modulator, a calculator type keyboard for game selection, a set of three skill select switches, and a game reset switch. Attached to the console are the player controllers which can consist of joysticks or a variety of controls suited to the game.

The console need never be opened once in operation; all changes to the system are plugged in externally. The cartridges and controls are the only items that are altered to give the 8600 system new game characteristics.

The block diagram shows the basic system with its expandability. Detailed console schematics for NTSC color and CCIR black and white are shown in Figs. 2 and 3 respectively.

SECTION A

There are three switches that will allow skill selections. These skills will be determined by the specific game cartridge and will control speeds, sizes and shapes of objects in any particular game cartridge. A fourth switch acts as game reset.

SECTION B

The game selections will be made by a maximum of ten momentary switches similar to the calculator keyboard. Again the number of games is determined by the cartridge.

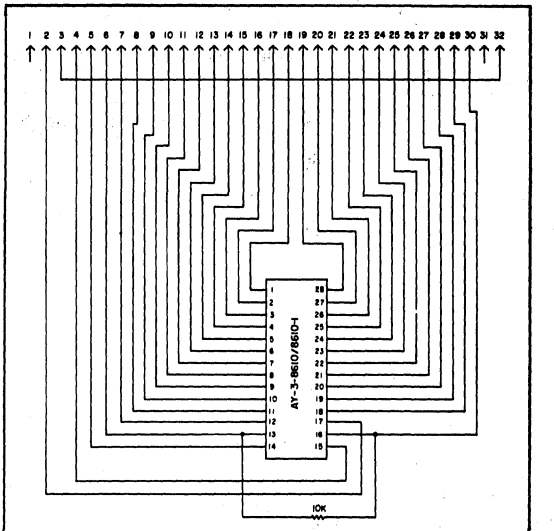


Fig. 1 AY-3-8610/8610-1 CARTRIDGE

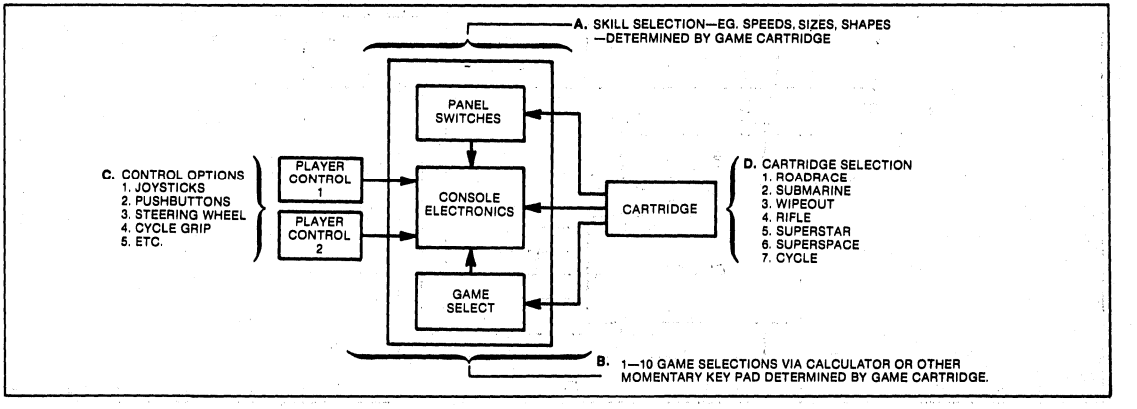
SECTION C

The controls are always in pairs to allow for two players. Depending on the game cartridge, a variety of controls may be used. Basically most games can be controlled by resistance joysticks. If controls are remote, the connectors used should be a minimum of six pins each to allow for game flexibility.

SECTION D

The cartridges will all be compatible with the console and a variety will be offered. Each cartridge will give the game a completely new objective. The cartridge should have a minimum of 34 pins to allow for special connections such as sound effects, etc., and remain compatible with the system.

Fig. 1 illustrates as an example the straightforward layout for the AY-3-8610/8610-1 Supersport game cartridge.



CONSUMER

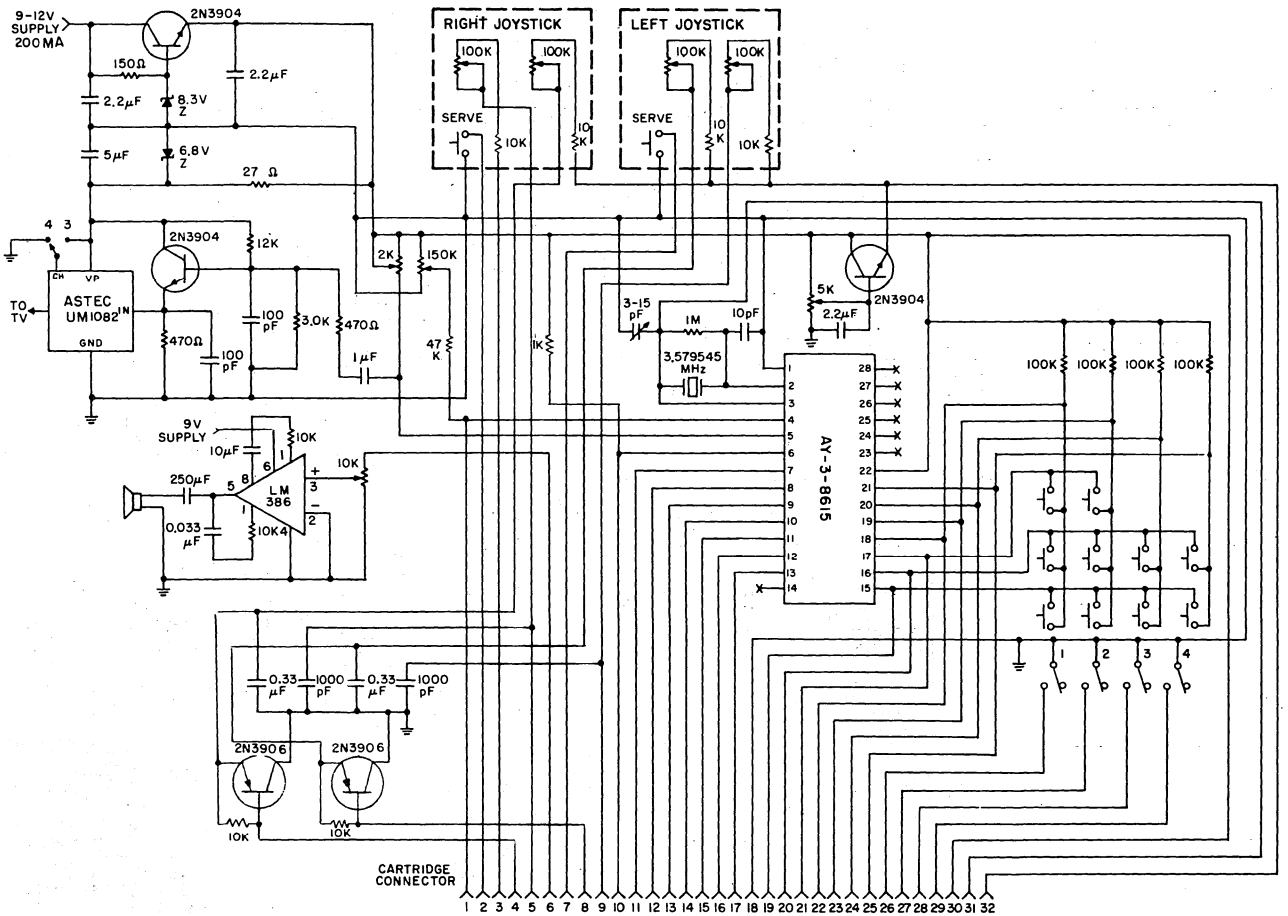


Fig. 2 GIMINI ECONOMY "8600" CONSOLE: NTSC COLOR

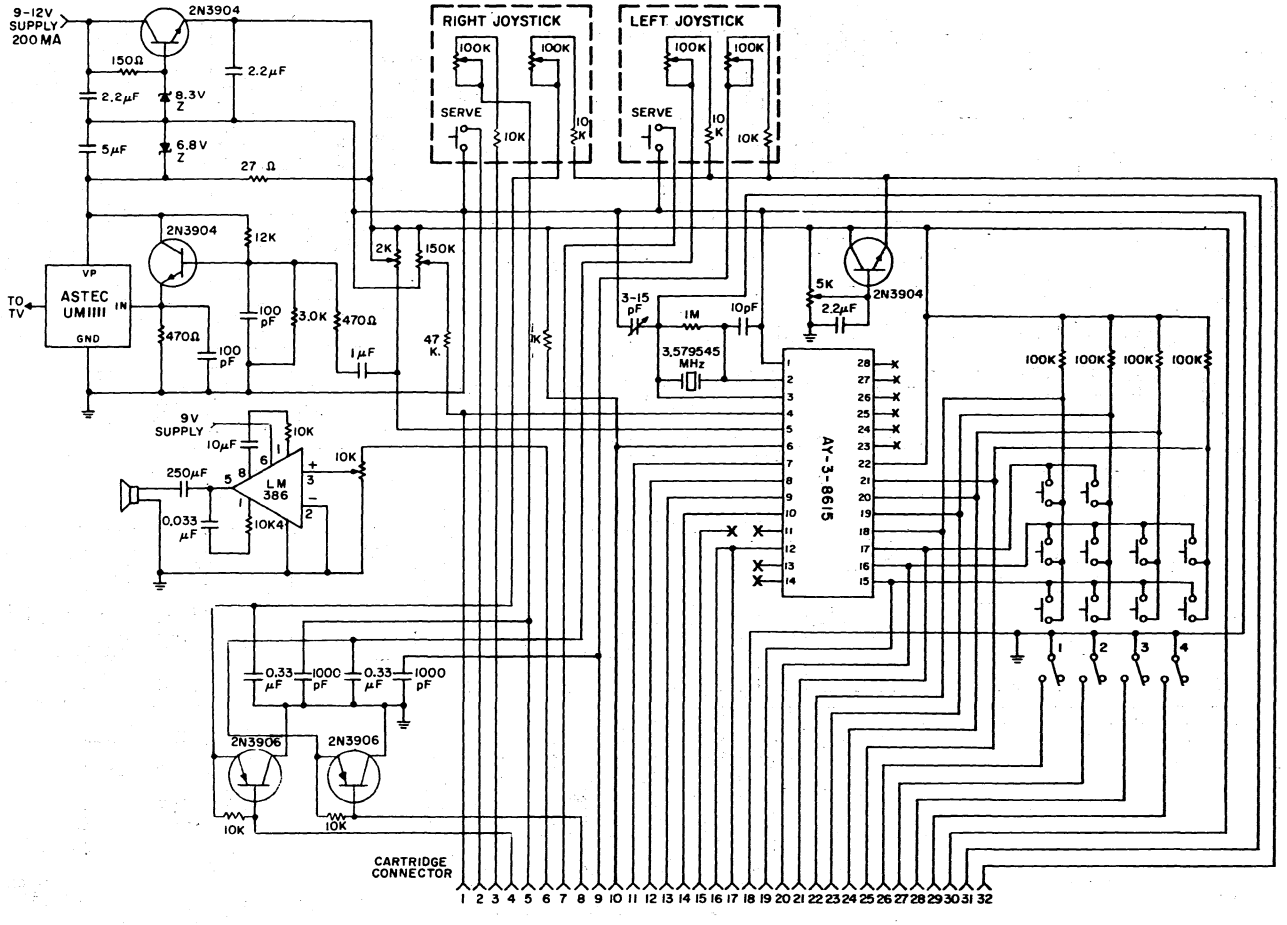


Fig. 3 GIMINI ECONOMY "8600" CONSOLE: CCIR B/W

Roadrace

FEATURES

- Two game selections—one and two player games
- T.V. raster generator
- All timing signals for color or black and white application
- Direct compatibility with Economy "8600" game console
- Automatic on-screen scoring
- Score color-keyed for each player
- Skill selection for difficult or easy driving conditions
- Realistic motor and crash sound generation with a minimum of external components

DESCRIPTION

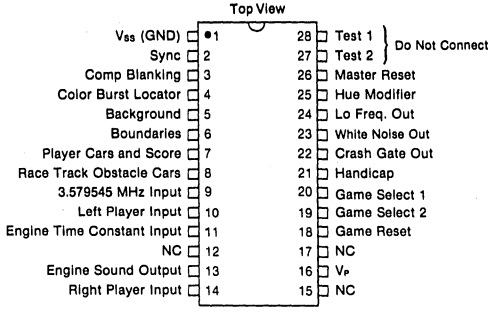
The AY-3-8603/8603-1 game circuit has been designed to provide a realistic roadrace game using a standard television receiver. The circuit is intended for color or black and white usage with a 525 (AY-3-8603-1) or 625 (AY-3-8603) line receiver. The circuit is designed to be either a stand-alone game or an add-on for the Gimini Economy "8600" game series.

OPERATION

The AY-3-8603/8603-1 utilizes two potentiometers to produce control voltages for the horizontal positioning of the race cars. Each player controls his own car. The circuit displays a score for each driver, processes the game logic and produces composite sync, color burst location and blanking signals for a 525 or 625 line T.V. receiver. Sound outputs are also included to produce simulated engine and crash sounds with a minimum of external components. The AY-3-8603/8603-1 are designed to be operated with the AY-3-8615 color circuit.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... −0.3 to +12V
Storage temperature range ..... −20°C to +70°C
Ambient operating temperature range ..... 0°C to 40°C
Operating voltage supply range ..... +7.5 to +9V

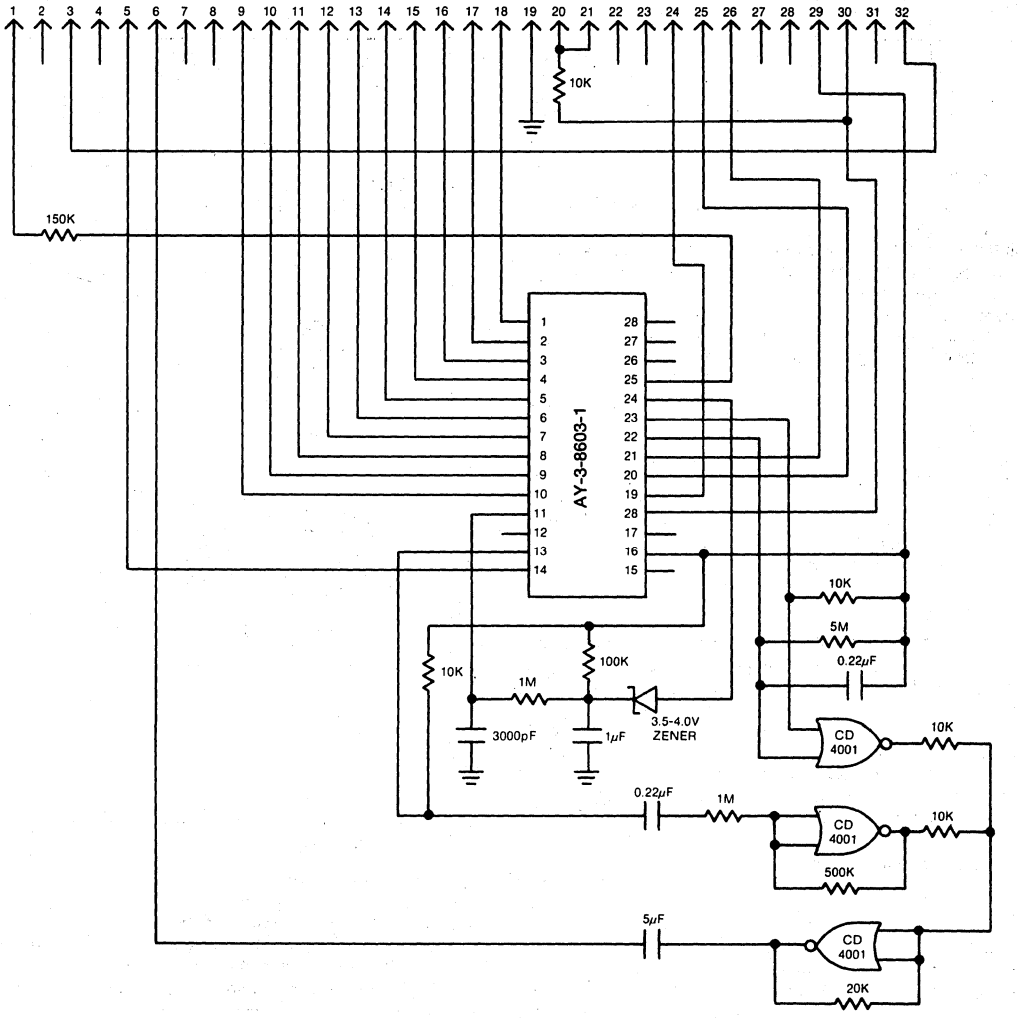
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

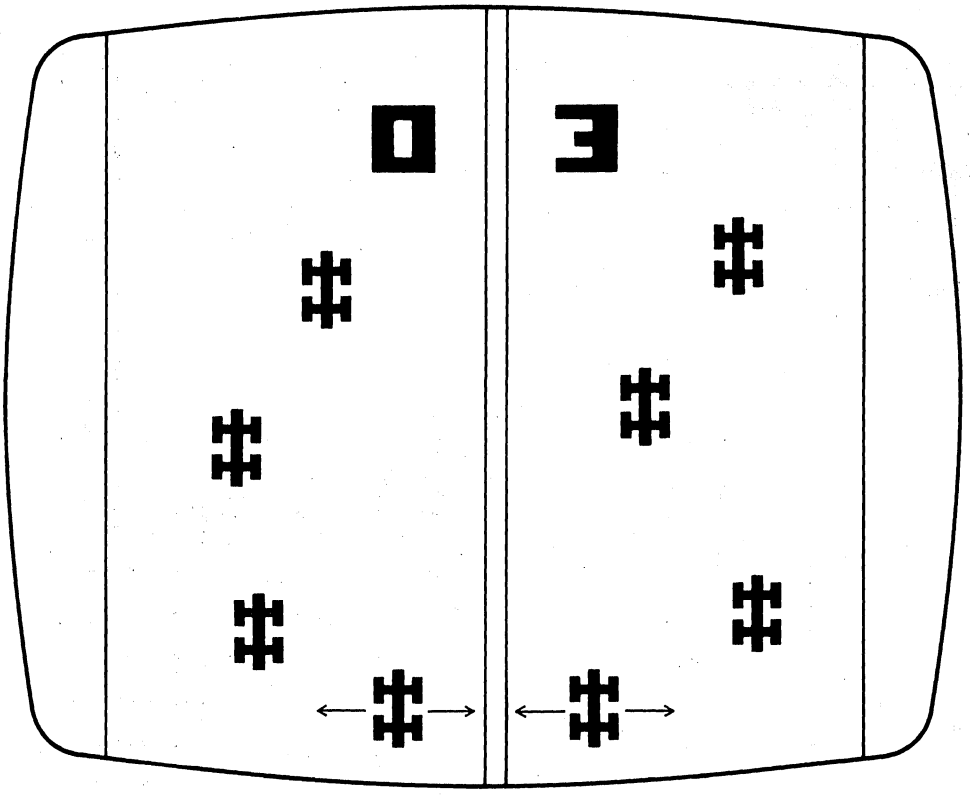
Standard Conditions (unless otherwise stated)

Parameter values at $T_a = 25°C$

Characteristic	Min	Typ	Max	Units	Conditions
Clock Input					
Frequency	—	3.579545	—	MHz	
Logic '0'	0	—	0.5	V	45-55% duty cycle
Logic '1'	V_p-2	—	V_p	V	
Leakage	—	—	—	—	
Control Input					
Logic '0'	0	—	0.2	V	Max. contact resistance of 1K to V_{SS}
Logic '1'	V_p-2	—	V_p	V	
Input Impedance	—	100	—	Kohms	Pull up to VP
Output pins	—	—	1	V	I_{out} = 2mA
On Off	—	1000	—	μA	$V_{out} = V_p$
Power Supply Current	—	—	60	mA	at V_p = 7.5V

CONSUMER


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
10K
150K
AY-3-8603-1
1 2 3 4 5 6 7 8 9 10 11 12 13 14
28 27 26 25 24 23 22 21 20 19 28 17 16 15
10K
5M
0.22μF
10K
100K
1M
3.5-4.0V ZENER
3000pF
1μF
CD 4001
10K
0.22μF
1M
CD 4001
10K
500K
5μF
CD 4001
20K



Roadrace (2 player)/ Qualify (1 player)

A typical T.V. screen display for the game is shown above. One driver for each car located at the bottom of each track controls his horizontal position only. After the game is reset the game starts as the picture produced simulates a race track in motion where each driver must maneuver his car around the other cars on the track. Both tracks have the same random obstacle car pattern with two visible per track, the pattern on the right is 24 lines ahead of the left pattern. This produces random cars on both tracks at one time with the same degree of difficulty for each driver. Video speeds increase every two seconds up to a maximum of seven speeds forward or until either player crashes his car into an obstacle car. Upon a crash, the video motion will stop and a crash sound will be generated. When the game restarts, the forward motion will start from slow and progress in speeds once again.

Simulated engine sound is produced during the game. The engine starts from low and increases in pitch at four second intervals during motion to simulate shift points during the game progress. Every crash scores one point for the opponent. Scores are shown over each track.

The one-player game selection removes the car image on the right track and left driver plays. A point is scored for the driver after passing every eight consecutive obstacle cars. Every crash gives the game, (right track) score one point. The first player or game to score 15 ends the game in either one or two player selection.

Warfare

FEATURES

- Outputs include NTSC (AY-3-8605-1) or CCIR (AY-3-8605) compatible composite sync, color burst location and blanking
- Operation from a 3.579545 clock
- One or two player game
- Digital on-screen scoring
- Sound generation for engine, sonar, firing and explosions
- Designed for use with AY-3-8615
- Outputs and power requirements compatible with the Gimini Economy "8600" game series

DESCRIPTION

The AY-3-8605/8605-1 game circuit has been designed to provide realistic sea and space battle games using a standard television receiver. The circuit is intended for use with a 525 (AY-3-8605-1) or 625 (AY-3-8605) line receiver.

OPERATION

The AY-3-8605/8605-1 utilizes two potentiometers (one for each player) or one axis of two joysticks to produce control voltages for internal Schmitt triggers. These position the submarine, destroyer, and spaceships, via rate controllers in the horizontal axis only. The circuit displays an on-screen score for each player, processes the game logic and produces a composite sync, color burst location and blanking signals for a 525 or 625 line T.V. receiver. Sound outputs are also included to produce simulated engine, sonar, firing, and explosion sounds with a minimum of external components.

The AY-3-8605/8605-1 may be operated with the AY-3-8615 color processor circuit. The outputs are designed for compatibility within the Gimini Economy Game series. Game selection is made via a 2 strobe/3 select switch matrix with momentary contacts. Two momentary switches that ground the "fire" input pins are used to activate the torpedoes, depth charges, and missiles.

SOUND OUTPUTS

Space background noise—7 Bit Polynomial Counter clocked at 2kHz rate.

Torpedo or Depth Charge fired—1kHz signal for 2 frames then off for 4 frames.

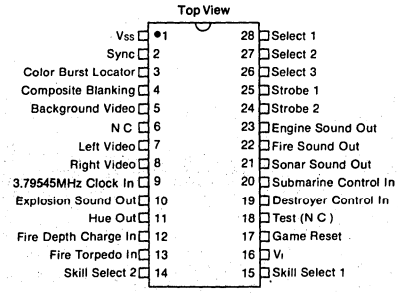
Explosion— ∿ 8kHz signal for∿ 3½ seconds.

Destroyer engine—Fast sound is a 240Hz clock into a 4 bit poly counter—Slow sound is a 120Hz clock rate.

Sonar for Submarine—Decaying 480Hz signal for ∿ 2.9 seconds followed by a 2kHz signal burst for∿ 200ms. This sound repeats every 3½ seconds.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



MOVEMENT

The cargo ship will traverse the screen in 16 seconds.

The destroyer ship will traverse the screen in 5.3 seconds.

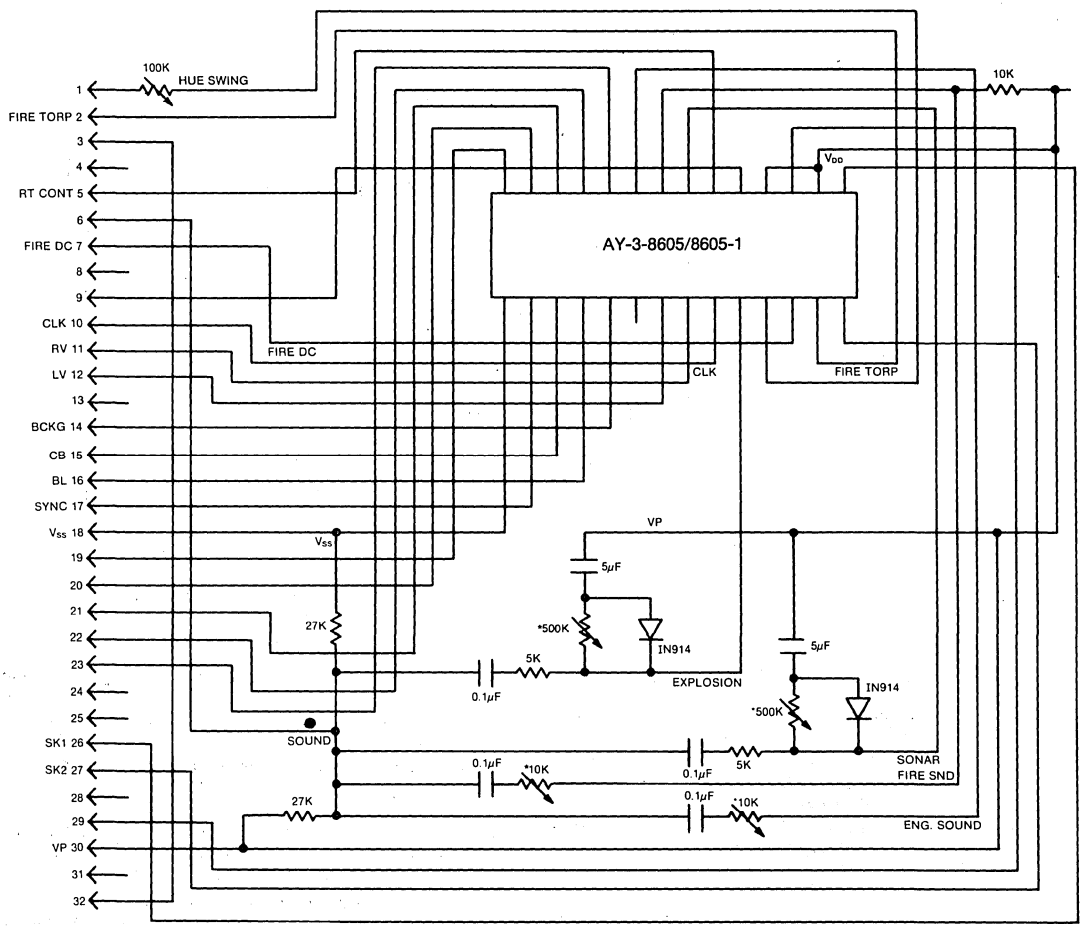
The submarine moves across the screen in 8 seconds.

The torpedo rises at a rate of 1 line per frame. To move the 100 lines to hit the destroyer will take 1.67 seconds.

The depth charge falls at a rate of 1 line every 2 frames. To hit the submarine will take 3.34 seconds.

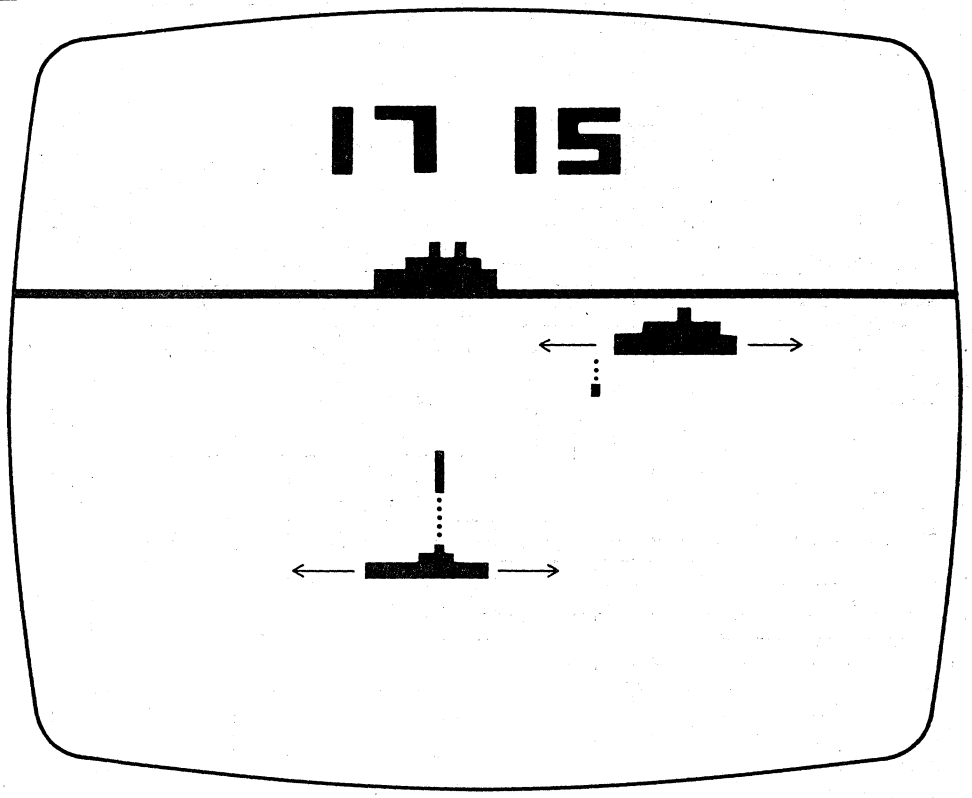
CONSUMER

WARFARE CARTRIDGE



*POTENTIOMETERS MAY BE REPLACED WITH FIXED RESISTORS AFTER DETERMINING RESISTANCE USED FOR BEST SOUND EFFECTS.

CONSUMER



Sea Battle (2 player)

One player controls the horizontal movement of the destroyer and the other player controls the horizontal movement of the submarine. The engine sound of the destroyer will be fast for either left or right movement and slow for no movement. Both the submarine and the destroyer will stop for a center position of the joystick. The cargo ship moves across the upper part of the screen at a fixed speed. The submarine player fires torpedoes to score 1 point for hitting the cargo ship and scores 2 points for hitting a restricted area of the destroyer. If the SKILL Switch #1 is off, the submarine player scores a point if the torpedo hits any area of the destroyer.

The destroyer player drops depth charges at the submarine and scores a point for hitting an area close to the submarine and scores 2 points for a direct hit if the SKILL Switch #2 is on.

A hit of the torpedo on the cargo ship or the destroyer will cause the cargo ship to disappear for the duration of the explosion and the destroyer ship will change color. A depth charge hitting the submarine will cause the submarine to change colors during the explosion.

Neither ship is allowed to go off-screen and only one torpedo will appear on the screen at any time, rising from the submarine to either strike a ship and cause an explosion or disappear. Only one depth charge will appear on the screen at any time, falling from the destroyer to explode on the submarine or disappear when hitting the sea bottom.

Sounds include a destroyer engine, submarine sonar, depth charge or torpedo firing, and explosions. The game is over when either player scores 30 points.

Counterattack I (1 player)

One player controls the horizontal movement of the submarine and fires torpedoes at the destroyer ship. There is no cargo ship in this game. The destroyer ship moves across the screen dropping depth charges. As the depth charge falls it will either hit the submarine and cause an explosion or hit the sea bottom and drop another depth charge.

The player scores 1 point if the torpedo hits any area of the destroyer (SKILL Switch #1 is off). 2 points are scored if the torpedo hits a restricted area of the destroyer and SKILL Switch #1 is on. Points against the player are scored if the depth charges hit the submarine. 1 point is scored for a hit close to the submarine and 2 points for a direct hit if SKILL Switch #2 is on.

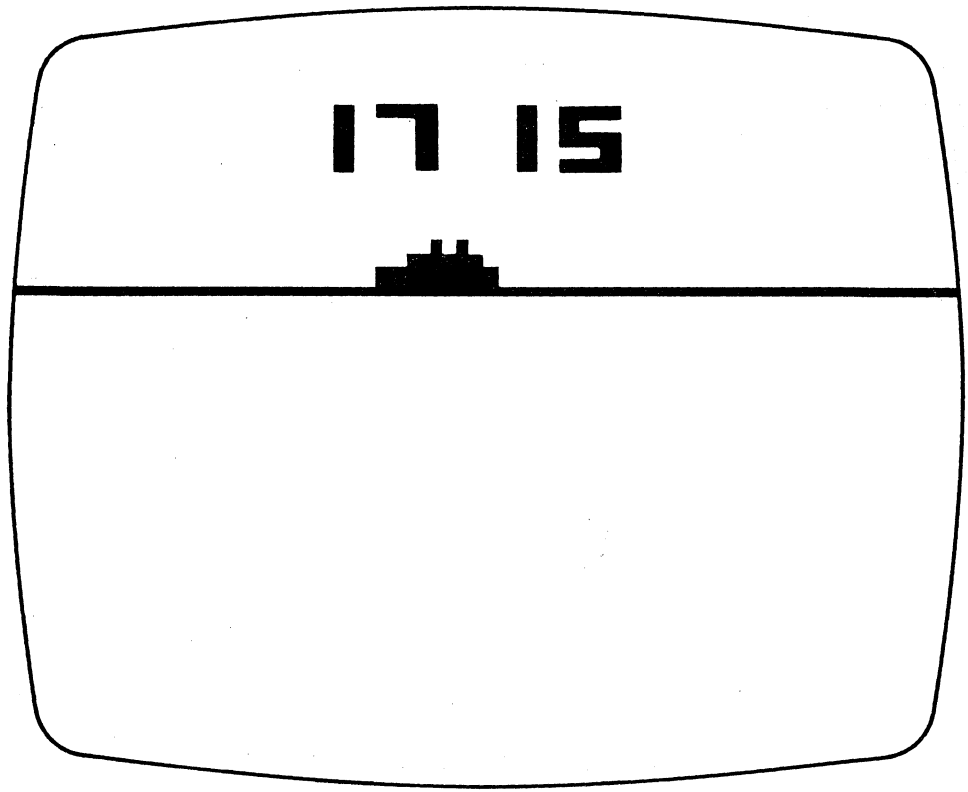
When either ship has been hit an explosion will occur and the ship that was hit will change color. It is possible that both ships have been destroyed at the same time.

The sounds include the destroyer ship engine, submarine sonar, torpedo firing, and explosions. The game is over when either the player scores 30 points or the destroyer has accumulated 30 points.

Counterattack II (1 player)

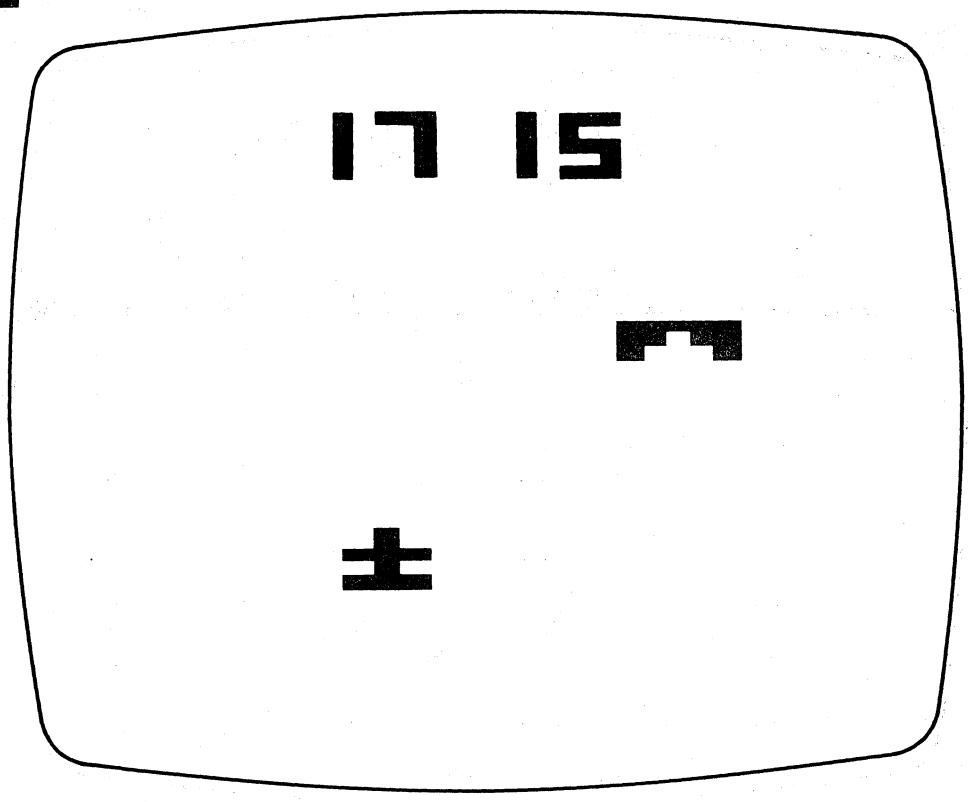
One player controls the horizontal movement of the destroyer and the firings of the depth charges. This player must protect his ship and the cargo ship from the torpedoes fired automatically from the submarine. As the submarines torpedoes destruct from a ship impact, another torpedo is launched after the 3½ second explosion. Torpedoes that miss the destroyer ship or the cargo ship will disappear in the air and a new torpedo will be launched. The submarine moves across the screen reversing its direction at each edge of the screen.

The scoring for this game is the same as for the previous games. The sounds include the destroyer ship engine, submarine sonar, depth charge firing, and explosions. The game is over when either the player scores 30 points or the submarine has accumulated 30 points.



Night Battle (2 player)

One player controls the horizontal movement of the destroyer and the other player controls the horizontal movement of the submarine. The cargo ship traverses the screen, changing directions when it reaches the edge of the screen. This game plays just like the 2 player - Sea Battle - except that the only time the submarine is visible is when a torpedo has been fired. Likewise the cargo ship and the destroyer are not visible until a depth charge has been dropped. Scoring, SKILL Switch selections, and sounds are the same as described in - Sea Battle -.



Space Battle I (2 player)

One player controls the Space Warp 1 vehicle and the other player controls the Space Warp 2 vehicle. Missiles are fired from one ship toward the other. There is no equivalent of a cargo ship from the sea battle games in this space game. The object is to fire your missiles at your opponent's vehicle and score either 1 or 2 points for the type of hit dependent on the SKILL Switch setting. The sounds include a space background and sounds for missile firings and explosions. The game is over when either player reaches 30 points.

Space Battle II (2 player)

This two player game is very similar to the Space Battle I game except that the space vehicle is only visible when it has fired a missile.

Wipeout

FEATURES

- Outputs include NTSC compatible composite sync, color burst location and blanking for AY-3-8606-1 and CCIR for AY-3-8606
- Operation from a 3.579545MHz clock
- One or two player games
- Digital on-screen scoring
- Sound generation for tones to indicate hits of ball to bat, ball to objects, and ball to border
- Designed for use with AY-3-8615
- Outputs and power requirements compatible with Gimini Economy "8600" Game Series to allow plug-in operation

DESCRIPTION

The AY-3-8606/8606-1 game circuit has been designed to provide an active paddle/squares game using a standard television receiver. The circuit is intended for use with a 525 (AY-3-8606-1) or 625 (AY-3-8606) line receiver.

OPERATION

The AY-3-8606/8606-1 utilizes two potentiometers (one for each player) one axis only of each joystick to produce control voltages for internal Schmitt triggers. These position the player's bats in the vertical axis only to allow play of the game. The circuit displays an on-screen score color coded to each player, processes the game logic and produces a composite sync, color burst location and blanking signals for a standard 525 (625 for AY-3-8606) line TV receiver. Sound output is also included to produce tonal sounds for ball hits to bats, ball hits to borders and ball hits on objects with a minimum number of external components.

The AY-3-8606/8606-1 is made to be operated with the AY-3-8615. The outputs are designed for compatibility within the Gimini Economy "8600" Game Series. Game selection is made via a 4 strobe, 3 select switch matrix with either fixed or momentary contact closures.

Two momentary switches that ground the input serve control pins are used to start the ball into motion after reset or when a reserve is necessary according to game rules. Three skill selection switches are used to determine game difficulty.

GAME OPERATION

Select 1 Strobe 1 (Game #1)

This game selection uses a playing area as shown in Figure 1. It is a single-player game in which the player manipulates the paddle in the vertical axis after manually serving the ball. The objective is to wipe out as many boxes as possible in the seven serves that are allowed during a single game.

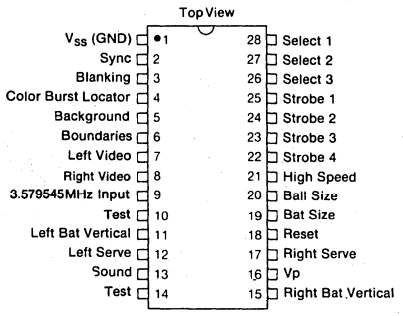
Select 1 Strobe 2 (Game #2)

This game selection uses a playing area as shown in Figure 2. It is a single-player game in which the player manipulates two paddles at each end of the playing area in the vertical axis after manually serving the ball. The objective is to wipe out as many boxes as possible in the seven serves that are allowed during a single game.

Select 1 Strobe 3 (Game #3)

This game selection uses a playing area as shown in Figure 3. It is a two-player game in which each player manipulates his paddle at the ends of the playing area in the vertical axis. The ball is served by the last player to score after game is in play. The objective is to wipe out all boxes in the playing area. The winner ends with the highest score.

PIN CONFIGURATION
28 LEAD DUAL IN LINE.



Select 1 Strobe 4 (Game #4)

This game selection uses a playing area as shown in Figure 4. It is a two-player game in which each player manipulates his paddle at the ends of the playing area in the vertical axis. The ball is served by the last player to score after the game is in play. The objective is to wipe out all the boxes in the playing area. The winner ends with the highest score. The ball will rebound off the center barrier.

Select 2 Strobe 1 (Game #5)

This game selection uses a playing area as shown in Figure 5. It is a single-player game in which the player manipulates two different colored paddles at each end of the playing area in the vertical axis after manually serving the ball. The objective is for the player to wipe out as many correct colored objects depending on which color paddle hits the ball into the playing area as possible. The game ends when all of one color objects are wiped out.

Select 2 Strobe 2 (Game #6)

This game selection uses a playing area as shown in Figure 6. It is a two-player game in which each player manipulates his paddle at the ends of the playing area in the vertical axis. The ball is served by the last player to score after the game is in play. The objective is to wipe out as many boxes color coordinated with the player's paddle. The first color completely wiped out wins.

Select 2 Strobe 3 (Game #7)

This game selection uses a playing area as shown in Figure 7. It is a two-player game in which each player manipulates his paddle at the ends of the playing area in the vertical axis. The ball is served by the last player to score after the game is in play. The objective is to wipe out as many boxes color coordinated with the player's paddle. The first color completely wiped out wins.

CONSUMER

Select 2 Strobe 4 (Game #8)

This game selection uses a playing area as shown in Figure 8. It is a single-player game in which the player manipulates the paddle in the vertical axis after manually serving the ball. The object is to wipe out as many color coordinated boxes with the player's paddle as possible in the seven serves that are allowed during a single game. The ball alternates colors on each rebound, thus it can only hit one color square to wipe out and is transparent to the other color at any one time. After a hit and rebound, the ball can wipe out the opposite color square.

Select 3 Strobe 1 (Game #9)

This game selection uses a playing area as shown in Figure 9. It is a single-player game in which the player manipulates the paddle in the vertical axis after manually serving the ball. The objective is to break through the end wall and score on as many blocks as possible. The game ends after either seven serves or the first breakthrough.

Select 3 Strobe 2 (Game #10)

This game selection uses a playing area as shown in Figure 10. It is a two-player game in which each player manipulates his paddle in the center of the playing area in the vertical axis. The ball is kept in motion by each player trying to protect the wall behind his paddle. If a player misses a hit with the paddle, the ball will hit the wall and one block will disappear and the score will increment for the opposite player. The objective of this game is to knock out as many blocks to get a high score before breaking through the wall. The first player to hit the ball through an open section of a wall ends the game.

NOTE: If the ball hits the left wall at a point where three blocks connect from the lower edge, the block in the same direction as the trajectory will disappear. See Figure 11.

SKILL SELECTION

The games mentioned in Section 4.0 can be made more difficult by selecting one or more of the following skills:

1. Bat Size (left player only)
2. Ball Size (in large ball size, bat must hit center of ball)
3. Ball Speed

A ground on any of these function pins shall:

1. Halve the bat size
2. Halve the ball size
3. Double the ball speed

ELECTRICAL CHARACTERISTICS

Maximum Ratings *

Voltage on any pin with respect to V_n pin ..... −0.2V to 12V
Storage temperature range ..... −20°C to +70°C

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

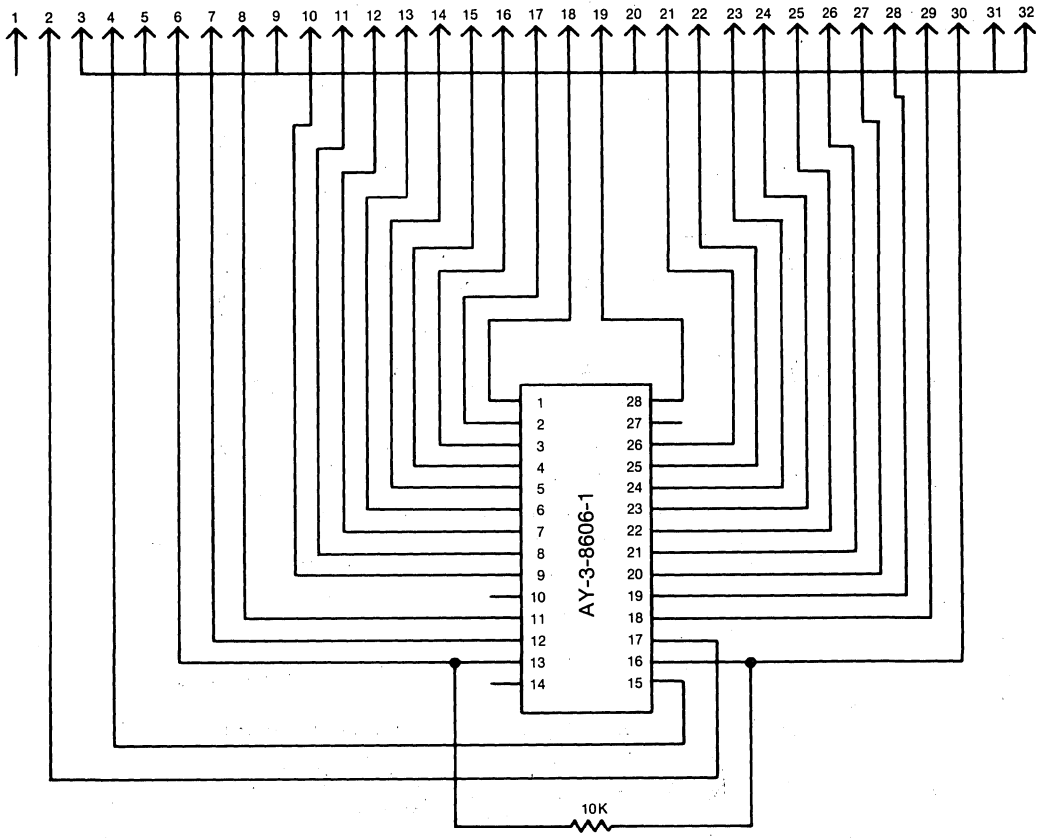
Standard Conditions (unless otherwise stated)

V_p = +7.5 to +9.0 volts
Ambient operating temperature range 0°C to +40°C
Characteristics at +25°C and V_p = 7.5V

Characteristics	Min	Max	Units	Conditions
CLOCK INPUT				
Frequency	—	—	MHz	
Logic '0'	0	0.5	V	45-55% duty cycle
Logic '1'	V_p-2	V_p	V	
Leakage	—	100	μA	
CONTROL INPUT				
Logic '0'	0	0.5	V	May contact resistance of 1K to V_n
Logic "1"	V_p-2	V_p	V	
Input Impedance	—	→	Kohms	
OUTPUT PINS 2-8, 13				
ON	—	1	V	I_{out} = 2mA
OFF	—	100	μA	V_{out} = V_p at 7.5V
OUTPUT PINS 22-25				
ON	—	1.0	V	I_{out} = .5mA
OFF	—	100 μA	μA	V_{out} = V_p (open drain)
Power Supply Current	—	75	mA	

CONSUMER

GIMINI ECONOMY 8600 GAME
AY-3-8606-1 CARTRIDGE



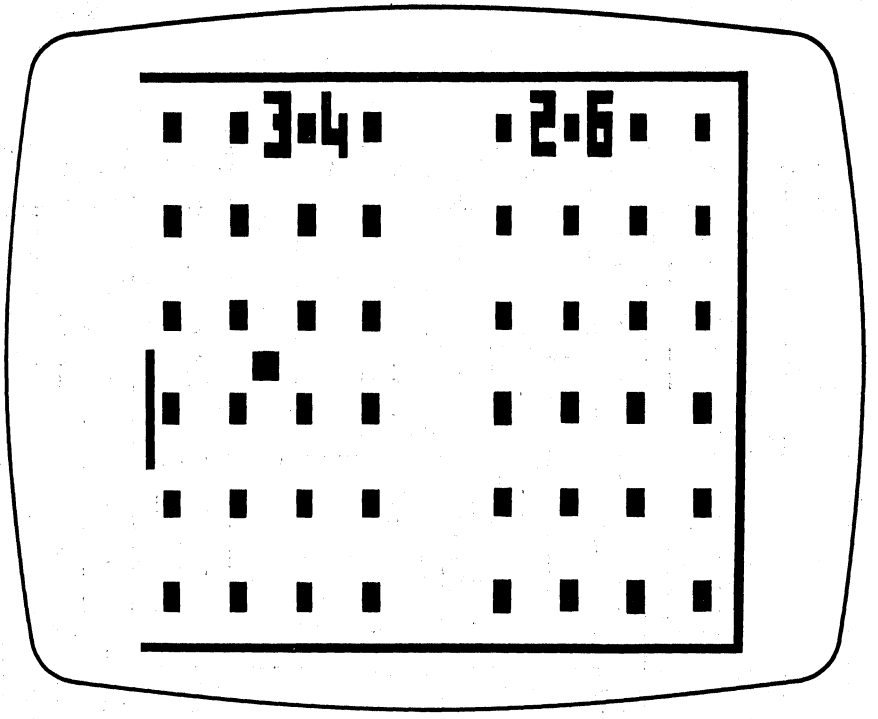


Fig. 1

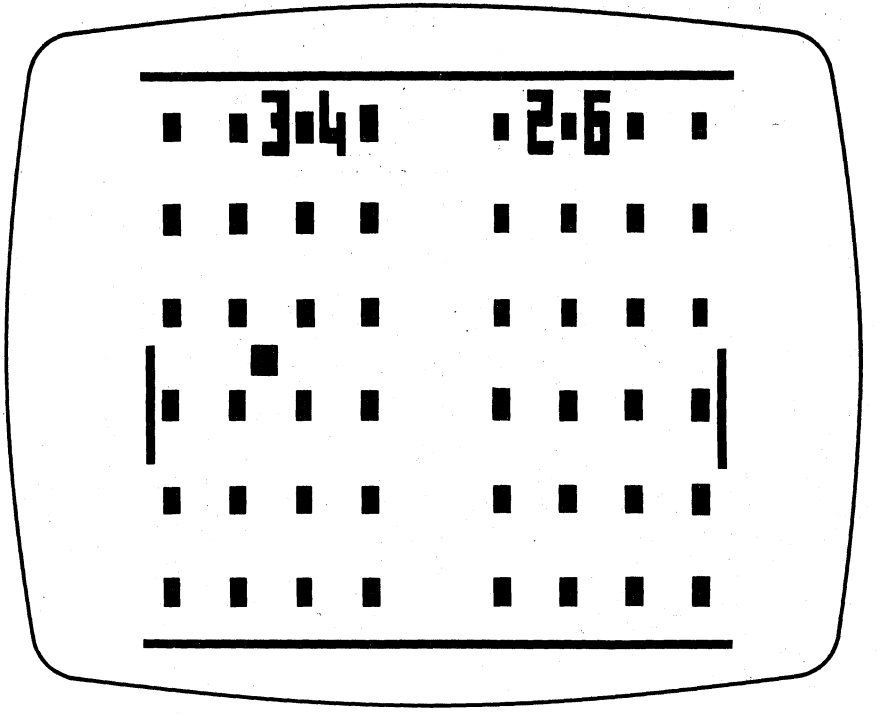


Fig. 2

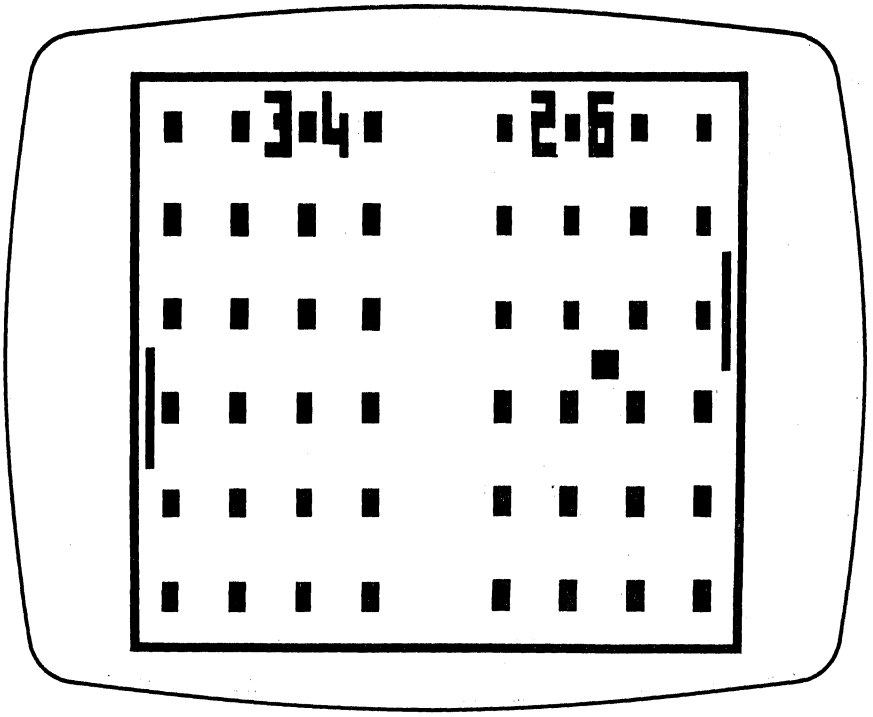


Fig. 3

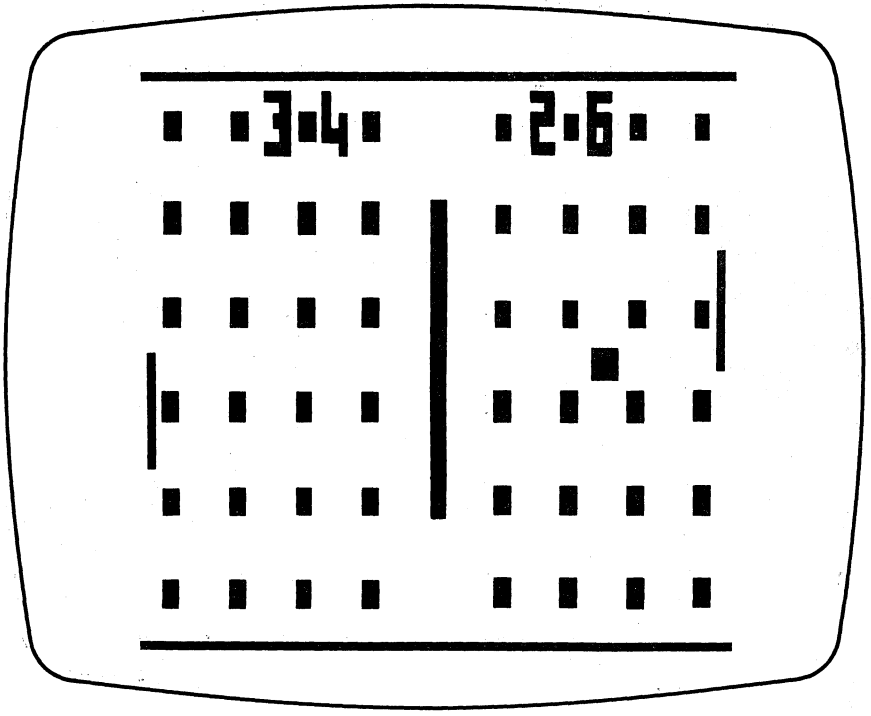


Fig. 4

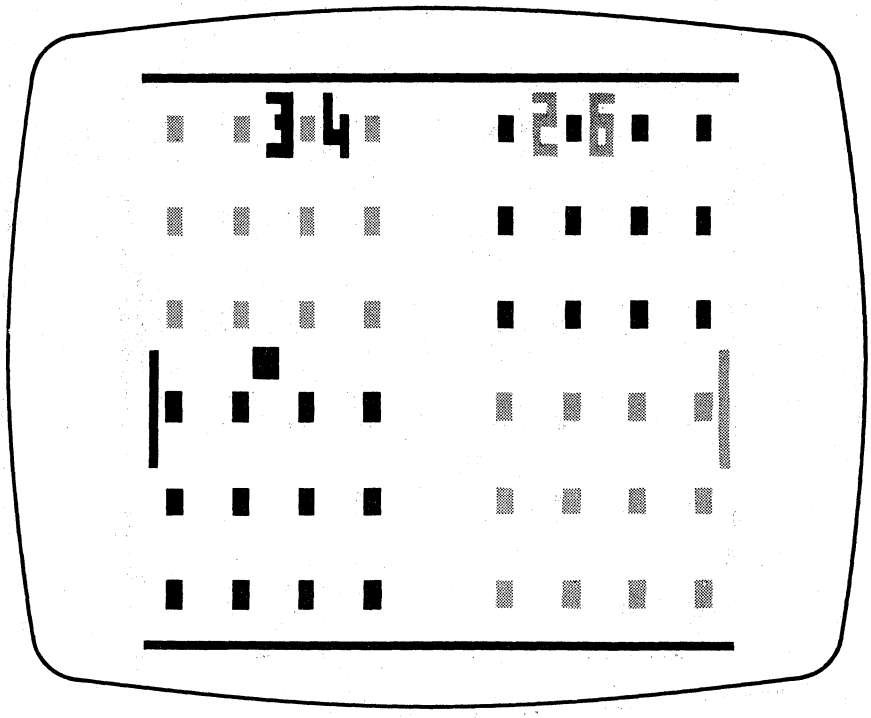


Fig. 5

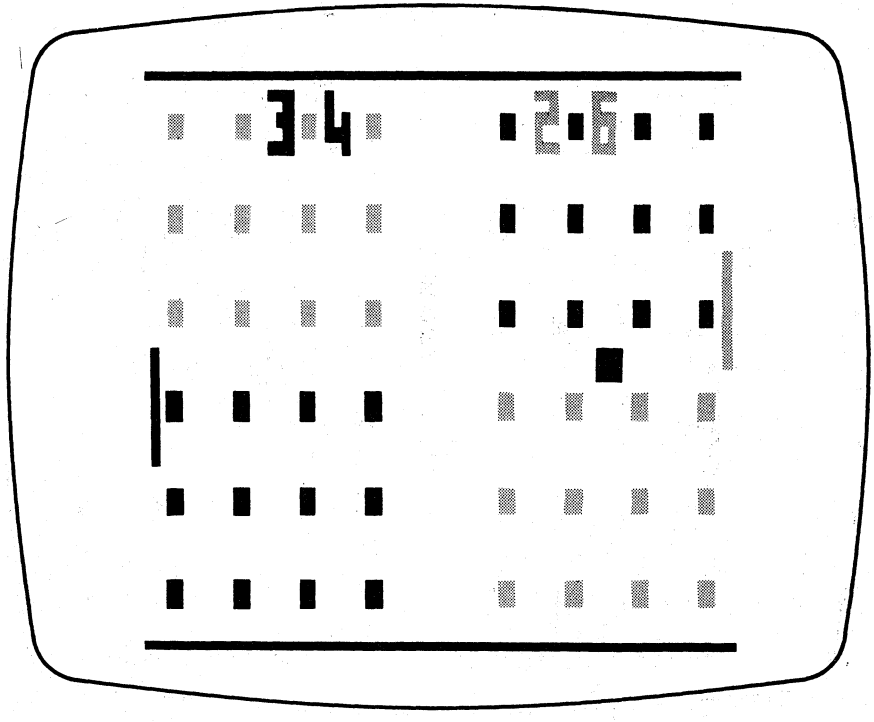


Fig. 6

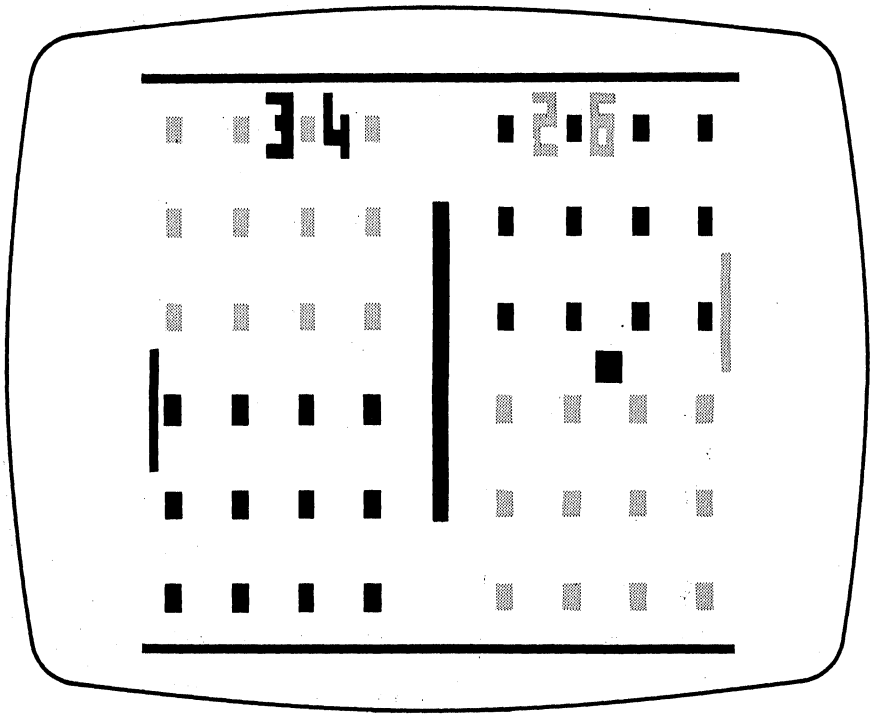


Fig. 7

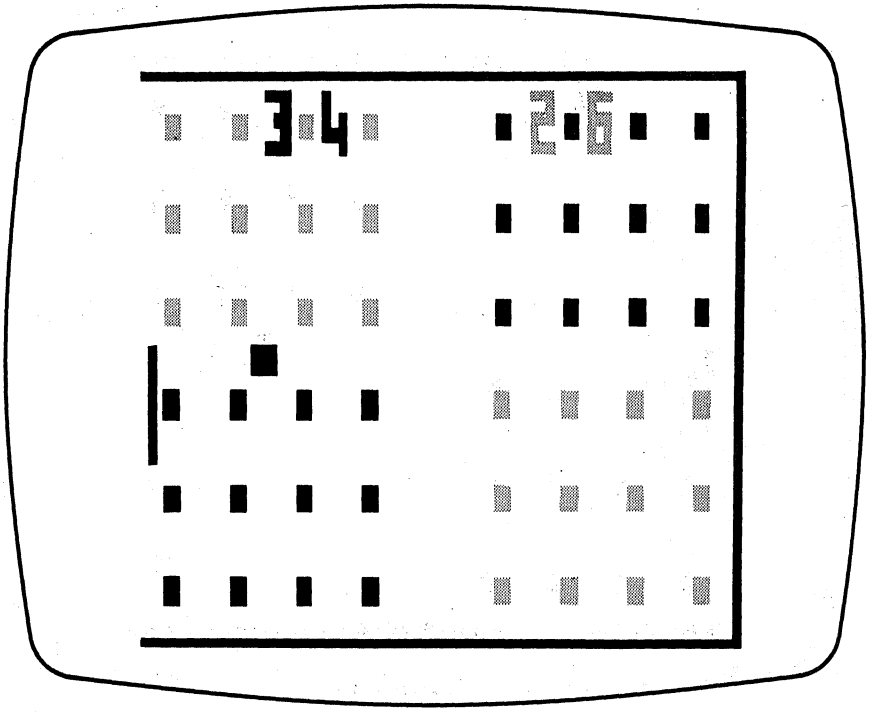


Fig. 8 NOTE: Ball alternates color with every hit against shapes.

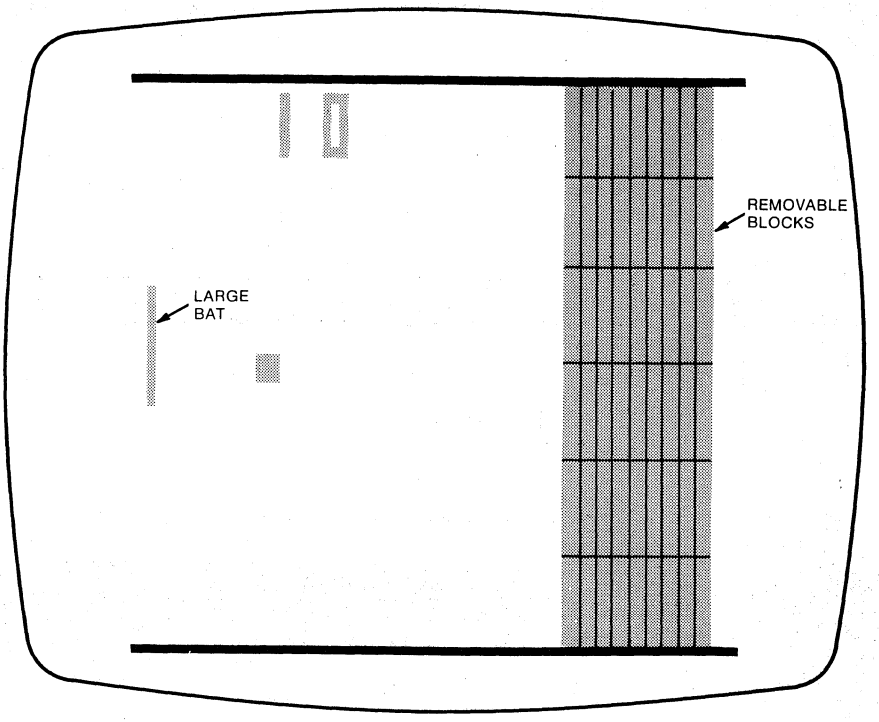

10
REMOVABLE BLOCKS
LARGE BAT

Fig. 9

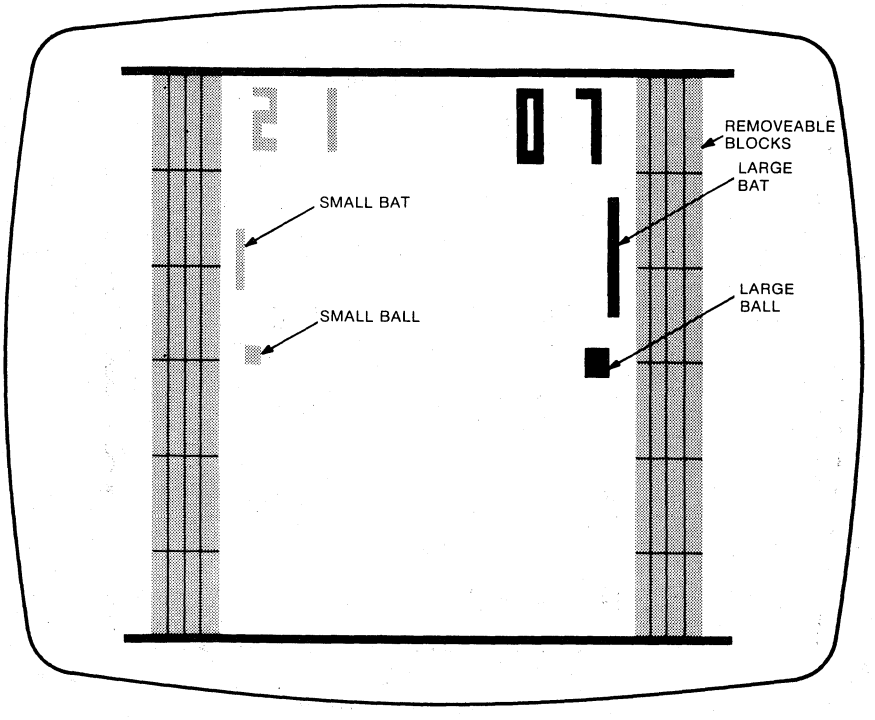

21
07
REMOVEABLE BLOCKS
LARGE BAT
SMALL BAT
LARGE BALL
SMALL BALL

Fig. 10

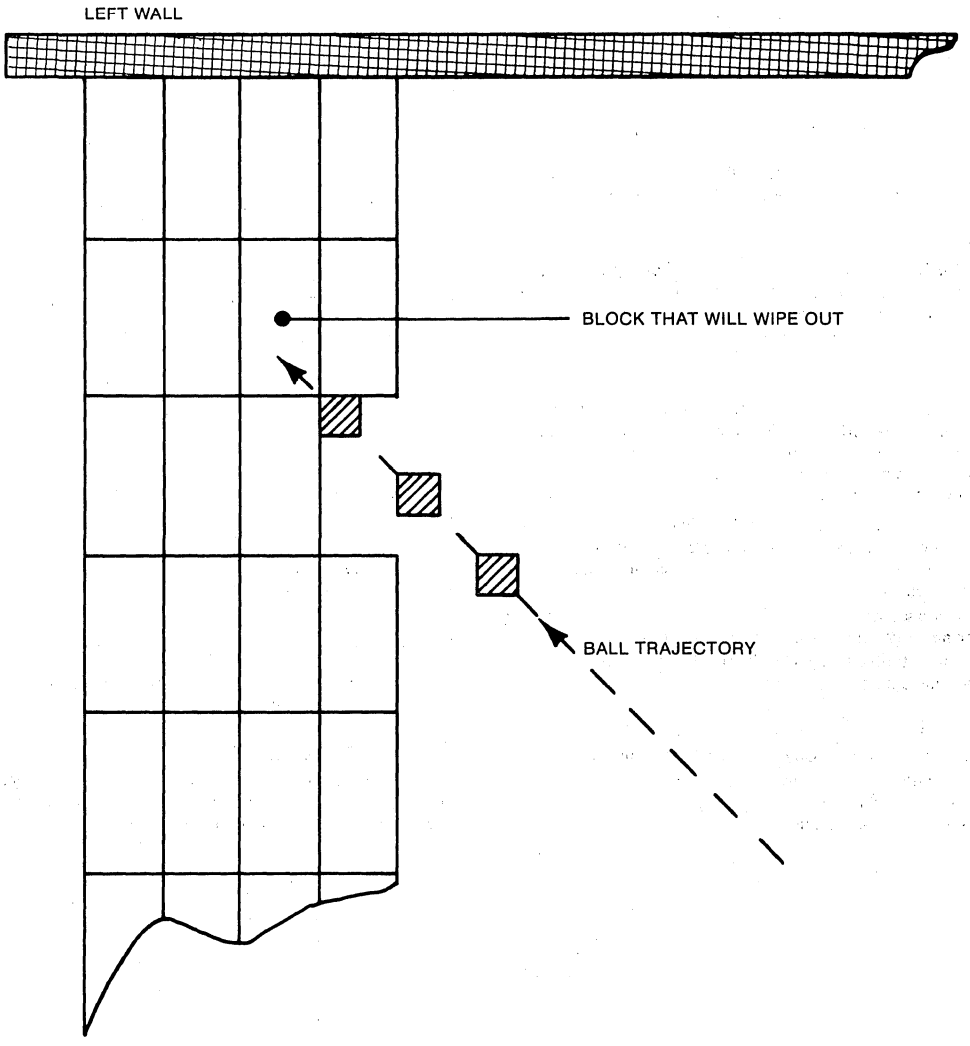


Fig. 11

Shooting Gallery

FEATURES

- Outputs include NTSC (AY-3-8607-1) or CCIR (AY-3-8607) compatible composite sync, color burst location and blanking
- Operation from a 3.579545MHz clock
- One or two player game
- Digital on-screen scoring
- Sound generation for flight, fall, hit and impact
- Designed for use with AY-3-8615
- Outputs and power requirements compatible with Gimini Economy "8600" Game Series to allow plug-in operation.

DESCRIPTION

The AY-3-8607/8607-1 game circuit has been designed to provide an active series of target games using a standard television receiver. The circuit is intended for use with a 525 (AY-3-8607-1) or 625 (AY-3-8607) line receiver.

OPERATION

The AY-3-8607/8607-1 utilizes an external photo cell mounted in a gun or rifle for recording hits. The logic requires the gun to input a shot pulse when the trigger is pulled and if the photocell in the gun records the hit (if on target) a pulse will be transmitted to the chip. (No pulse if off target).

Some of the two-player games require two guns.

With the two-player game where one player controls the target and the other shoots, the joystick in the console will be used for target control.

Skill select switches on the console are used for (1) target size large or small (2) target speed, fast or slow. In two-player/two-rifle games, the left joystick is used for additional handicapping/skill selection.

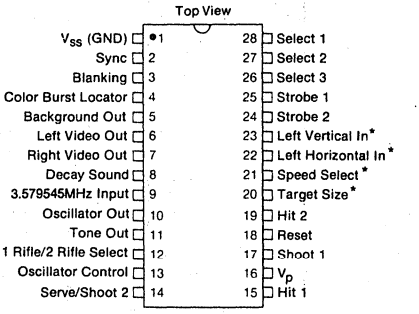
GAME SKILLS

All games will have difficulty selection in the following areas:

A. Two speeds for the target — fast and slow.
B. Two sizes for the target — large and small.
C. Joystick-selected handicap.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



*Pin functions are for one-player games.
For two-player games, the functions of pins 20 thru 23 are:

20—Player 1 Target Size
21—Player 1 Speed Select
22—Player 2 Target Size
23—Player 2 Speed Select

These selections are to be made on two pins which will make one selection (the easiest) when left open.

ON SCREEN SCORING

All scoring will be displayed on the screen momentarily after each flight or target sequence to show an update of the game in progress. Score is flashed at end of game.

CONSUMER

CIRCUIT OPERATION

The AY-3-8607 utilizes an external photo cell mounted in a gun or rifle for hits made. The logic requires the gun to input a shot pulse when the trigger is pulled and if the photocell in the gun records the hit (if on target) a pulse will be transmitted into the chip (no pulse if off target).

Some of the two-player games require two guns.

With the two-player game where one player controls the target and the other shoots, the joystick in the console will be used for target control.

Skill select switches on the console are used for (1) target size, large or small (2) target speed, fast or slow. In two player two rifle games left joystick is used to give handicapped skill selections.

GAME SELECTIONS

Select	Strobe	1 Gun	2 Guns
1	1	Attack II	Attack IV
2	1	Target I	Target III
3	1	Target II	Target IV
1	2	Skeet I	Skeet III
2	2	Skeet II	Skeet IV
3	2	Attack I	Attack III

GAME DESCRIPTIONS

Skeet I

This game selection uses a playing area as shown in Figure 1. It is a single-player game in which the player tries to shoot a target on the screen with an external gun. The target moves from the foreground into the background and the player is allowed one shot to be taken per flight. The target can start from either the right or the left side of the screen at random. When either the hit count or the number of flights reaches 15 the game ends.

Skeet II

This game selection uses a playing area as shown in Figure 1. It is a two-player game in which one player tries to shoot the target and the other player controls the direction in which the target flies with the horizontal axis of the joystick, and also controls the start of flight with the left "serve" button. The target moves from the foreground into the background and the player with the gun is allowed one shot to be taken per flight. The game ends when either the hit count or the number of flights reaches 15.

Skeet III

This game selection uses a playing area as shown in Figure 1. It is a two-player game in which both players use guns to shoot at the target. The target moves from the foreground into the background from random sides. Each player is allowed one shot per flight. The first player to hit the target gets the score. The game ends when either player reaches a score of 15.

Skeet IV

This game selection uses a playing area as shown in Figure 1. It is a two-player game in which both players use guns to shoot at the target. The target moves from the foreground into the background from random sides. Each player alternately shoots at the target starting with the left player first. If the player whose turn it is to shoot, hits the target during the initial part of the flight, he retains his turn to shoot next, thereby preventing his opponent from playing in turn. This rewards fast accurate shooting. The first player to score 15 points wins, and the game ends.

Attack I

This game selection uses a playing area as shown in Figure 2. It is a single-player game in which the player tries to shoot the target on the screen with an external gun. The target moves from the background toward the foreground. The target can start and change course in flight at random. Only one shot is allowed per flight of the target. The game ends when either the hit count or the number of flights reaches 15.

Attack II

This game selection uses a playing area as shown in Figure 2. It is a two-player game in which one player tries to shoot the target and the other player controls the direction in which the target flies with the joystick. The target moves from the background into the foreground and the player with the gun is allowed one shot to be taken per flight. The game ends when either the hit count or the number of flights reaches 15.

Attack III

This game selection uses a playing area as shown in Figure 2. It is a two-player game in which both players use guns to shoot at the target. The target moves from the background into the foreground with random trajectories. Each player is allowed one shot per flight. The first player to hit the target gets the score. The game ends when the first player reaches a score of 15.

Attack IV

This game selection uses a playing area as shown in Figure 2. It is a two-player game in which both players use guns to shoot at the target. The target moves from the background into the foreground with random trajectories. Each player alternately shoots at the target starting with the left player first. If the player whose turn it is to shoot hits the target during the initial part of the flight, he retains his turn to shoot next, thereby preventing his opponent from playing in turn. This rewards fast accurate shooting. The first player to score 15 points wins, and the game ends.

Destruct I

This game selection uses a playing area as shown in Figure 3. It is a single-player game in which the player tries to shoot the targets as they are flashed on the screen with an external gun. The targets flash sequentially on the screen and disappear as each is hit. The game ends when either the hit count or the number of sequences reaches 15.

Destruct II

This game selection uses a playing area as shown in Figure 3. It is a single-player game in which the player tries to shoot the targets as they are flashed on the screen. The targets flash randomly on the screen and disappear as each is hit. The game ends when either the hit count or the number of sequences reaches 15.

Destruct III

This game selection uses a playing area as shown in Figure 3. It is a two-player game in which both players use guns to shoot at the target. The targets flash sequentially on the screen and the first player to hit the target scores. If both players hit the same target simultaneously, both players will get a score. The game ends when all targets disappear.

Destruct IV

This game selection uses a playing area as shown in Figure 3. It is a two-player game in which both players use guns to shoot at the target. The targets flash randomly on the screen and the first player to hit the target scores. If both players hit the same target simultaneously, both players will get a score. The game ends when all targets disappear.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_n pin ..... −0.3 to +12.0V
Storage temperature ..... −20°C to +70°C
Ambient operating temp. range ..... 0°C to 40°C

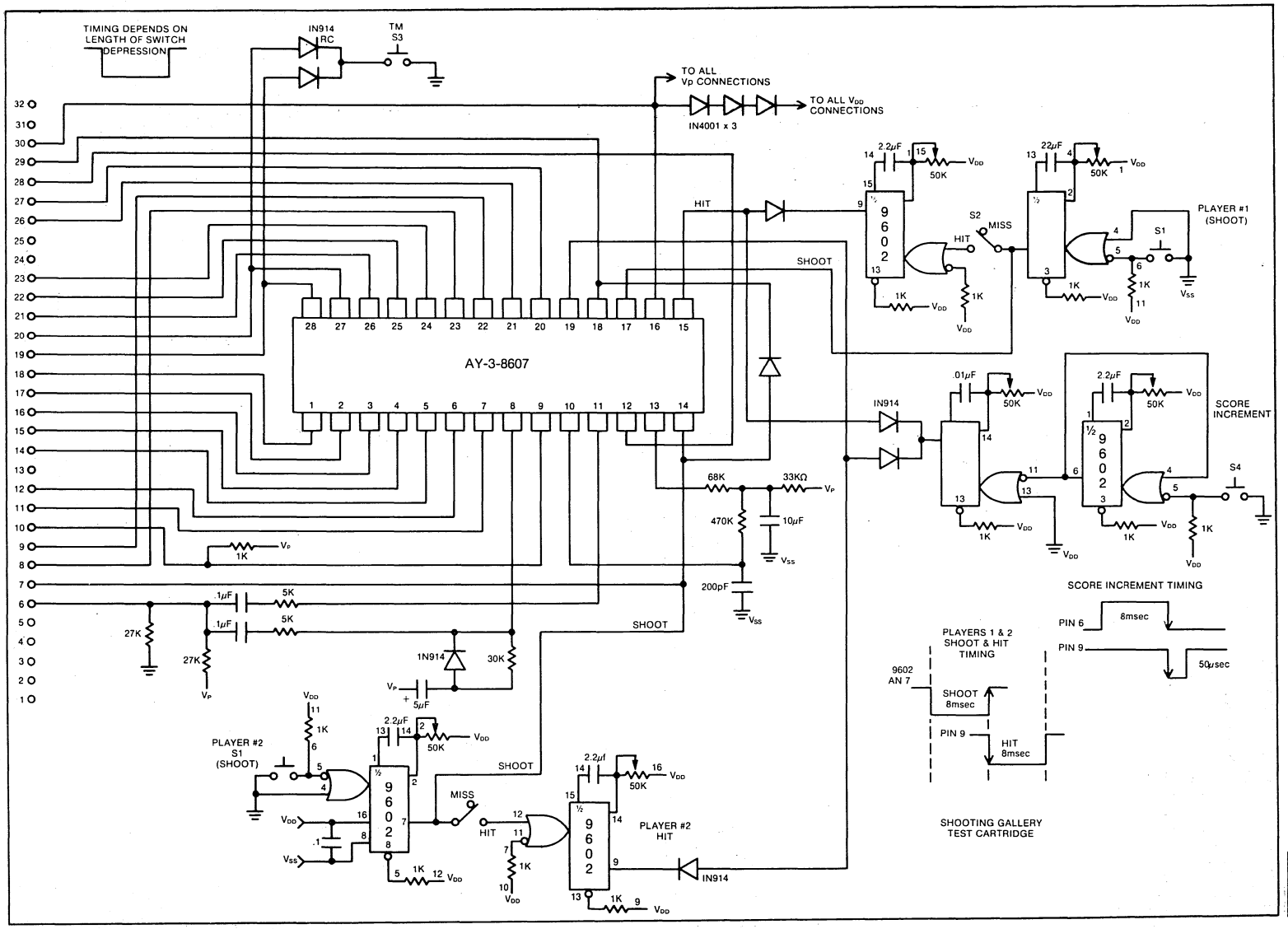
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

V_{dd} = 7.5 to 9.0 Volts
V_{ss} = 0 Volts
All characteristics specified at 25°C and V_{dd} = 7.5 volts

Characteristics	Min	Max	Units	Conditions
Clock Input	—	—	—	Crystal controlled @ 3.579545MHz with 45% to 55% positive duty cycle.
	0	0.5	Volts	Logic "0" level
	V_{dd}-2	V_{dd}	Volts	Logic "1" level
	—	100	μA	Leakage, $V_{in} = V_{dd}$
Outputs				
Pins 2, 3, 4, 5, 6, 7	—	1.0	Volts	Logic "0" level $I_{out} = -2mA$
	—	100μA	μA	Off volt = V_{dd} = 7.5 Volts
Output Pin #8	—	1.0	Volts	$I_{out} = -0.5mA$
	V_{dd}-2	—	Volts	$I_{out} = +0.5mA$
Output Pins 11, 13	—	1.0	Volts	$I_{out} = -0.2mA$
	V_{dd}-2	—	Volts	$I_{out} = +0.2mA$
Output Pin #22, 23	—	1.0	Volts	$I_{out} = -0.5mA$
	—	35	μA	Volt = V_{dd} = 7.5 Volts
Inputs				
Pin #26, 27, 28	150	375	K	V_{dd} = 7.5 Volts
Pin #12, 14, 17, 18, 20	75	150	K	V_{dd} = 7.5 Volts
Power supply current I_{dd}	—	65	mA	V_{dd} = 7.5 Volts

CONSUMER


TIMING DEPENDS ON LENGTH OF SWITCH DEPRESSION
IN914
RC
TM
S3
TO ALL Vp CONNECTIONS
TO ALL VDD CONNECTIONS
IN4001 x 3
HIT
SHOOT
AY-3-8607
PLAYER #1 (SHOOT)
S2
MISS
S1
SCORE INCREMENT
S4
SCORE INCREMENT TIMING
PIN 6
8msec
PIN 9
50μsec
PLAYERS 1 & 2 SHOOT & HIT TIMING
9602 AN 7
SHOOT 8msec
HIT 8msec
SHOOTING GALLERY TEST CARTRIDGE
PLAYER #2 S1 (SHOOT)
PLAYER #2 HIT
68K
33KΩ
470K
10μF
200pF
1N914
30K
27K
5K
1μF
2.2μF
.01μF
50K
1K
5μF

CONSUMER

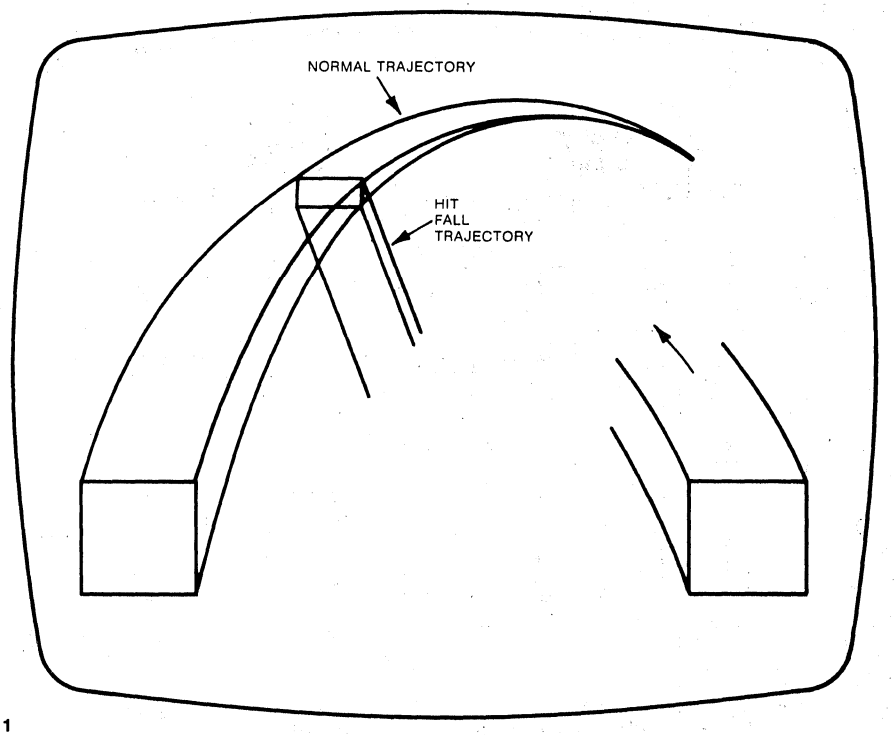


Fig. 1

NOTE: Target can start from either right or left foreground depending on random game control or 2nd player joystick control when applicable.

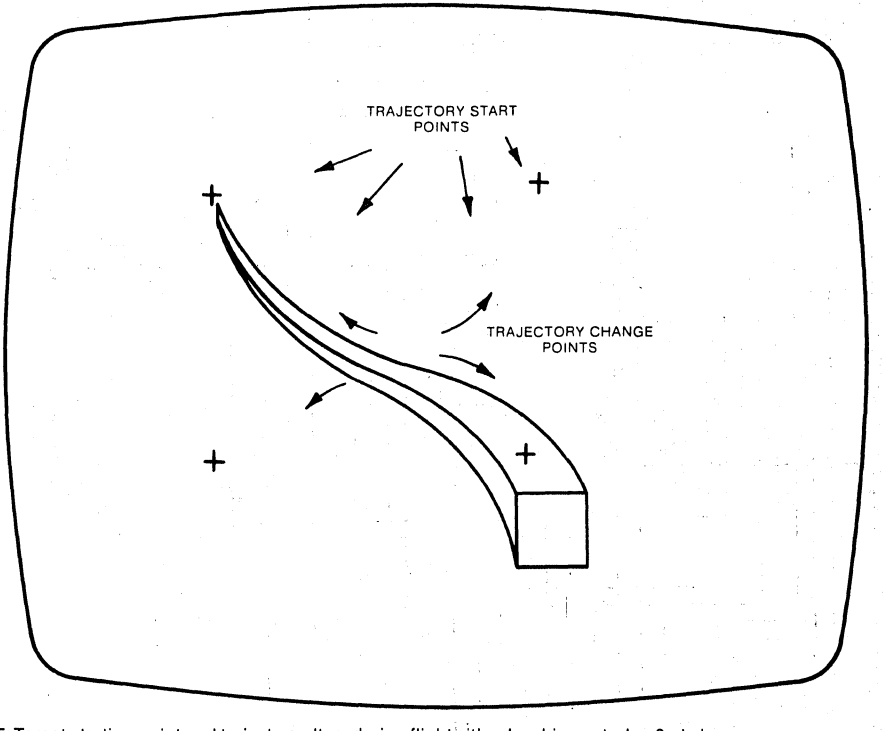


Fig. 2

NOTE: Target starting point and trajectory alters during flight either by chip control or 2nd player joystick control when applicable.

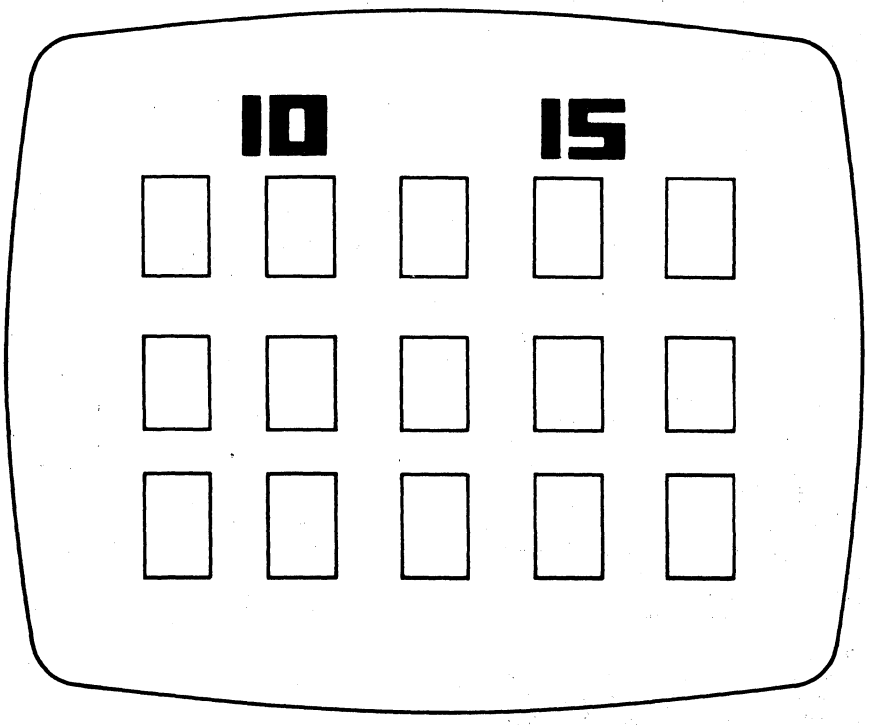


Fig. 3

NOTE: 1.Only one box is visible at any time.
2.Sequential target order starts from the left side to the right side of the screen starting from top to bottom.

Supersport

FEATURES

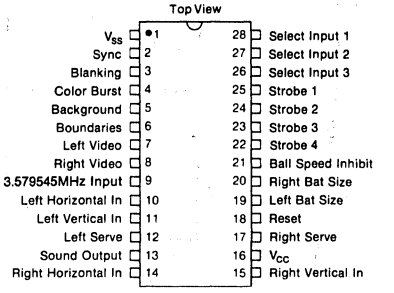
- Full **COLOR** Operation with AY-3-8615
- Ten selectable games — tennis, hockey, soccer, squash, practice, gridball, basketball, basketball practice, one and two player target
- 625 Line (AY-3-8610) and 525 Line (AY-3-8610-1) versions
- T.V. raster generator
- Two axis player motion
- Automatic on-screen scoring, 0-15
- Automatic ball speed-up after 7 hits or may be disabled by ball speed inhibit input
- Realistic ball service and scoring
- Score color keyed to player
- Independent player selectable bat size for handicapping
- Fast ball speed inhibit
- Five segment bats giving high, low, and horizontal ball angles
- Sound outputs for hit, rebound and score
- Shooting forwards in hockey and soccer

DESCRIPTION

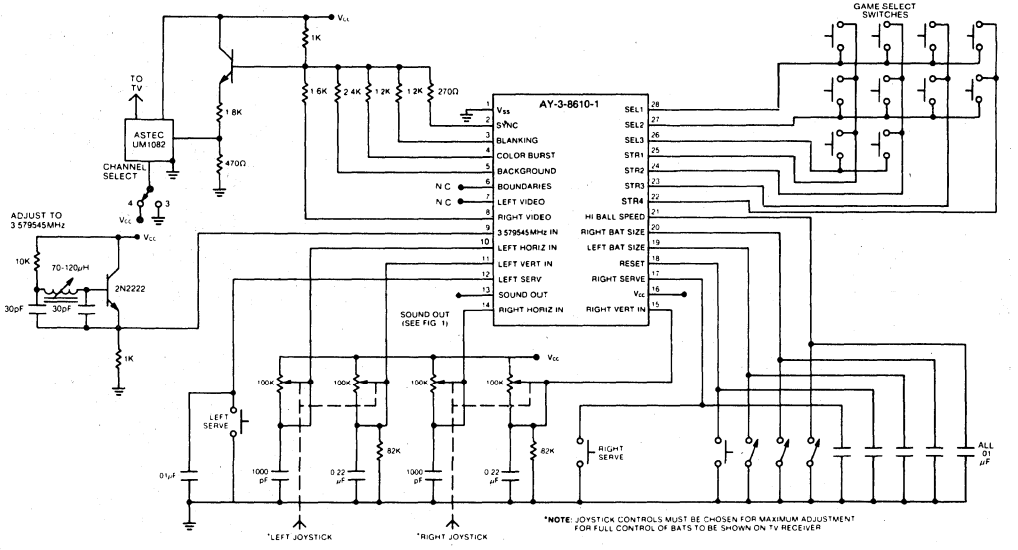
The AY-3-8610 and AY-3-8610-1 circuits have been designed to provide a TV 'game' function which gives active entertainment using a standard color or black and white domestic television receiver.

The circuit is intended to be battery powered and a minimum number of external components are required to complete the system.

PIN CONFIGURATION
28 LEAD DUAL IN LINE

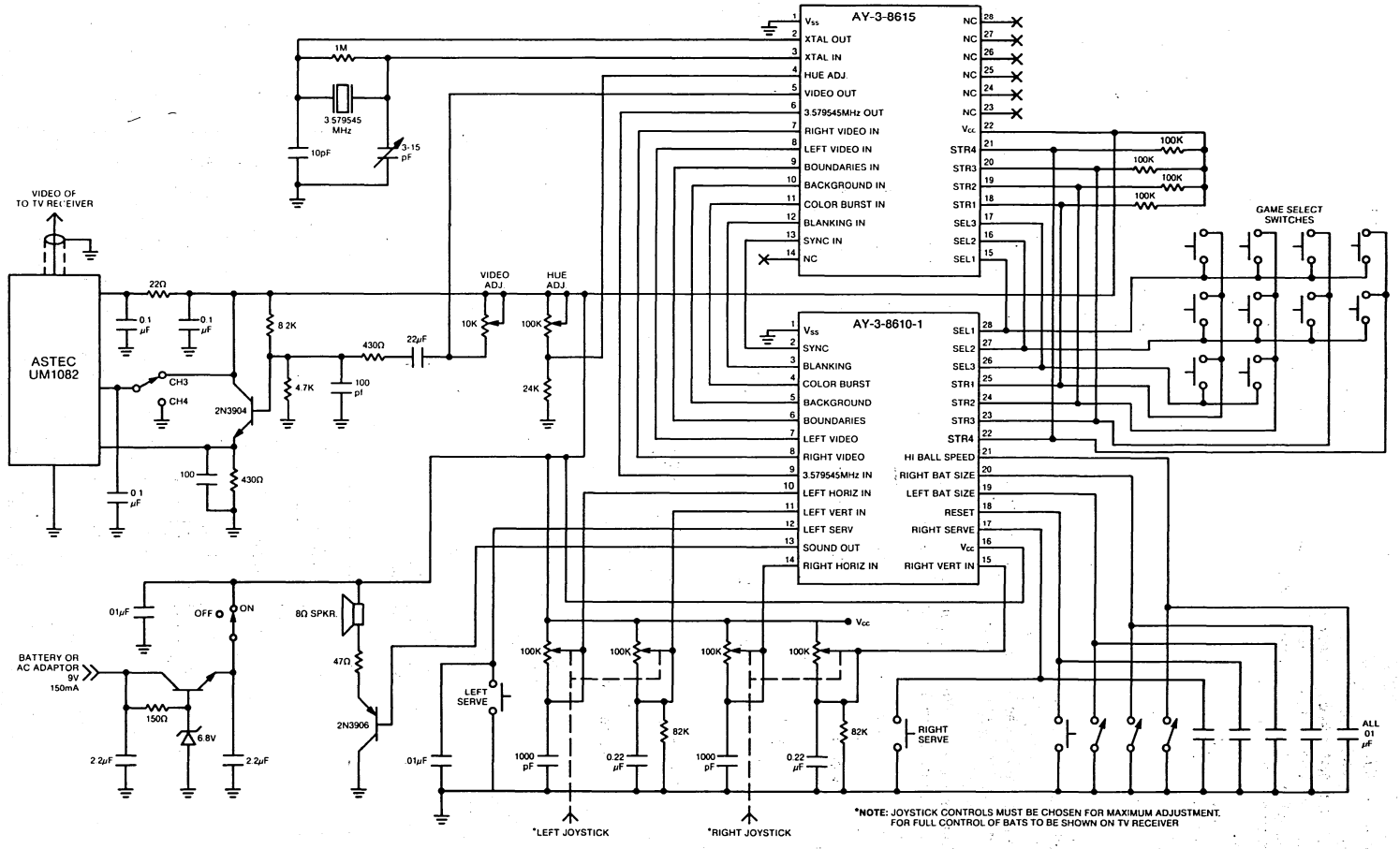


SYSTEM DIAGRAM 1: BLACK AND WHITE IMPLEMENTATION



CONSUMER

SYSTEM DIAGRAM 2: AY-3-8610-1 FULL COLOR IMPLEMENTATION USING AY-3-8615 COLOR CONVERTER CIRCUIT



PIN FUNCTIONS

Power

V_{CC} positive supply input
V_{SS} negative (substrate) supply input

Clock Input — 3.579MHz — color burst to N.T.S.C.

For black and white operation, a simple LC oscillator can be used for the clock, but for color, the clock must be derived from a color crystal as shown in System Diagram 2.

Color Inputs

Right player vertical control
Right player horizontal control
Left player vertical control
Left player horizontal control
Right player serve
Left player serve
Right player bat size
Left player bat size
High speed ball inhibit
Game reset

The game is reset with scores set to zero and ball returned to the service position by momentarily connecting the reset input to V_{SS}.

Bat size can be selected as either small or large individually for handicapping purposes. Connection of the bat size input to V_{SS} selects small bat.

Bat position is set by a variable resistor and capacitor connected as shown in the System Diagram.

Fast ball speed may be inhibited by connecting V_{SS} to the High Speed Ball Inhibit input.

Game Select Inputs/Outputs

Strobe 1	Select Input 1
Strobe 2	Select Input 2
Strobe 3	Select Input 3
Strobe 4	

Game selection is made by the interconnection of one of the output strobes, STR 1, STR 2, STR 3, or STR 4, with one of the three input selection lines SEL 1, SEL 2, or SEL 3.

The game selections are defined as:

STR 1/SEL 1	Tennis
STR 1/SEL 2	Hockey
STR 1/SEL 3	Squash
STR 2/SEL 1	Practice
STR 2/SEL 2	Soccer
STR 2/SEL 3	Basketball
STR 3/SEL 1	Basketball Practice
STR 3/SEL 2	Gridball
STR 4/SEL 1	Single Player Target
STR 4/SEL 2	Two Player Target

Video Outputs

Right bat, score and ball
Left bat, score and ball
Boundaries
Background
Sync
Blanking
Color burst locator

All signals are present in the circuit to generate a composite video signal with composite blanking and sync. The combined video signal provides the input to the game RF modulator.

In addition to the above outputs, a color burst locator output is provided for use where external color generation is desired. The signal locates the position in the waveform behind the sync pulse.

In all games, the ball starts at slow speed. If the high speed mode has been selected the ball will switch to high speed after 7 consecutive hits by the players without a goal being scored.

The bats will be segmented into 5 zones, each zone defining a different rebound angle. The zones listed from top of bat to bottom are nominally high angle up, low angle up, horizontal, low angle down, high angle down. A ball passing through a forward from behind will have its angle influenced as above, but not its left/right direction.

All two player games will terminate when one player has 15 points at which time the bats have no further effect on the ball. The ball cannot be restarted until a game reset is applied.

Sound Output

Tone of approximately 500Hz, 1kHz and 2kHz will be output for a nominal period of 24 msecs for ball hits wall, ball hits bat and score. The output is capable of directly driving 100 ohm speakers.

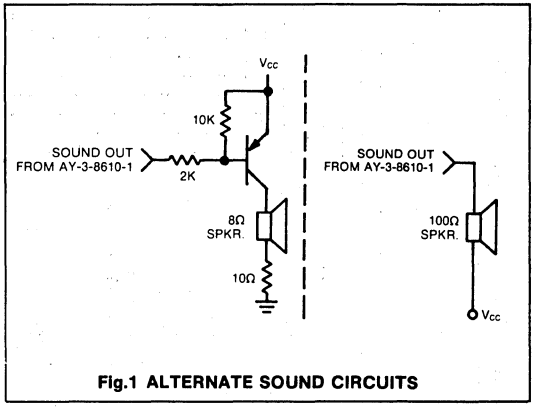


Fig.1 ALTERNATE SOUND CIRCUITS

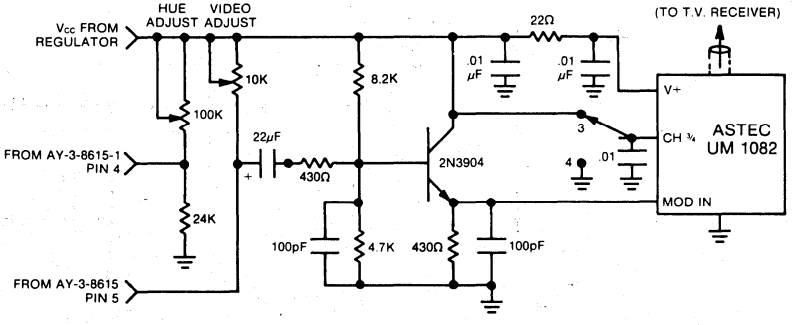


Fig.2 MODULATOR INTERFACE CIRCUIT

CONSUMER

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... −0.2 to +12V
Storage Temperature Range ..... −20°C to +70°C
Ambient Operating Temperature Range..... 0°C to +40°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +7.5 to +9.0V
V_{SS} = 0V

Characteristics**	Min	Typ	Max	Units	Conditions
Clock Input					
Frequency	—	3.579545	—	MHz	
Logic '0'	0	—	0.5	Volts	50% duty cycle ±5%
Logic '1'	V_{CC} −2	—	V_{CC}	Volts	
Leakage	—	—	100	μA	
Control Inputs 12, 17, 18, 19, 20, 21, 26, 27, 28					Max. contact resistance of 1K to V_{SS}
Logic '0'	0	—	0.5	Volts	
Logic '1'	V_{CC}−2	—	V_{CC}	Volts	
Input Impedance	—	100	—	kΩ	Pull up to V_{CC}
Outputs Pins 2-8, & 13					
On	—	—	1.0	Volts	I_{out} = 2mA
Off	—	—	100	μA	V_{out} = V_{CC} (open drain)
Outputs Pins 22-25					
On	—	—	1.0	Volts	I_{out} = 0.5mA
Off	—	—	100	μA	V_{out} = V_{CC} (open drain)
Power supply current	—	—	60	mA	At V_{CC} = +7.0V

**At 25°C & V_{CC} = 6V

CONSUMER

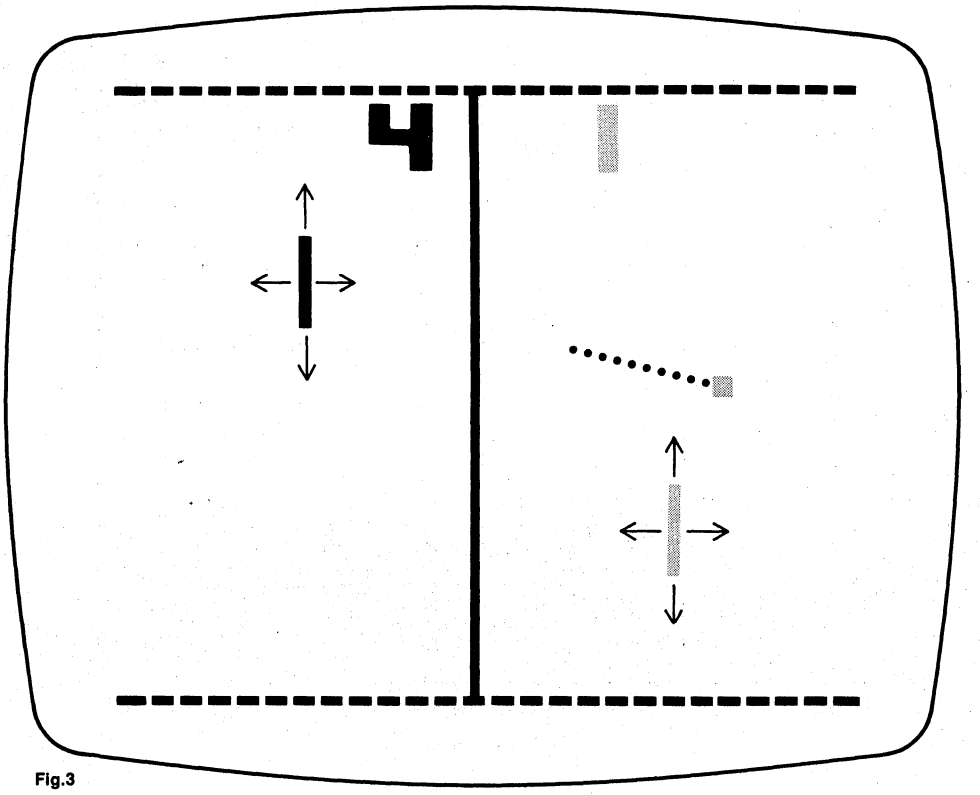


Fig.3

Tennis

This game uses a playing area as shown in Fig. 3. Each player can only move around his side of the court. The game will start when the player whose turn it is to serve, depresses his service button. The service will automatically change every five points scored. At service the ball will move away from the service point with a random angle but always toward the net.

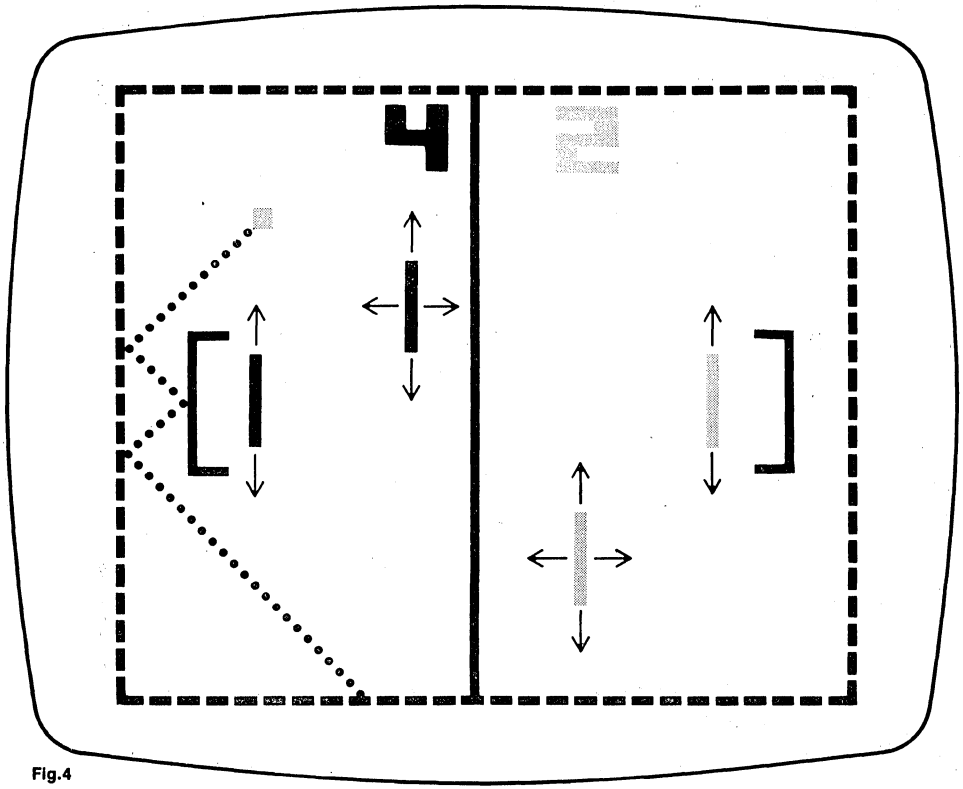


Fig.4

Hockey

This game uses a playing area as shown in Fig. 4. The forwards on both sides have freedom to move over the entire playing area. The goal keepers will be locked in the horizontal axis in front of their respective goals but will move in the vertical axis in the same manner as the forwards.

The game starts when both players have depressed their service buttons. The ball will move away from the face off point with a randomly selected angle in either direction.

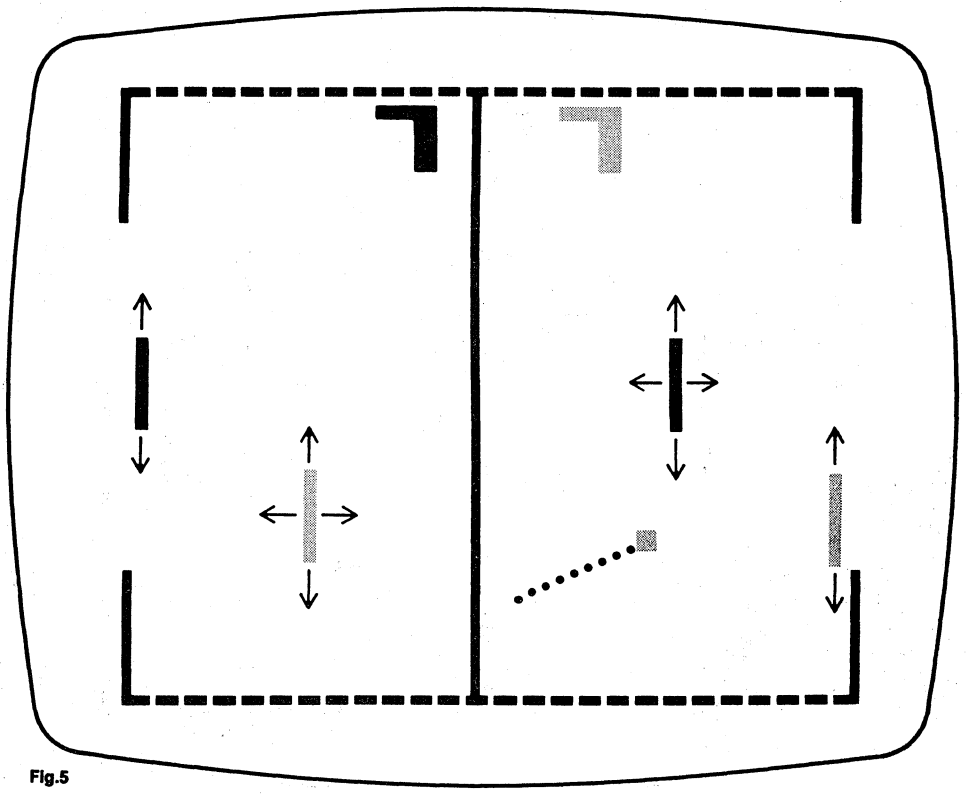


Fig.5

Soccer

This game uses a playing area as shown in Fig. 5. The motion of the players is as in the hockey game. The game will start when the loser of the previous goal depresses his service button. The ball will move away from the kickoff point with a randomly selected angle but always towards the goal of the winner of the previous goal.

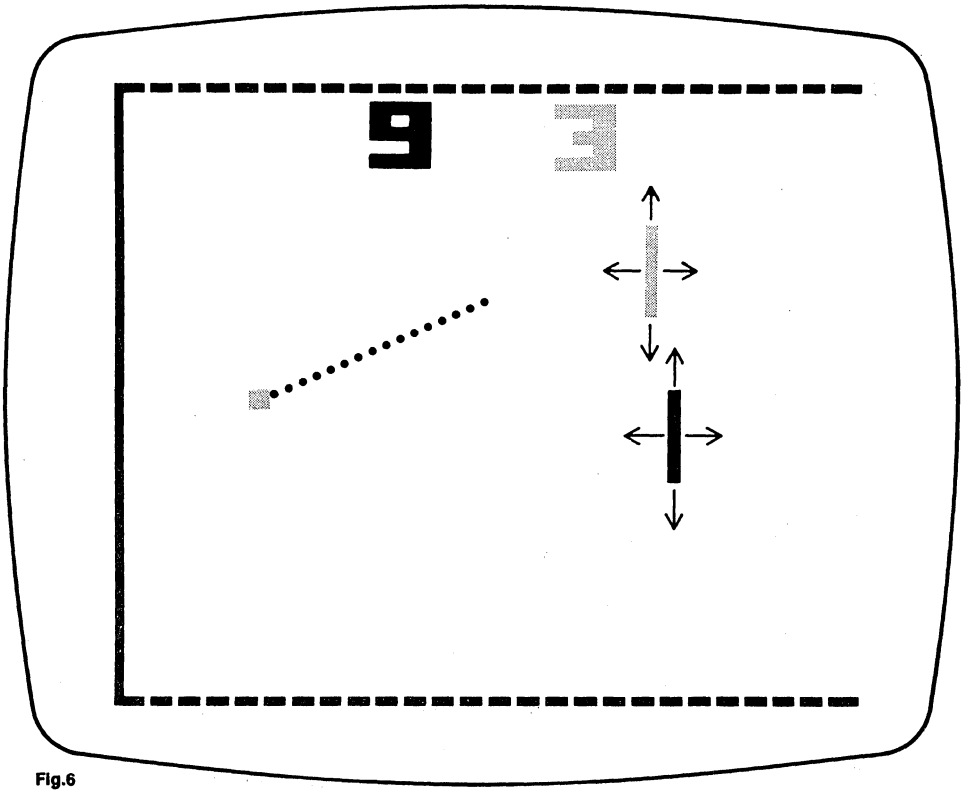


Fig.6

Squash

This game uses a playing area as shown in Fig. 6. Each player can move over the whole court. The game will start when the player whose service it is, depresses his service button. The ball moves off with a random angle toward the front wall. The color of the ball will change to the color code of the next player to hit the ball. Should the wrong player intercept or be hit by the ball it will be considered a fault. Points will only be given if won on player's own service. Points won on opponents serve will only cause a service change.

Practice

This game is a single player squash (See Fig. 7). The right score counts the number of successive hits in the current game (to a maximum of 15), the left score the number of volleys played.

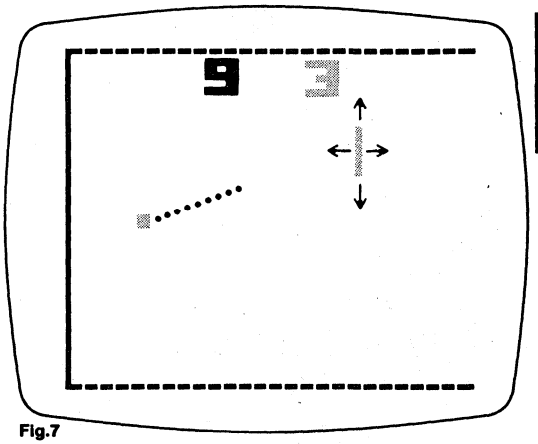


Fig.7

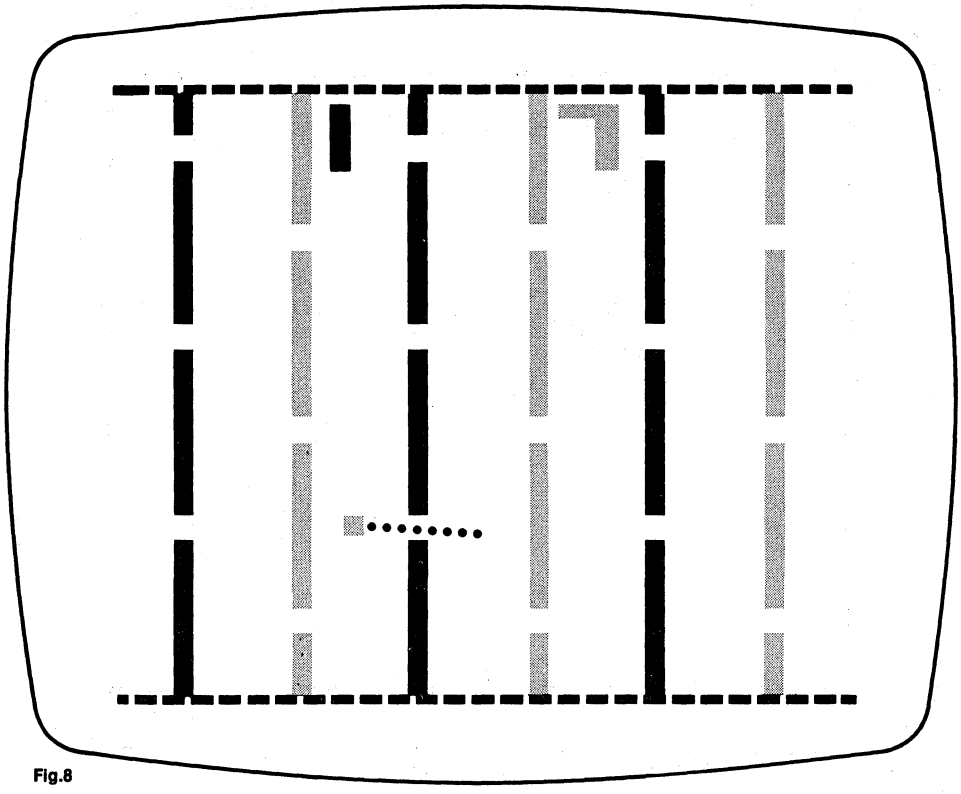


Fig.8

Gridball

This game uses a playing area as shown in Fig. 8. Each player has three sets of vertically moving barriers to block the ball from approaching his end and opening in the barriers to permit the ball to advance toward the opponent's end. The game starts when both players have depressed their service buttons. The ball moves away from the face off point with a random angle in either direction.

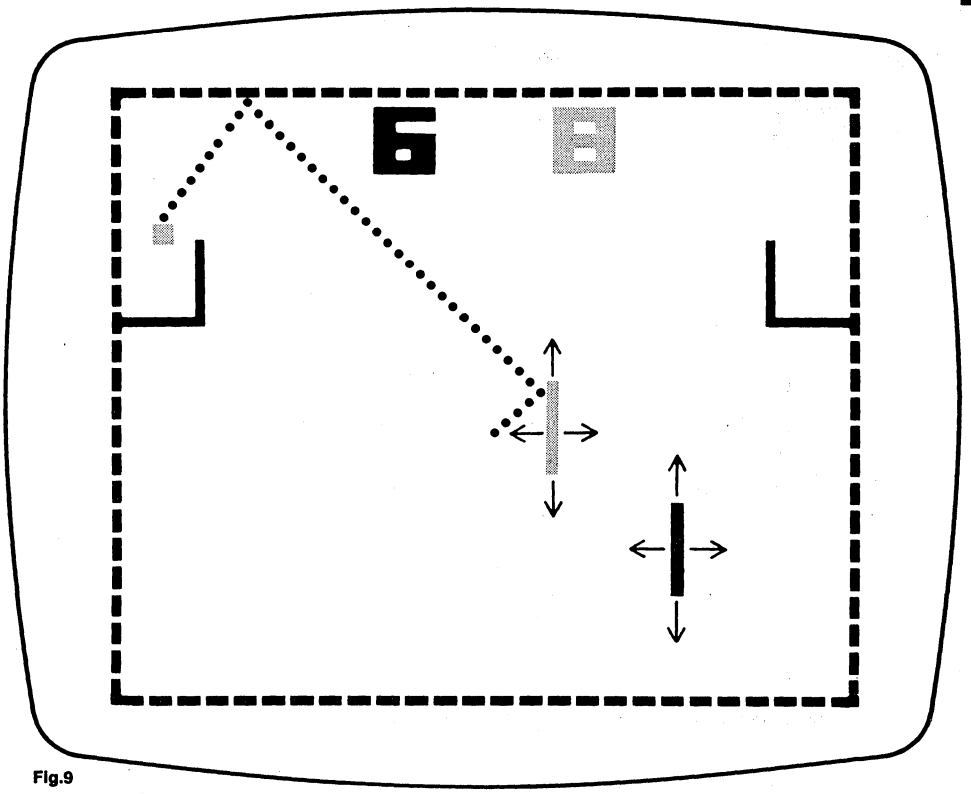


Fig.9

Basketball

The basketball games use the closed playing area as shown in Fig. 9. The players must deflect the ball and cause it to either the top of the goal to score. The game starts when both players depress the service buttons. The ball moves from the serve point with a random angle in either direction.

Basketball Practice

Basketball practice is a one player game which utilizes only the left basket as shown in Fig. 10. The right counter displays the number of hits the player makes without scoring while the left counter shows the number of baskets made. Play starts when the right serve button is depressed.

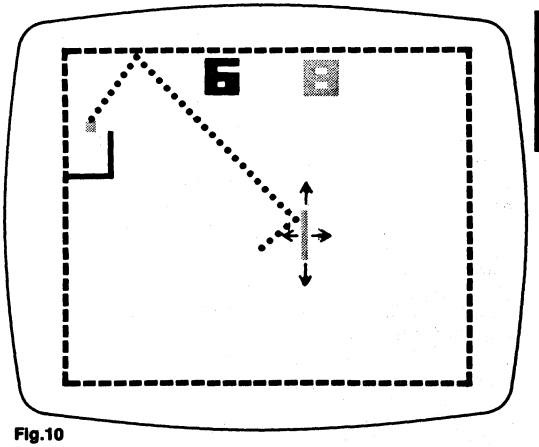


Fig.10

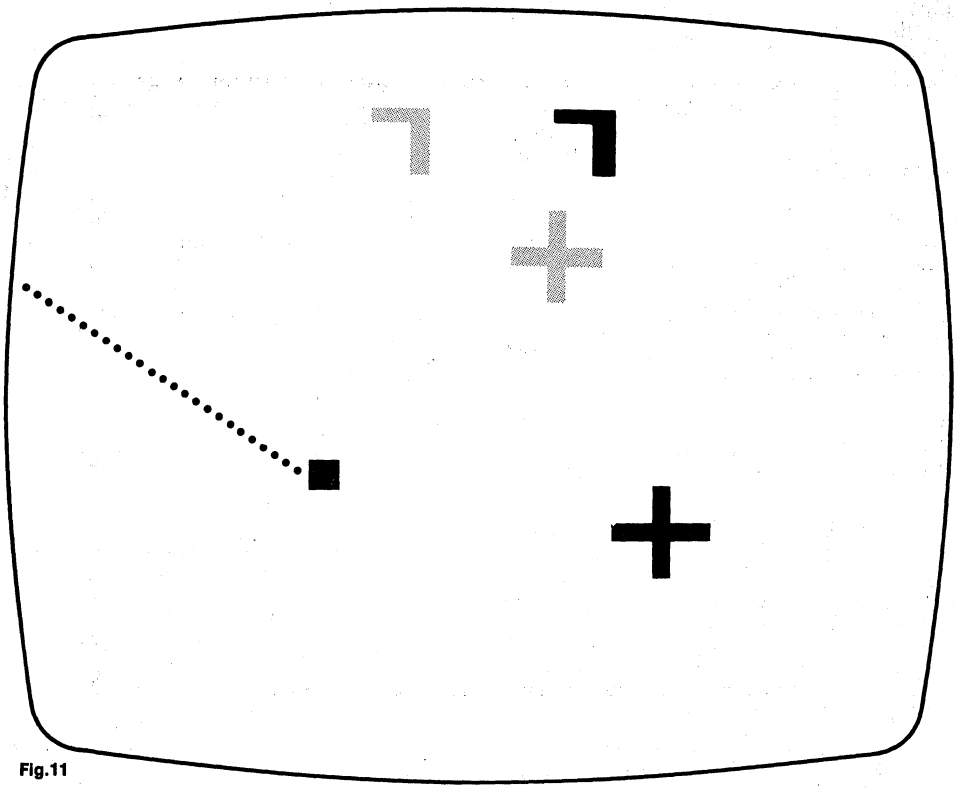


Fig.11

Two Player Target

The two player target game follows the same rules as the single player game except that both players control their own cursors and shot buttons. The left score displayed is for the left player and the right score displayed is for the right player. The target can only be shot at once on each traverse by either player but only recognizes the first hit. The first player to reach a score of 15 wins the game.

Single Player Target

The single player target game is a game in which the player moves a cursor displayed on the T.V. screen over a moving target and depresses the serve button for shots to be taken. The player has only one "shot" for each traversal of the screen by the target. Additional "shots" are ignored after the first shot on each traverse. The right score indicates the number of hits made and the left score indicates the misses. A count is made on either score on each traverse of the target across the screen. The target disappears when hit and the game ends when either of the scores displayed reaches 15.

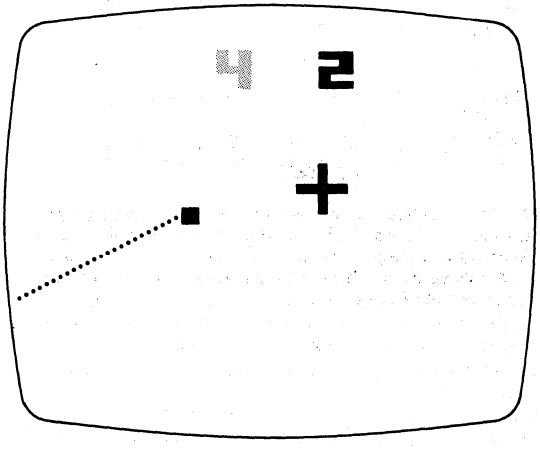


Fig.12

Color Processor

DESCRIPTION

The AY-3-8615 is a single N-Channel MOS circuit which processes video signals from any of the Gimini "8600" Game Series circuitry. It converts these video signals into a single color composite video output. The colors of the background and objects are selectively changed directly by the game select matrix. The circuit also provides, as an output, a buffered 3.579545MHz clock for the game chip.

OPERATION

The AY-3-8615 provides a color composite video signal with color burst envelope and sync for input to the RF modulator of a TV game.

Sync: The sync input from any of the "8600" games is OR'ed with the video output of the color circuit. The sync amplitude level is compensated to ensure correct operation in color TV circuits.

Color Burst: A color burst signal, containing ten cycles of the 3.579MHz color reference is supplied after sync. The color phase of the burst is internally shifted by the game matrix inputs with respect to the phases of the background, right player and left player so that different colors may be rendered for each game. This color change may be affected with no external components.

Video Inputs: Seven video inputs are provided on the AY-3-8615. These are: field, background, color burst locator, left player, right player, blanking, and sync.

Video Output Mixer: With OR'ed sync, color burst and blanking, the video consists of background, field scores, right player, left player, and objects on a single output pin.

Grounded Select Input	Back-ground	Field	Right Player	Left Player
1. Sel1/Str1, Sel2/Str2, Sel2/Str4	Green	Yellow	Magenta	Blue
2. Sel2/Str1 Sel2/Str3	Blue	Cyan Blue	Dk. Blue	Red
3. Sel3/Str1, Sel3/Str2	Magenta	Lt. Red	Blue	Yellow
4. Sel1/Str2, Sel1/Str3, Sel1/Str4	Cyan Green	Green	Brown	Blue

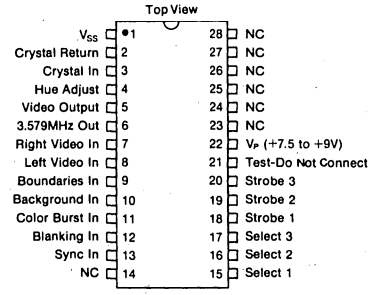
Colors may be adjusted for system variations by the chip hue control which varies the phase delay of the color outputs.

Luminescence Levels: The luminescence levels of the various signals in the composite video output have been selected to provide black and white compatibility. The field and left player signals are set to near white levels, the right to near black, and the background is set at a mid level to show gray.

Figure 1 shows the typical composite video waveform from the circuit.

In order to assure the correct video levels, a 2K variable potentiometer should be used to adjust the output to the min/max values specified for the modulator used.

PIN CONFIGURATION
28 LEAD DUAL IN LINE



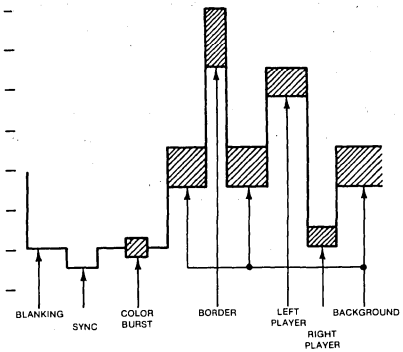


Fig. 1 COMPOSITE VIDEO OUTPUT

CLOCK INPUT

The AY-3-8615 is operated directly from a 3.579545MHz crystal input. A variable capacitor with a range of 3 to 15 pF should be used to tune the crystal.

CLOCK OUTPUT

The AY-3-8615 generates low impedance 3.579545MHz clock to directly drive the "8600" series game chips without external components.

Characteristics at +25°C	Min	Typ	Max	Units
Clock Input (Crystal)	—	3.579545	—	MHz
Video & Game Select				
Logic "0" (Select)	—	—	0.2	Volts
Logic "0" (Video)	—	—	1.0	Volts
Logic "1" (all)	V_P–2	—	—	Volts
Hue Adjust (External)	2.0	—	V_P	Volts
Video Output (2 K pot to V_P)	—	1K	—	Ω
Clock Output Rise & Fall Time	—	100	—	ns
Supply Current	—	—	25	mA

CONSUMER

Motor Cycle

FEATURES

- Full color operation with AY-3-8615 color processor
- 4 game selections—Time Out, Obstacle Race, Moto Jump and Rally Run
- 2 skill selections—PRO/AM
- 625 line (CCIR) and 525 line (NTSC) pin selectable
- Internal TV (raster) generator
- Automatic on-screen scoring
- Realistic sound effects

DESCRIPTION

Motor Cycle is a game for one player who controls the speed of a motorbike and rider. At the start of each game the motorbike and rider are stationary at the upper left-hand side of the TV screen. As the player moves the joystick, the motorbike and rider move across the screen on track 1. The motorbike sound starts with the bike movement and as the bike and rider accelerate, the motorbike sound reflects these speed changes. The motorbike wheels have an appearance of rotating at a speed also related to the throttle setting.

At the end of track 1 the bike and rider reappear on track 2 at the left-hand side, and likewise at the end of track 2 the bike appears on track 3 at the left-hand side of the screen. The movement of the bike and rider on track 3 to the right edge of the screen will cause a reinitialization of the bike and rider at the left of the screen on track 1. There will be no movement until the throttle is reset to a slow speed and then increased. Figure 1 shows the playing field for each game.

GAME OPERATIONS

Time Out

The object of this game is to reach the end of track 3 in the shortest time. The three-digit score is automatically reset as the rider first begins to move on track 1 and the score is incremented until the game is over. The score appears centered on the screen above track 1, and the score remains until the start of the next game.

Time Out requires a speed shifting to achieve the lowest time scores. As the throttle speed is increased and the rider begins to move, the bike object is in speed one and moves at a set rate across the screen. The only way to accelerate the bike object motion is to return the throttle to a "slow" position and then turn to a "fast" position. This shifting procedure will move the bike into speed 2 and the object will go across the screen at a faster rate. Another "shift" will allow speed 3.

A PRO/AM option switch is provided to select a difficulty factor. In the hard mode, a crash occurs if the player tries to increase the throttle speed too rapidly. A crash will flip the bike and rider upside down and the sound will be a high-pitch screech. At the end of the crash the bike and rider are reinitialized on track 1 and the score reset. In the easy mode no crash is allowed.

Obstacle Race

As the throttle speed is increased, the bike and rider move across track 1 at a rate determined by the throttle controller setting. Obstacle Race has no speed shifting. Located on each of the three tracks are obstacles. The easy/hard option switch selects the number of obstacles per track. The easy mode has one obstacle per track and the hard mode has two obstacles per track.

The object of this game is to traverse the three tracks in the shortest time, doing a wheelie over each obstacle. The score counters record the run time in the same manner as the Time Out Game.

In Obstacle Race the crash is not caused by accelerating too rapidly. The crash is caused by not doing a wheelie over an obstacle. In the wheelie position, the bike will have the front wheel lifted off the track. A crash into an obstacle will flip the bike upside down and produce the screech sound. The score is reset at the end of the crash.

Moto Jump

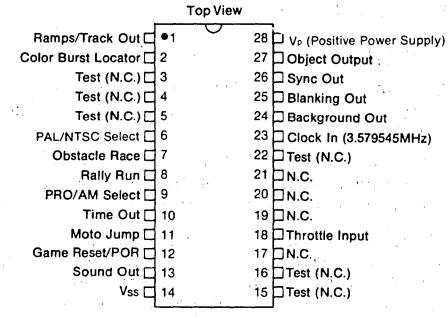
The object of this game is to control the throttle speed to properly jump the ramp and buses located on track 3. The game begins with 8 buses and with each successful jump over the ramp and buses an additional bus appears. The game is over when the maximum number of errors has been reached, which is 3 or 7 errors, depending on the position of the PRO/AM switch. The game is then started by reselecting the Moto Jump game input.

Errors are caused by accelerating too rapidly, insufficient speed to clear the buses, or landing too far past the back ramp after the jump. The bike and rider flip upside down and a screeching sound indicates an error. The score records the number of errors in the first digit and the number of displayed buses in the next two digits.

Rally Run

This game is similar to Moto Jump with the addition of obstacles on track 1 and track 2. The object of Rally Run is to do a wheelie over each obstacle and then adjust the throttle for the correct speed to jump the buses on track 3. The PRO/AM option switch selects two obstacles per track and allows three errors per game in the hard mode, and one obstacle per track and seven errors per game in the easy mode. Errors are caused by accelerating too rapidly, not in wheelie position over the obstacles, insufficient speed to clear the buses, or landing too far past the back ramp after the jump. The score records the number of errors and the number of buses displayed the same as in the game of Moto Jump.

PIN CONFIGURATION
28 LEAD DUAL IN LINE



CONSUMER

PIN FUNCTIONS

Pin No.	Name	Function
1	Ramps and Tracks	The output of this pin is the video signal of ramps and tracks
2	Color Burst Locator	The output of this pin is the color time slot which occurs after the sync signal during horizontal blanking.
3	Test	Not Connected
4	Test	Not Connected
5	Test	Not Connected
6	PAL/NTSC	This input is provided with an internal resistor pull-up to V_P. If this input is tied to V_{SS} NTSC (262 vertical lines) is selected. If this input is tied to V_P or allowed to float, PAL (312 vertical lines) is selected.
7	Obstacle Race	This pin is provided with an internal resistor pull-up to V_P. If this input is momentarily connected to V_{SS}, this game will be selected. Otherwise, this pin is normally open.
8	Rally Run	This pin is provided with an internal resistor pull-up to V_P. If this input is momentarily connected to V_{SS}, this game will be selected. Otherwise, this pin is normally open.
9	PRO/AM Option	This pin is provided with an internal resistor pull-up to V_P. If this input is switched to V_{SS}, the PRO (hard) mode is selected. Switching this pin to V_P or allowing it to float selects the AM (easy) mode.
10	Time Out	This pin is provided with an internal resistor pull-up to V_P. If this input is momentarily connected to V_{SS}, this game is selected. This pin is normally open.
11	Moto Jump	This pin is provided with an internal resistor pull-up to V_P. If this input is momentarily connected to V_{SS}, this game is selected. This pin is normally open.
12	Game Reset and POR	The input to this pin is provided by an external RC network, which generates a reset signal. This network consists of a 100KΩ resistor from this pin to V_P and a 0.1 μF capacitor from this pin to V_{SS}.
13	Sound	The output of this pin is the sound for the bike engine, bus hit, crash, screech and a good jump. This output is designed to drive a PNP transistor, which in turn drives the game speaker.
14	V_{SS}	This input is the negative power supply.
15	Test	Not Connected
16	Test	Not Connected
17	N.C.	Not Connected
18	Throttle	The input to this pin is an oscillator signal for controlling the motion of the bike and rider.
19	N.C.	Not Connected
20	N.C.	Not Connected
21	N.C.	Not Connected
22	Test	Not Connected
23	Clock In	The input to this pin is the 3.58MHz oscillator.
24	Background	This output provides the background video signal.
25	Blanking	This output provides the horizontal composite blanking between each line of video information.
26	Sync	This pin provides the combined output of horizontal sync or vertical flybacks.
27	Object Output	The output of this pin is the video output signal for the bike, buses, score and obstacles.
28	V_P	This input is the positive power supply.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

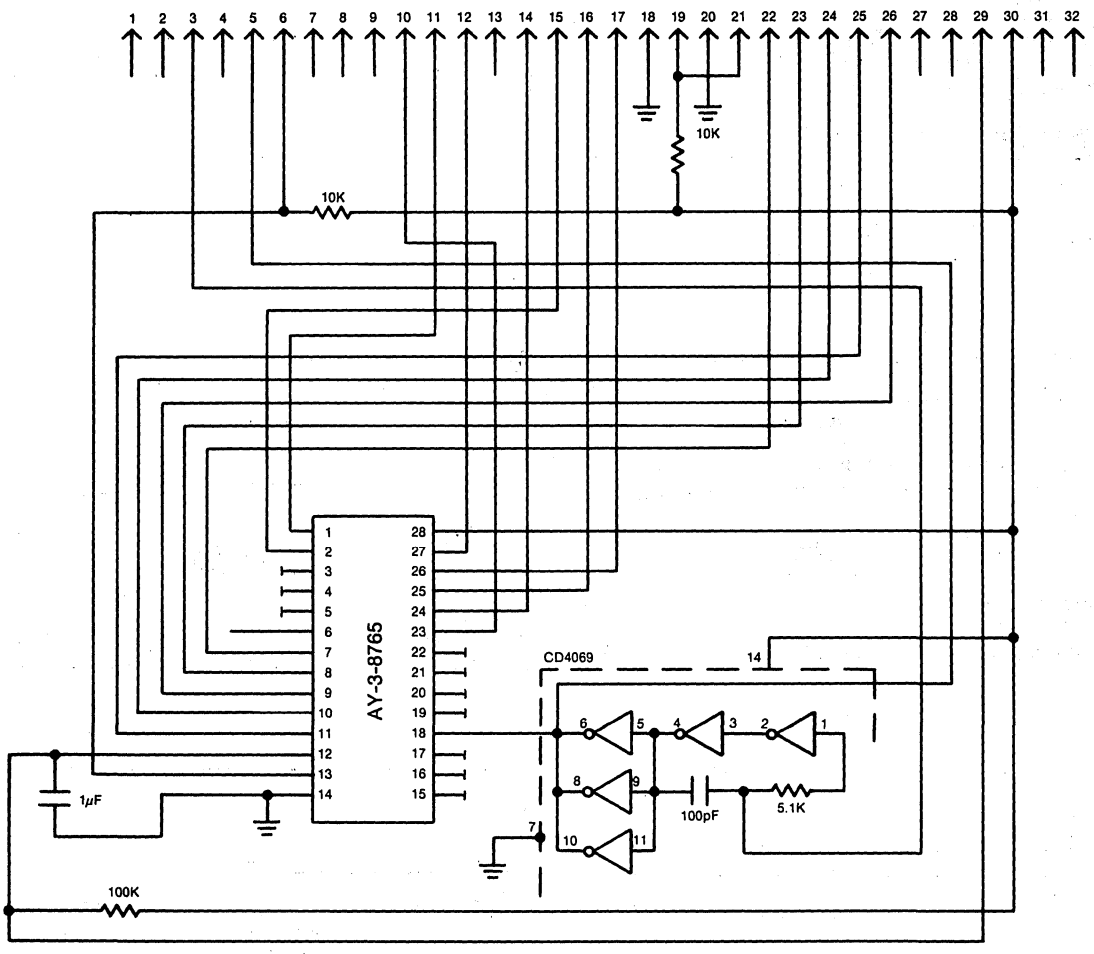
Voltage on any pin with respect to Vss ..... -0.3 to +12 Volts
Storage temperature range ..... -20° to +70°C
Ambient operating temperature range ..... 0°C to +40°C
Operating voltage supply range ..... +7.5 to +9 Volts

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)
Parameter values at $T_a = 25°C$

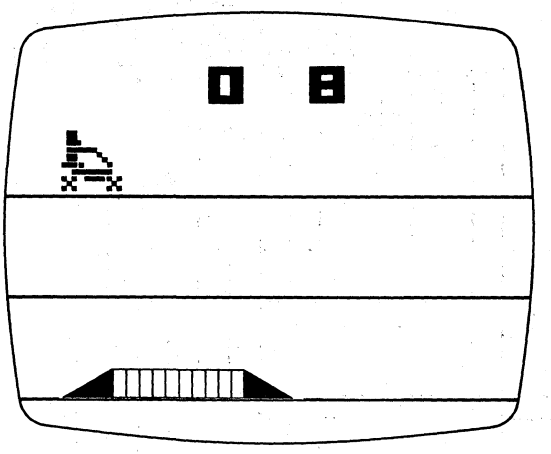
Characteristics	Min	Max	Units	Conditions
Clock In (Pin 23)				
Frequency	—	—	MHz	Nominal 3.579545
Input low voltage	Vss −0.3	Vss +0.3	V	
Input high voltage	Vss +6.5	V_p	V	
Duty Cycle	35	65	%	Clock swing from 0 to V_p
Throttle (Pin 18)				
Frequency	50	250	kHz	
Pulse width—positive	1.5	—	μs	
Input low voltage	Vss −0.3	Vss +0.2	V	
Input high voltage	Vss +6.5	V_p	V	
Inputs (Pins 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 16, 22)				
Input high voltage	Vss +6.5	V_p	V	
Input low voltage	Vss −0.3	Vss +0.2	V	
Sound Output (Pin 13)				
Voltage output low vol.	—	Vss +0.5	V	Force 0.75mA at $V_p = 7.5V$
FTC Out (Pin 19)				
Voltage output low (V_{ol})	—	Vss +0.5	V	Force 0.5mA at $V_p = 7.5V$
Other Outputs (Pins 1, 2, 24, 25, 26, 27)	—	Vss +0.5	V	Force 1.0mA at $V_p = 7.5V$
Voltage output low (V_{ol})	—	—	—	
Power Supply Current	—	75	mA	At $V_p = 7.5V$

CONSUMER

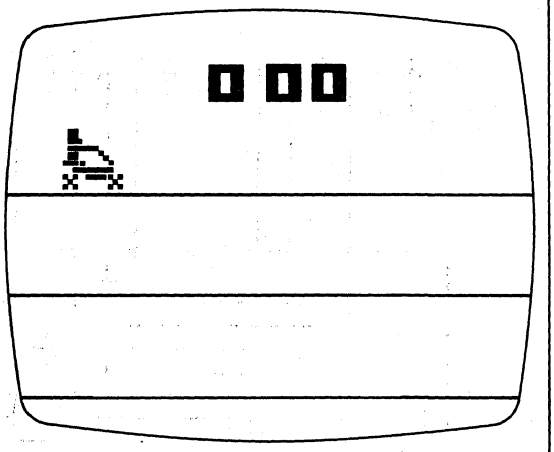


*NOTE:
PIN 6 OPEN FOR CCIR OPERATION
PIN 6 TIE TO V_{SS} FOR NTSC OPERATION

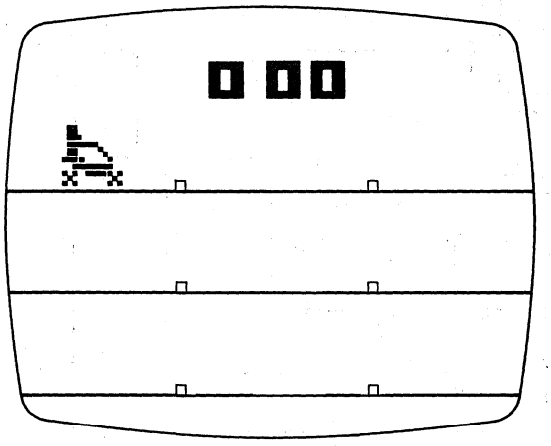
CONSUMER



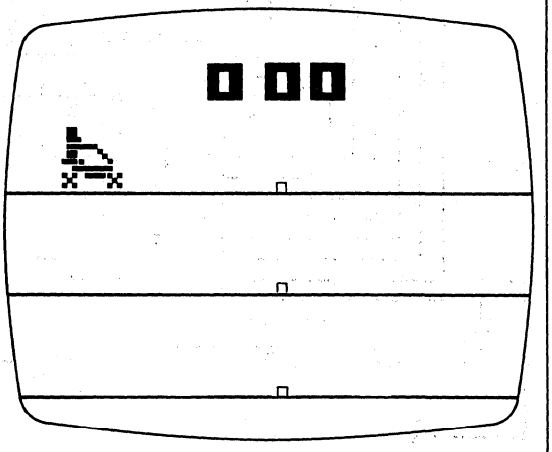
MOTO JUMP



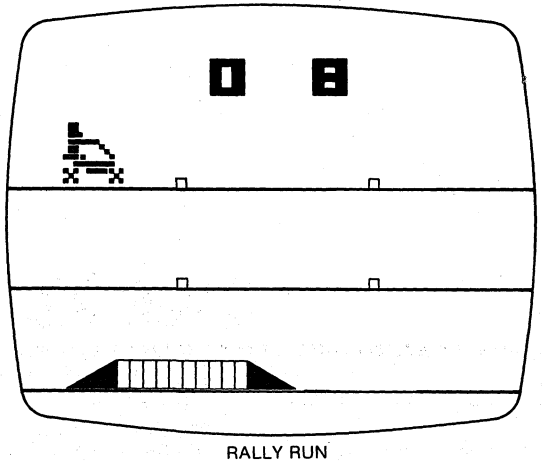
TIME OUT



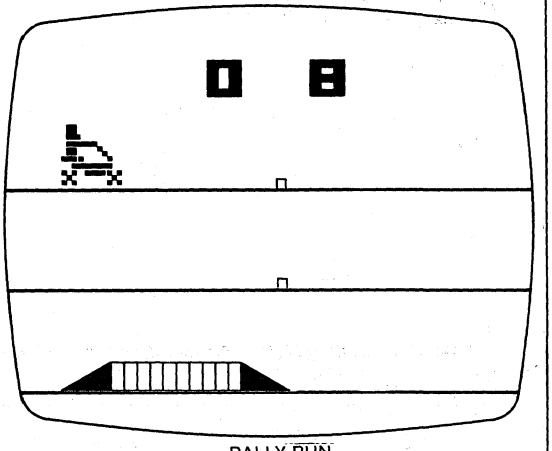
OBSTACLE RACE
(PRO MODE)



OBSTACLE RACE
(AM MODE)



RALLY RUN
(PRO MODE)



RALLY RUN
(AM MODE)

Clocks

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
4 DIGIT	12/24 hour clocks with features for most clock/timing applications.	AY-5-1202A	8-60
		AY-5-1203A	8-60
		AY-5-1224A	8-63
4 DIGIT CLOCK RADIO	12/24 hour clock, 24 hour alarm, sleep timer, battery standby.	CK3300	8-65

4 Digit Clock Circuits

FEATURES

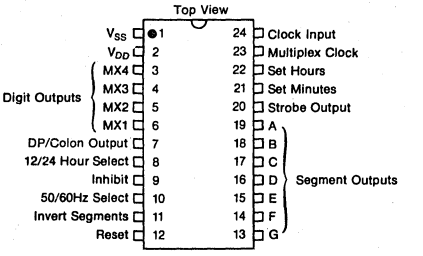
- Hours and minutes display
- 12/24 hour operation
- 50/60Hz operation
- High voltage direct Fluorescent drive Outputs
- Flashing seconds output (option)
- BCD output (option)
- Leading Zero Blanking (option)
- Power-On Reset to zero
  (Counting does not start until time is set.)
- Options:

	7 Seg	BCD	Zero Blank	Flashing Sec
AY-5-1202A	Yes	No	Yes	Yes
AY-5-1203A	No	Yes	No	Yes

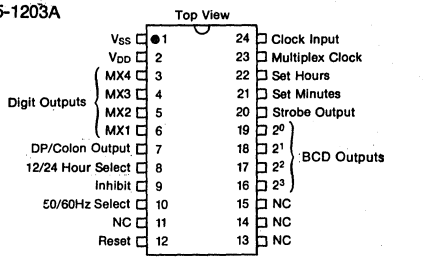
PIN CONFIGURATION

24 LEAD DUAL IN LINE

AY-5-1202A



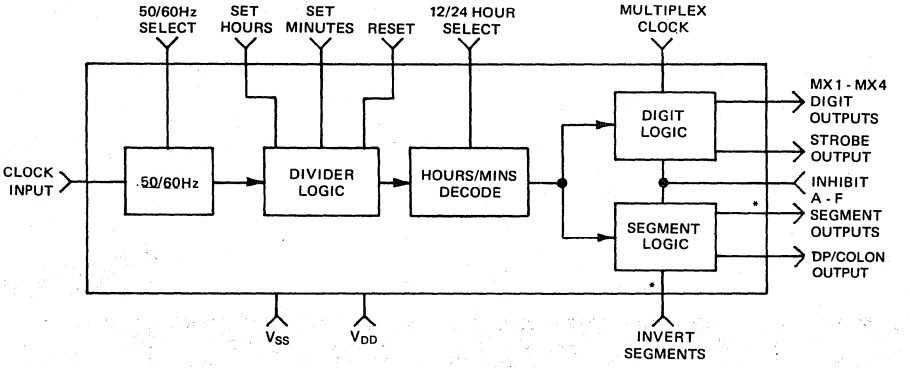
AY-5-1203A



DESCRIPTION

The AY-5-1202A and AY-5-1203A are P-Channel MOS integrated circuits, containing all the logic necessary to make a 4 digit, 12 or 24 hour clock, operating from 50 or 60Hz. High voltage output stages capable of driving fluorescent displays are provided.

BLOCK DIAGRAM



* Not included in the AY-5-1203A. Four BCD outputs are provided in place of the seven segment outputs.

CONSUMER

PIN FUNCTIONS

Name	Function
Segment Outputs A—F	In 7 segment mode the digits are multiplexed on to these pins. These outputs are at logic '0' to display (positive) and will drive Fluorescent displays directly. In BCD mode outputs A to D are used, the code for 0 being 0000.
DP/Colon Output	This is a high voltage output intended to drive a decimal point or colon. It is enabled during the MX3 time slot and can flash once per second if required.
Multiplex Outputs MX1—MX4	These outputs select the display digits sequentially, they will drive Fluorescent displays directly. Five multiplex time slots are generated the fifth one being blank. Minutes are output in MX1 time, 10's of hours in MX4 time.
Reset Input	When taken to logic '0' the clock is reset to zero.
Set Minutes Input	When taken to logic '0' the minutes counter is advanced at the rate of 2 min. per sec. and the hours counter at the rate of 2 hours per minute.
Set Hours Input	When taken to logic '0' the hours counter is advanced at the rate of 2 hours per second.
50/60Hz Select Input	When taken to logic '0', 60Hz operation will result.
12/24 Hours Select Input	When taken to logic '0', 12 hour operation will result.
Invert Segments Input	When taken to logic '0' the segment outputs will be inverted.
Multiplex Oscillator	An external capacitor is used to select the multiplex frequency. If required the pin can be driven by an external oscillator.
50/60Hz Input	The master clock is input to the pin. Hysteresis is provided so that the input waveform is not critical.
V_{SS}	Positive Supply.
V_{DD}	Negative Supply.
Inhibit Input	When taken to logic '0' all outputs are switched OFF.
Strobe Output	This is a short pulse occurring during the middle of each multiplex period.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin (except Segment and Multiplex outputs) . . . . . +0.3 to -35V
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -65°C to +150°C
Power Dissipation at +70°C Ambient—Total 500mW
Per Output. 50mW

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = - 0V
V_{DD} = -17V ± 10% (AY-5-1202A)
V_{DD} = -11.4V to -19V (AY-5-1203A)
Operating Temperature (T_A) = 0°C to +70°C

NOTE:
In the chart below, numbers in ( ) refer only to the AY-5-1203A.

Characteristic	Min.	Typ**	Max	Units	Conditions
Clock input frequency	DC	50/60	—	Hz	
Clock input logic '0'	+0.5	—	-2(-1)	Volts	Note 1
Clock input logic '1'	-8	—	V_{DD}	Volts	
Multiplex clock frequency	DC	—	50	kHz	Note 2
Control inputs logic '0'	+0.3	—	-1.5(-1)	Volts	
Control inputs, current logic '0'		100	—	μA	Note 3
Control inputs logic '1'	-6	—	$-V_{DD}$	Volts	
Segment Outputs					
ON current	2(1.3)	—	—	mA	V_{OUT} = -2V
OFF leakage		—	5(10)	μA	V_{OUT} = -25V(-19V)
		—	10	μA	V_{OUT} = -35V
Multiplex Outputs					
ON current	5(3.3)	—	—	mA	V_{OUT} = -2V
OFF leakage	—	—	5(10)	μA	V_{OUT} = -25V(-19V)
	—	—	10	μA	V_{OUT} = -35V
Supply Current	—	8.5(6.5)	14	mA	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. The clock input pin may be taken positive with respect to V_{SS} provided that the current is limited to 100μA. The input will behave like a forward biased silicon diode in this condition.
2. The frequency is determined by an external capacitor.
3. These inputs have a 170Kohm pull up resistor to V_{DD}.

CONSUMER

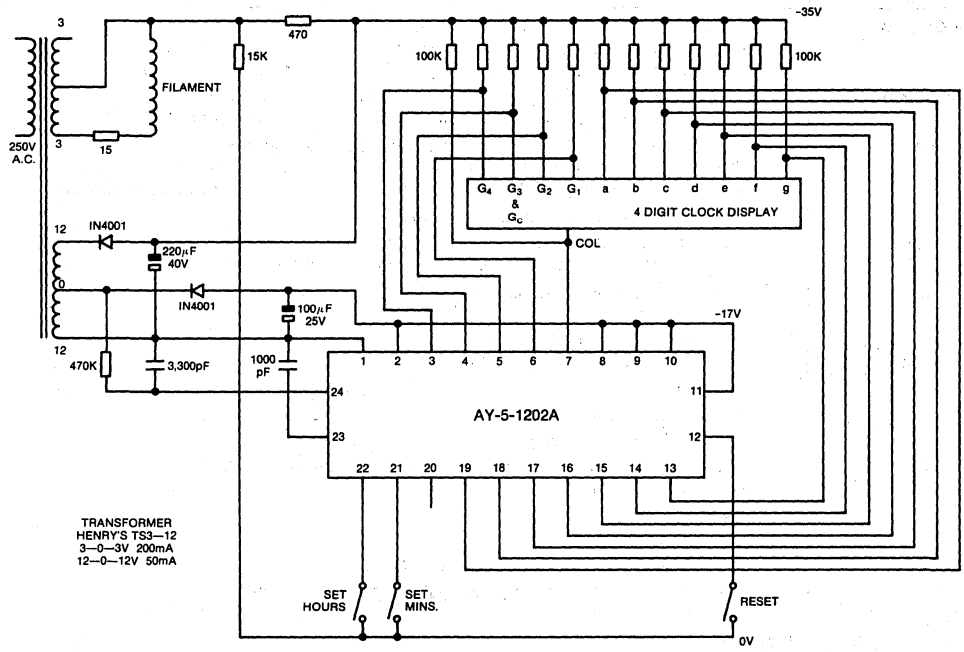


Fig.1. DIGITAL CLOCK CIRCUIT USING AY-5-1202A WITH FUTABA FLUORESCENT DISPLAY 5-LT-01

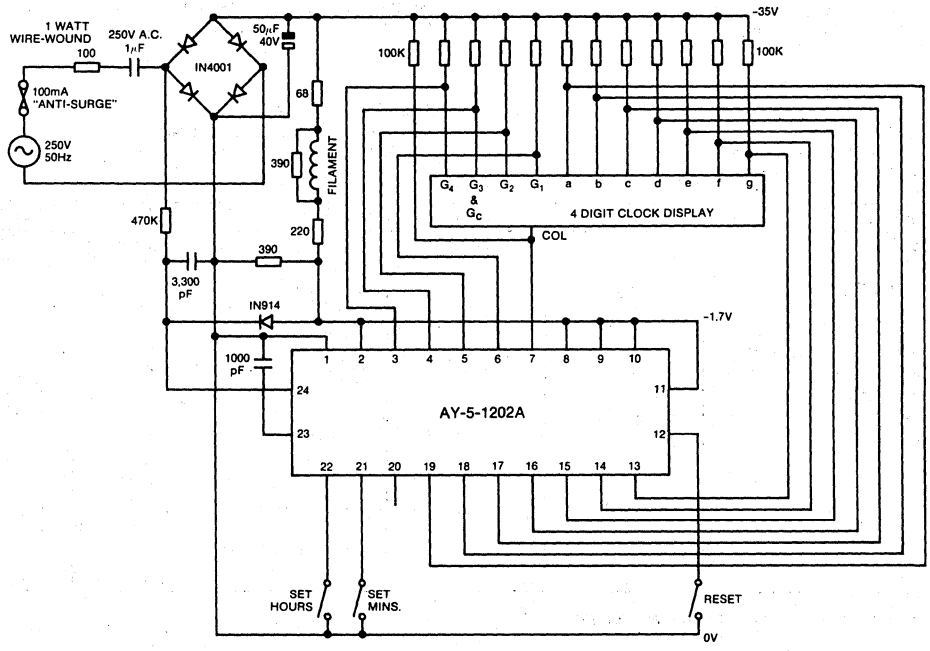


Fig. 2. DIGITAL CLOCK CIRCUIT USING AY-5-1202A WITH FUTABA FLUORESCENT DISPLAY 5-LT-01 AND CAPACITIVE POWER SUPPLY

CONSUMER

4 Digit Clock Circuit

FEATURES

- 12/24 hour operation
- Leading zero blanking in 12 hour mode
- 50 or 60 Hz clock input
- Hours and minutes display (4 digits)
- 7 segment outputs direct LED drive or TTL compatible BCD outputs
- Complement control for segment outputs
- Interdigit blanking for gas discharge displays
- On chip multiplex oscillator
- Single 15V supply
- Power-On Reset to zero (Counting does not start until time is set.)

DESCRIPTION

The AY-5-1224A is a P channel MOS integrated circuit containing all the logic necessary to make a 4 digit, 12 or 24 hour clock operating from a 50 or 60Hz input. It has multiplexed BCD or 7-segment outputs and will drive LED, Fluorescent and Gas discharge displays with the minimum of interfacing.

PIN FUNCTIONS

Pins 1 and 11 are multifunction. During multiplex times 1 to 4 they function as data outputs, either 7 segment code or BCD according to the display mode selected. During multiplex time 5 (Strobe) they function as inputs.

Segment Outputs A-G (Pins 1 and 11 to 16)
In 7 segment mode the digits are multiplexed out on to these pins. Normally the outputs are at logic '0' (positive to display). Interdigit blanking for ¼ the digit time is incorporated for gas discharge displays.

BCD Outputs 2^0—2^3 (Pins 1, 16, 15, 14)
In BCD mode the digits are multiplexed on to these pins in BCD code. Normally the outputs are at logic '0' (positive), i.e. code 0=0000.

Multiplex Outputs 1-4 (Pins 10, 9, 8, 7)
These pins are successively switched to logic '0' to select appropriate digit display. A fifth multiplex time (Strobe) is used to enable the control inputs. These outputs have interdigit blanking. The multiplex rate is 1/20th the multiplex clock frequency.

Strobe Output (Pin 6)
This pin is used to enable the control input keyboard, it goes to logic '0' to enable.

Set Hours Input (Pin 1)
When taken to logic '0' during strobe time this input causes the hours counter to advance at the rate of 1 hour per second.

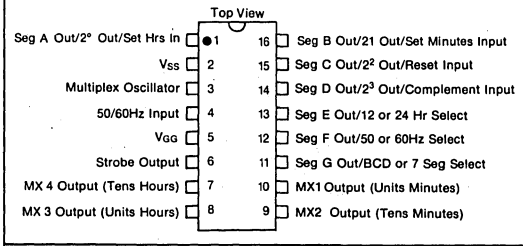
Set Min Input (Pin 16)
When taken to logic '0' during strobe time this input causes the minutes counter to advance at the rate of 1 per second and the hours counter to advance at the rate of 1 hour per minute.

Reset Input (Pin 15)
When taken to logic '0' during strobe time this input causes the clock to reset to zero.

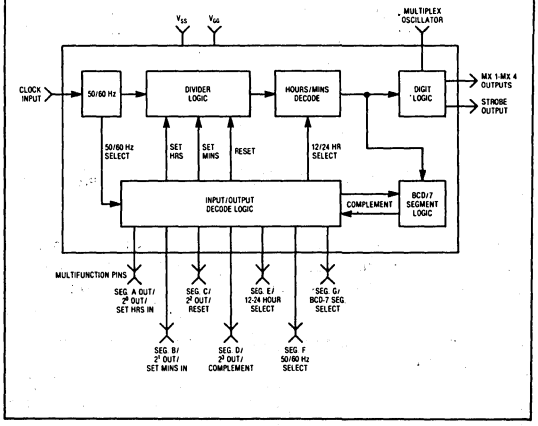
Complement Input (Pin 14)
When left open the segments and BCD outputs will have normal polarity. When connected to Strobe output via a diode the 7 segment and BCD outputs will be inverted.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



BLOCK DIAGRAM



12/24 Hour Select (Pin 13)
When left open the clock will run in the 12 hour mode, when connected to strobe via a diode 24 hour operation will result.

50/60Hz Select (Pin 12)
When left open a 50Hz clock will be accepted. When connected to strobe via a diode 60Hz operation will result.

BCD/7 Segment Select (Pin 11)
When left open 7 segment outputs will be provided, when connected to strobe via a diode BCD outputs will be provided.

50/60Hz Input (Pin 4)
The master clock (50 or 60Hz) is input to this pin. Hysteresis is provided on the input so that the input wave form is not critical.

Multiplex Oscillator (Pin 3)
An external capacitor is used to set the multiplex frequency. If required this input can be driven by an external oscillator.

V_{SS} (Pin 2)
Positive supply line nominally 0V.

V_{GG} (Pin 5)
Negative supply line nominally -15V.

Power-On Reset
At power-on the chip is reset to zero. Counters will not start until Set Hours or Set Minutes has been activated.

CONSUMER

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} . . . . . +0.3 to −20V
Operating Temperature Range . . . . . 0° to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Power Dissipation at 70°C Ambient—Total 500mW
Per Output. 50mW

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

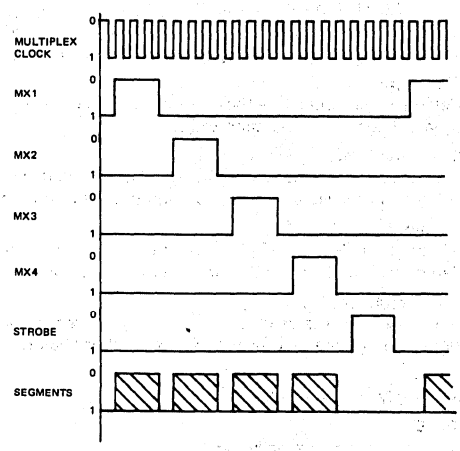
$V_{SS} = 0V$
$V_{GG} = -12$ to $-18V$
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Clock input frequency	DC	50/60	—	Hz	—
Clock input logic '0'	+0.5	—	−2	Volts	Note 1
Clock input logic '1'	−8	—	V_{DD}	Volts	—
Multiplex Clock Frequency	DC	—	50	kHz	Note 2
Interdigit Blanking	—	150	—	μs	at 6.67kHz Note 3
Control inputs logic '0'	+0.3	—	−1.5	Volts	—
Control inputs logic '1'	−6	—	V_{DD}	Volts	—
Outputs Logic '0'	—	—	500	Ω	$V_{OUT} = -2V$, $I_{OUT} = 4mA$
Outputs Logic '1' (Leakage)	—	—	10	μA	$V_{OUT} = -18V$
Supply Current	—	—	10	mA	$V_{GG} = -15V$

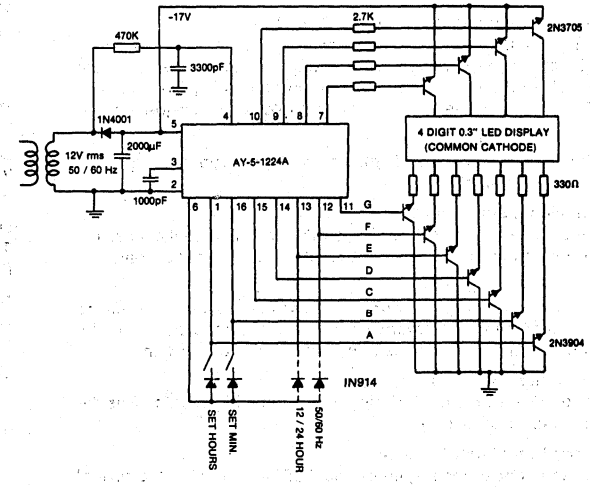
**Typical values are at +25°C and nominal voltages.

NOTES:
1. The clock input pin may be taken position with respect to V_{SS} provided that the current is limited to 100μA. The input will behave like a forward biased silicon diode in this condition.
2. The frequency is determined by an external capacitor.
3. At 6.67kHz multiplex frequency the digit ON time is 450μs and the OFF time is 150μs.

TIMING DIAGRAMS



AY-5-1224A WITH 0.3" LED DISPLAY



CONSUMER

4 Digit Clock Radio Circuit

FEATURES

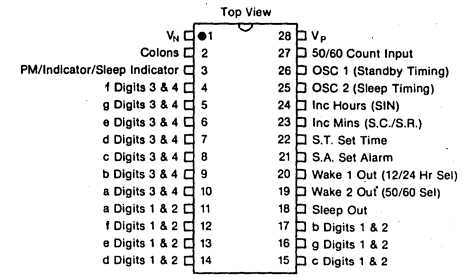
- 4 Digits plus colons
- LED direct duplex drive
- No display-IC interface components
- No radio frequency interference problems
- No external contact noise elimination circuits required
- No external line frequency noise rejection circuits required
- 12 or 24 hour display
- Leading zero suppression in 24 hour mode
- PM indication in 12 hour mode
- Alarm-snooze indicator
- 50Hz or 60Hz operation
- On-chip oscillator for standby operation with battery during line Failure
- Line power interrupt indication
- Sleep operation indicator
- Low power dissipation (under 30 mW)

CLOCK RADIO FEATURES

- Simple support electronics
- Analog sleep setting (user controlled 5 to 120 mins with 1 minute resolution). No necessity for daily adjustment
- Totally independent sleep and wake timing
- Independent volume of music during sleep and wake
- Radio sound muting during normal radio listening
- Wake to music or alarm tone
- Self-cancelling alarm after 80 minutes of wake
- 5 minute repeating snooze with radio and/or alarm
- Sleep override or sleep repeat
- Wake to alarm tone with quiet radio override (every 5 minutes) during snooze time (repeatable)
- Simple setting of time, alarm, and sleep
- Hold and synchronize capability for time setting
- Independent hours, minutes setting (carry propagation suppressed)
- 5 minute pre-alarm appliance switching
- Automatic tape recorder control (record your favorite program automatically 0-120 minutes—starting from the exact second)

PIN CONFIGURATION

28 LEAD DUAL IN LINE



DESCRIPTION

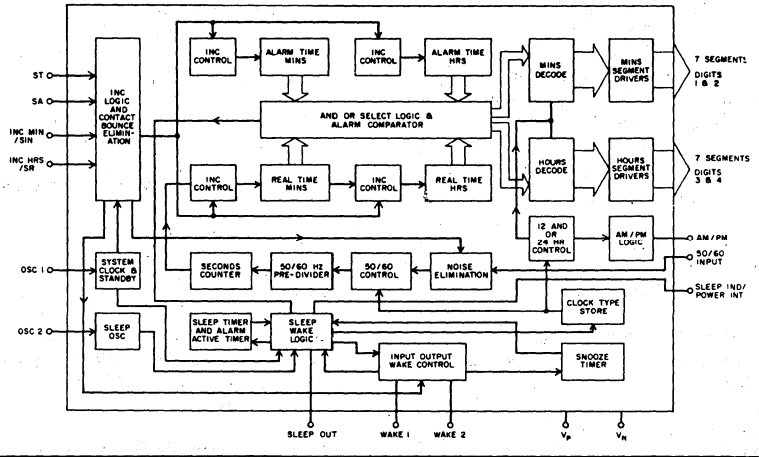
The CK3300 N-Channel MOS I.C. contains all the necessary logic, contact noise elimination circuits, control switching, segment drivers and timing circuits to implement simple-to-use, low cost, multi-featured clock radios.

Due to the extreme difficulties in eliminating R.F.I. in radios when used in conjunction with digital electronics a great deal of care has gone into the design of the L.S.I. to ensure that little or no R.F.I. problems are met by the clock radio designer. The largest R.F.I. problem in Display Driving has been solved using a novel technique—that of half-line cycle anode duplexing using the half-sine waves produced by two diodes, and ensuring that all segment data changes occur at the zero crossings of the line cycle. This technique allows brightness control to be achieved simply by resistively dividing down the line voltage with a potentiometer, or a simple two level scheme using a transformer tap.

Segment driving of the two groups is directly from the I.C. through 50 ohm switches which allow the high current peaks required of LEDs, up to one inch in size, while keeping the I.C. Power dissipation, for reliability, down to the 200 to 250 mW level.

The I.C. also contains many unique features which enable the equipment designer to put into the clock radio his company's own product image.

BLOCK DIAGRAM



CONSUMER

PIN FUNCTIONS

V_N - (Pin 1)
Is the most negative power supply to the chip (0 volts).

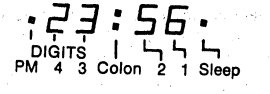
Segment Drivers (Pins 2-17)
These outputs are 50Ω switches which drive the segments of common anode LED's directly. Their use and operation is as follows:

To use the CK3300 with LEDs, the LEDs must be of the COMMON ANODE TYPE, and connected in the following manner.

segment a digit 1 connected to segment a digit 2
segment b digit 1 connected to segment b digit 2
segment c digit 1 connected to segment c digit 2
segment d digit 1 connected to segment d digit 2
segment e digit 1 connected to segment e digit 2
segment f digit 1 connected to segment f digit 2
segment g digit 1 connected to segment g digit 2
segment a digit 3 connected to segment a digit 4
segment b digit 3 connected to segment b digit 4
segment c digit 3 connected to segment c digit 4
segment d digit 3 connected to segment d digit 4
segment e digit 3 connected to segment e digit 4
segment f digit 3 connected to segment f digit 4
segment g digit 3 connected to segment g digit 4

Colon 1 segment connected to colon 2 segment
PM indicator segment connected to sleep/power down indicator segment
Anode digit 1 to anode digit 3
Anode PM indicator to anode digit 4
Anode sleep indicator to anode digit 1
Anode colon upper to anode digit 3
Anode digit 2 to anode digit 4
Anode colon lower to anode digit 2

The anodes can then be selected by the application of alternate half-cycle sine waves derived from a transformer from the line. The phase of the incoming 50/60Hz count to IC will then automatically deliver the correct segment data to the display.



Anode phasing: 50/60 high = digit (1 & 3) selected
low = digit (2 & 4) selected

Sleep Output (Pin 18)
This output turns on while the sleep counter is running and is indicated as active by an indicator in the display (Pin 3). This output turns on immediately following a sleep initiate and is cancelled either by sleep time being complete, a sleep cancel, an alarm comparison taking place, or an end of snooze period. This pin is also used as an input during circuit test to speed up testing.

Wake 2 Output/50-60Hz Mode Select (Pin 19)
This output turns on at alarm compare time and stays on unless either an alarm cancel or a snooze repeat is activated.

If snooze repeat is activated this pin will go off until the next 5 minute period elapses when it will again turn on.

The snooze can be repeated indefinitely.

If the alarm is not cancelled this output will turn off 80 mins after the last snooze repeat re-triggering alarm for the next 24 hour period.

This pin is also the 50/60Hz Select input during the time at which Set Time and Set Alarm are at a logic '1' (last data on this input when either Set Time or Set Alarm changes state is stored in an internal latch).

Wake 1 Output/12 Or 24 Hour Select (Pin 20)
This output turns on at alarm compare time and stays on uninterrupted until either:

a. An alarm cancel
b. 80 continuous minutes from alarm time
c. 80 continuous minutes from last snooze repeat

During the time that Set Time and Set Alarm are at a logic '1' together, this pin is the 12/24 hour select input.

The last data on this pin before a data change on Set Time or Set Alarm is stored internally in a latch, and defines 12 or 24 hour operation.

Set Alarm (Pin 21)
This pin, held at zero while Set Time is at a logic '1', enables the Increment Minutes and Increment Hours inputs to the alarm counter, such that each change of state (1→0) of the increment inputs will advance the appropriate counter by one unit.

Set Time (Pin 22)
Is identical in operation to the Set Alarm pin, but in this instance allows the counts to be entered into the time counter.

Taking both Set Time and Set Alarm to a logic '0' allows the Wake outputs to become active when the time reaches the alarm time. Returning either Set Time or Set Alarm to a logic '1' will cancel the alarm.

Increment Mins/Sleep Cancel/Snooze Repeat (Pin 23)
If Set Time or Set Alarm is at zero, this input provides one unit of increment for each logic transition from one to zero. (This input is de-bounced against switch noise). If both Set Time and Set Alarm are at a logic '1' or logic '0' and the sleep timer is running, a logic zero on this input will cancel sleep.

If both Set Time and Set Alarm are at a zero and the Wake outputs are active (i.e., post alarm time), then Wake 2 will be cancelled for a period of up to 5 mins when Pin 23 is taken to logic '0'. If this input is at zero when the alarm comparison takes place, then Wake 2 will stay off until 5 minutes have passed.

Increment Hours/Sleep Initiate (Pin 24)
If either Set Time or Set Alarm is at logic '0', this input provides one unit of increment to the required counter for each logic transition from 1 to 0. (This input is de-bounced against switch noise). If both Set Alarm and Set Time are at logic '1' or logic '0', this input will cause Sleep output to become active for the time resulting from current sleep oscillator frequency.

OSC 2 (Pin 25)
This pin produces a triangular wave oscillation depending on the value of resistance and capacitance. This oscillator is used to produce the sleep period by being gated internally with 160th of Osc 1 frequency (i.e. 50/60Hz).

Additionally connected to this pin is a low level detect circuit used with oscillator 1 for re-setting all internal logic to 12:00 in 12 hour mode and 0:00 in 24 hour mode. This low level detect is also used to detect that standby operation is required.

OSC 1 (Pin 26)
This pin produces a triangular wave oscillation depending on the external value of resistance and capacitance. The signal is used during normal operation to provide internally to the I.C.—
a. the internal timing for a series of one-shot gates
b. After division, the frequency to de-bounce other external pins via D-type latches. This frequency is further divided down to 50/60Hz and is used as the source frequency during standby operation.
Connected internally to this pin is a low level voltage detector which is used in conjunction with a low level voltage detector on Osc. 2 (pin 25) to reset all the internal logic to 12:00 in 12 hour mode and 0:00 in 24 hour mode. This low level detect is also used for test purposes.

50/60Hz In (Pin 27)
This input is the normal source of timing. This input drives both the internal count and the alternate half line selection of the segment outputs.
For equal brightness in the display this input must have a 1:1 mark space ratio (±20%).
There is no necessity for eliminating line noise externally when providing this input signal as an internal arrangement eliminates undesired counts.

V_P (Pin 28)
Is the most positive power supply to the chip (typically 10 volts)

CONSUMER

FUNCTIONAL OPERATION

Pins 19, 20, 23 and 24 are dual function pins which operate as inputs or outputs dependent on the state of the Set Time and Set Alarm inputs:

S.T.	S.A.	INC MIN	INC HR	SC/ SR	SIN	Wake 1	Wake 2	50/ 60	12/ 24
1	1	-	-	*	*	-	-	*	*
1	0	*	*	-	-	-	-	-	-
0	1	*	*	-	-	-	-	-	-
0	0	-	-	*	*	*	*	-	-

*Operable - Not Operable

Set time (S.T.)	Pin 22
Set alarm (S.A.)	Pin 21
Increment minutes (inc min)	Pin 23
Increment hours (inc hrs)	Pin 24
Sleep cancel (S.C.)	Pin 23
Snooze repeat (S.R.)	Pin 23
Sleep initiate (SIN)	Pin 24
Wake 1	Pin 20
Wake 2	Pin 19
50/60Hz Select	Pin 19
12/24Hr. Select	Pin 20

Using Wake 1 Or 2—Input/Output Functions

When the Set Time (S.T.) and Set Alarm (S.A.) inputs are at logic one, the IC outputs Wake 1 and Wake 2 become inputs to two bistable gates which store the logic conditions on those pins: 50/60Hz Select on the Wake 2 pin and 12/24Hr. Select on the Wake 1 pin.

50/60Hz Select

Set Time or Set Alarm must be at zero before data on Wake 2 changes, or clock can change its 50/60 pre-divide mode. To avoid this, the following circuit is recommended:

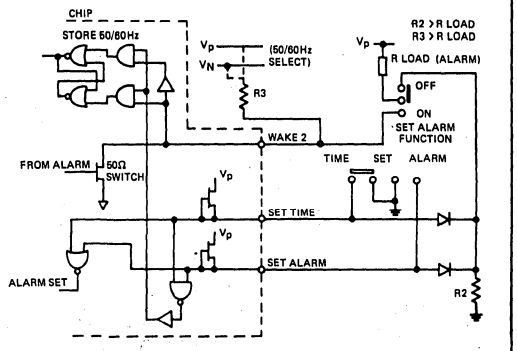


Fig.1 SUGGESTED USE OF WAKE OUTPUTS TO ENSURE PROPER OPERATION OF INPUT/OUTPUT FUNCTION

With the Set switch in the center position the set inputs are pulled up to a logic '1' by the IC, provided the Alarm switch is in the off position. The load (R load) will pull the junction of the two diodes and R2 to a logic '1'.

The output pin Wake 2 will either be pulled up or down depending on the connection of R3.

Changing of Set switch will pull down the appropriate input and not affect other external circuit conditions.

Change of position of alarm ON-OFF switch will allow R2 to pull down both Set inputs to zero before Wake 2 output is connected to load. This ensures that the internal IC latch is disconnected from wake line before data on wake line can influence stored data in latch.

12/24 Hr. Select

For the "Wake 1 output 12-24 hour select", changing the logic polarity will immediately change the displayed time from 12 hour mode to 24 hour mode or vice versa.

e.g. 21 : 56 becomes •9 : 56
or •9 : 56 becomes 21 : 56

No leading zero is shown in 24 hour mode:

12 : 32 in 12 hour time becomes 0 : 32 in 24 hour time

(Note: 12 to 24 hour displayed time change can only be achieved when the alarm is not requested and not in set mode)

For economy of LEDs a single dot is employed which is illuminated during the PM period in 12 hour time.

Time Setting

Four input pins (S.T., S.A., Inc Hr., Inc Mins.) are provided to enable the following four functions to be provided:

a. Setting the time
b. Setting the alarm
c. Stopping the clock
d. Starting the clock

For synchronizing purposes

S.T. = 0

Allows each depression of Inc Hrs to advance hrs by one count. Clock will stop on the first inc mins and will remain stopped until ST = 1, thus allowing synchronization. The device assumes that the hours may need to be changed without affecting mins, but assumes clock is incorrect if minutes are changed, thus stopping clock and re-setting internal seconds counter to zero.

S.A. = 0

Selects alarm time and, for each depression of Inc Hours, hours are advanced one and, for each depression of Inc Mins, minutes are advanced one.

NOTE:
No carries from minutes to hours occur during setting of time or alarm

Radio Control Inputs

The inputs S.T., S.A., Inc Min, Inc Hr, serve as radio control inputs under the following conditions.

S.T. And S.A.

At zero together—alarm is requested. S.T. and S.A. at logic one together—alarm not requested, but if taken to logic one during post alarm, alarm is cancelled.

S.T. and S.A. different will also cancel alarm if alarm is active.

S.T.	S.A.	Pre-Alarm	Post-alarm
1	1	Not required	Cancel
1	0	Not required	Cancel
0	1	Not required	Cancel
0	0	Requested	Alarm maintained for 80 mins

S.T., S.A. = 1

If S.T. and S.A. are at a logic 1 together during pre-alarm time, the following functions can be obtained using Inc Min—Inc Hrs inputs. Inc Hrs input going to logic zero for at least 20 msecs will result in sleep output going to zero for the period of time set by sleep potentiometer.

At any time Inc Mins input (SC/SR) going to zero for at least 20 msecs will cancel sleep timer if sleep output is active.

To reduce the number of knobs, switches, wiring etc., in the clock radio the following alternative feature is provided. If (S.C./S.R.) is wired to (SIN) a dual action is achieved, 1st depression of switch activates sleep, 2nd cancel sleep, 3rd re-activates etc. This allows features (a) if user decides he wishes radio off after he has been in bed for a few minutes, he pushes button, or (b) radio goes off automatically because sleep period has finished, but user is not asleep and would like radio to continue, so he presses button again.

S.T., S.A. = 0

In pre-alarm period the function performed when S.T., S.A. = 1 is identical. (When the alarm sounds at the requested alarm time the input (S.C./S.R.) (Inc Mins) becomes the 5 min snooze repeat input.)

At alarm, the effect of (S.C./S.R.) becoming zero for at least 20 msecs is to turn Wake 2 output off until next 5 min interval, if again depressed, Wake 2 will turn off for a further 5 mins—this sequence will go indefinitely until S.T., or S.A. or both are returned to logic '1', cancelling alarm. If inputs to the device are left unchanged for 80 mins then alarm will re-set for 24 hours.

Again to improve the radio features and simplify radio operation the tied function of (S.C./S.R.) and (SIN) on one button performs the following three functions:

Initiate sleep (SIN)
Cancel sleep (S.C.)
Snooze repeat (S.R.)

Delaying Alarm by 5 Minutes

If, when Wake 1 ouput is capacitively coupled to (S.C./S.R.) input then at alarm time Wake 1 will turn on and stay on but Wake 2 will immediately become cancelled, hence no alarm will be heard from radio until 5 minutes later; this allows an electrical appliance to be turned on 5 minutes prior to alarm sounding.

Use of Sleep Timer for Tape Recorder Control

If sleep input (SIN) in directly coupled to Wake 1 output, then a tape recorder or any electrical equipment can be turned on at alarm time using sleep output for a period of time set on sleep potentiometer.

Radio Control Outputs

There are three radio control outputs:

a. Wake 1
b. Wake 2
c. Sleep output

Function

1. Wake 1—goes at zero; i.e. is on at alarm time for a period of 80 mins or until an alarm cancel.

2. Wake 2 goes to zero at alarm time, and stays at zero until a snooze repeat is activated then it will stay off until next 5 minute point then return to zero, for a period of 80 mins unless snooze repeat is re-activated. Snooze repeat can be used indefinitely, until either a continuous 80 mins occurs or alarm is cancelled.

Note: The 5 minute period is any 5 min interval from alarm time and not 5 min from each snooze repeat.

3. Sleep output goes low after a sleep initiate for the period of time set by sleep potentiometer. (Will be overridden by Wake if sooner.)

Colon Utilization

	COLON CONDITIONS	
FUNCTION	BOTTOM	TOP
Set time	on	off
Set alarm	off	on
Stopped (Sync)	off	off
Run (alarm not requested)	1Hz	off
Run (alarm requested)	1Hz	1Hz
Snooze period	1Hz	1Hz

Sleep dot is on for sleep timer running, flashing for post line interrupt (removed from flashing by movement of S.T. or S.A. to '0')

Stand-By Operation

If a circuit is employed to change the IC power source to battery during line failure, e.g. two diodes, then if the external timing components of oscillator 1 are set to give 8kHz (nominally R = 120KΩ = 2200pF), then the IC will maintain operation to an accuracy of one part in 120, i.e., 30 secs/hr, during the failure. On return to main power the sleep indicator will flash at 1Hz to notify user that indicated time could be in error.

The standby condition is detected by the failure of oscillator 2 to oscillate, therefore oscillator 2 is connected to the line-derived. power source, not the battery.

It is assumed OSC 2 input has gone to zero volts.

To remove flash condition take S.T. or S.A. momentarily to zero.

Analog Sleep Control

A second oscillator is provided on IC whose frequency can be controlled by an RC network. The oscillator is identical to oscillator one (Standby oscillator) and occupies the same silicon real estate location ensuring that process variations, temperature variations and voltage variations have as nearly as possible identical effects on frequency stability. Oscillator 1, which is set to 8KHz is divided down to 50Hz (20.0 msecs) and is used as a gating time for oscillator 2 (Sleep Timer Source). The number of gated counts is loaded in the sleep timer (capacity 160 counts) and subsequently counted up at one per minute until 160 is reached.

The range of sleep time is controlled by varying OSC 2 resistance. At 4:1 change in resistance will give variation of 160 to 40 gated pulses, this giving a sleep time of 0 to 120 minutes.

NOTE:
Minimum sleep time to ensure correct snooze operation should be a minimum of 5 minutes.

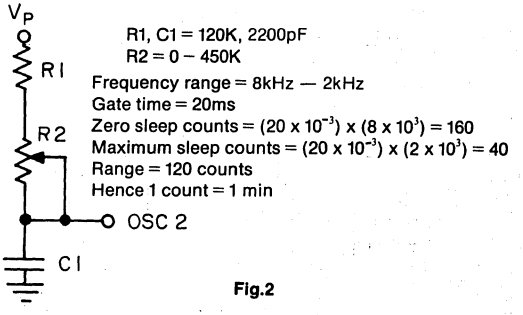


Fig.2

To initiate the sleep timer both S.T. and S.A. must logically be the same, and INC HR/SIN must be momentarily at zero. (See later section).

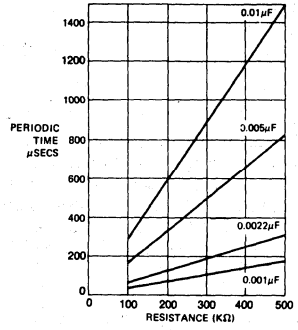


Fig.3 OSCILLATOR CHARACTERISTICS FOR V_P = 10V

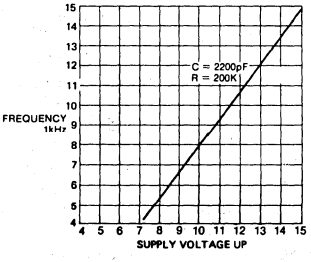


Fig.4 OSCILLATOR CHARACTERISTICS WITH VOLTAGE

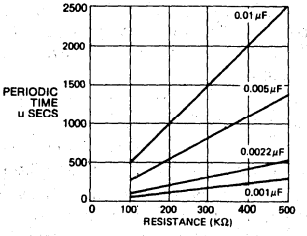


Fig.5 OSCILLATOR CHARACTERISTICS FOR V_P = 7.5V

CONSUMER

Operation Clock Radio Example
(showing some features and their use) - ref Figs.21 and 22.

Start-Up
Radio is connected to line for 1st time, then battery is inserted.

Assume following switch position RADIO OFF, SET TIME SWITCH = RUN

Actions
Display will illuminate and read 12:00 sleep indicator will flash at 1Hz. Set clock as indicated previously (Flashing will cease).

In 24hr mode 0:00 will illuminate with flashing sleep indicator.

Snooze Bar Action
IN RADIO OFF POSITION

1st button depression	Low volume radio (set required volume)
2nd button depression	Radio off
3rd button depression	Radio on low volume
4th button depression	Radio off

etc. . . .

IN RADIO ON POSITION
Radio comes on high volume (set wake volume required)

1st button depression	Low volume radio (mute facility)
2nd button depression	High volume
3rd button depression	as 1
4th button depression	as 2

Radio Auto
In auto, alarm is requested at "set alarm" time. If sleep is desired press button. Subsequent button pushes will have same effect as in radio "off" position.

Select Wake to Alarm Tone or Radio
Assume radio selected

At alarm time radio will come on at wake volume setting.

1st button depression	Radio will switch to low volume
2nd button depression	Radio will switch off
3rd button depression	Radio back a low volume

If after first depression radio is left untouched, radio will return to wake volume after five minutes.

If after 2nd depression radio is left untouched, radio will stay off for five minutes then return to wake volume.

This wake volume, if left, will be maintained for 80 mins unless radio is returned to radio ON or radio OFF switch position, changing switch momentarily from auto to ON or OFF and back to auto will reset alarm and re-request for same time next day. The above, repeating snooze, can be maintained indefinitely if button is pushed before 80 mins elapses.

Note: 80 mins is timed either from alarm time, if untouched, or 80 mins from last button depression

Select Wake to Alarm Tone
The alarm tone or buzzer is obtained by placing positive feedback around the audio amplifier or radio in such a manner that the desired sound can be achieved and the feedback can be stopped by open circuit one point in the network.

At alarm time buzzer will sound:

On 1st button depression	Buzzer will cease and radio will switch to low volume
2nd button depression	Radio and buzzer will be off

If after first depression radio is left untouched, radio will return to buzzer after 5 mins.

If after 2nd depression radio is left untouched, radio and buzzer will be off and at 5 mins BUZZER WILL AGAIN SOUND.

As for radio position—radio will reset after 80 mins for 24 hrs. At any time in buzzer sequencing, buzzer radio select can be changed over to radio, then the radio will alternate high-low volume with button. Cancelling in buzzer mode is identical to radio mode.

Typical Application
To combine the S.A. and S.T. functions to provide simple and rapid clock setting. It is suggested that the follwing is incorporated in the clock radio.

Two toothed wheels are placed over two separate sprung contacts and coupled to two concentric rotating knobs, (say 12 teeth each) along side is a three position switch labeled 'set time, run, set alarm'.

To set clock, select time or alarm and rotate Hrs knob, or mins knob, each click will result in one unit change of time, rapid rotation will result in 12 increments per revolution of knob.

The above procedure results in an easy to use system with the advantage over mechanical clocks of independent hrs and mins setting.

NOTE:
No carries from mins to hrs can occur during setting of time or alarm.

Use of Auto Tape
Fig.21 shows - the facility for automatically switching on an appliance (e.g. tape recorder) at a specific time and keeping appliance active for a period of time up to 120 mins. In this mode the wake output is made to start the sleep - timer at the wake time.

Use of 5 Min Delayed Alarm with Appliance Switching
In this mode of operation the wake 1 output is made to cancel the first alarm through the SC (inc hr) input such that radio or alarm time will only occur at the end of the first snooze period.

This result in appliance being activated at set alarm time and after 5 mins the alarm or radio will sound.

Fig.6 — shows a typical clock-radio block diagram
Fig.7 — shows the chip/display circuit.

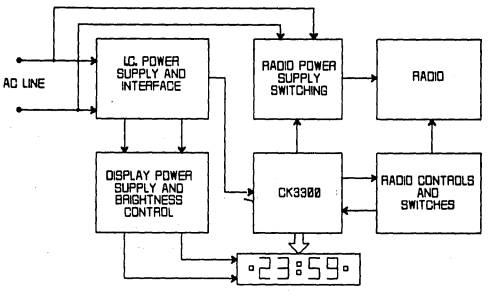


Fig.6

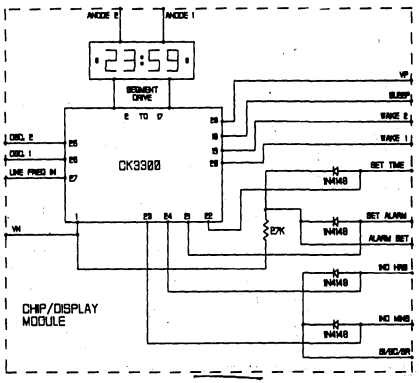


Fig.7

Interface with a Radio

There are many possible configurations of clock radios in use today and a wide range of different radio chassis are employed in these units. It is necessary therefore that the clock radio I.C. be sufficiently flexible to allow simple interfacing to be accomplished.

The following section gives different options, features and interfacing to demonstrate some of the approaches possible with the CK3300.

Power Supply Interface

To enable any existing line operated radio chassis to be used with the minimum of changes it is suggested that the following power supply is used with the adoption of a 2nd line transformer. This will (a) reduce the need for a change at the existing transformer. (It is unlikely that the existing transformer will be capable of providing the additional power required of the display).

a. Allow the electronic clock movement to be self contained therefore, keeping the interface wiring to a minimum.

b. Allow the same electronic movement to be used with several radio chassis.

Options

1. Without battery standby facility Fig.8
2. With battery standby facility Fig.9

Display Interface and Power Source

Four options are shown

1. No brightness control Fig.10
2. Day/night brightness (two level) Fig.11
3. Manual brightness control Fig.12
4. Automatic brightness control Fig.13

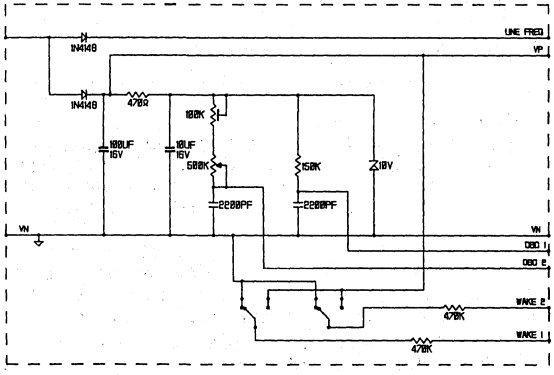


Fig.8 POWER SUPPLY INTERFACE WITHOUT STANDBY

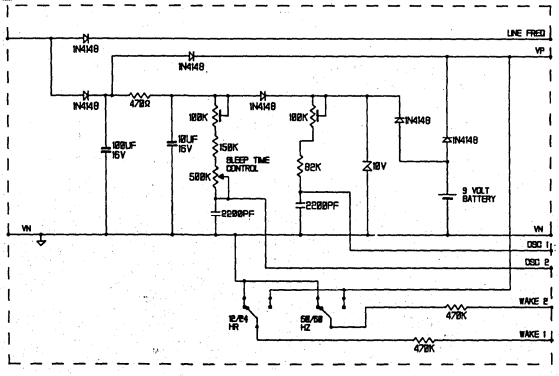


Fig.9 POWER SUPPLY INTERFACE WITH STANDBY OPTION

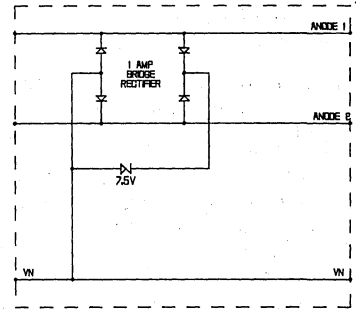


Fig.10 NO BRIGHTNESS CONTROL

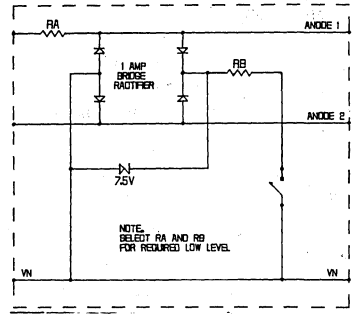


Fig.11 TWO LEVEL BRIGHTNESS CONTROL

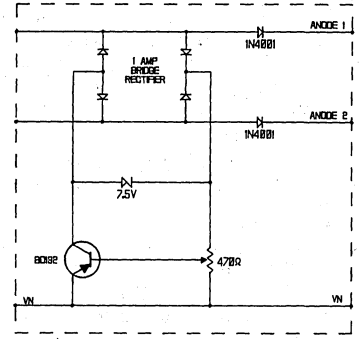


Fig.12 MANUAL BRIGHTNESS CONTROL

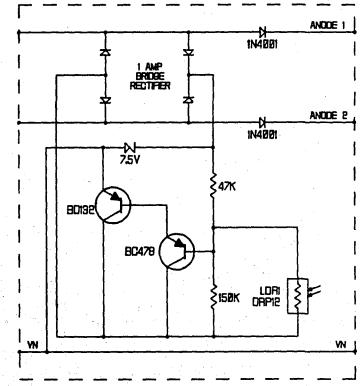


Fig.13 AUTOMATIC BRIGHTNESS CONTROL

Radio Switching
Option 1 Push button operation (Fig.14)
Option 2 Rotary switch operation (Fig.15)

Radio Powering
Option 1(Fig.16A, 16B) Direct audio amplifier control (no active components)
Option 2 (Fig.17) Power supply switching using Transistor
Option 3 (Fig.18) Power supply switching using a relay

Tone Generation
Option 1 (Fig. 19) Saw tooth generation independent of radio
Option 2 (Fig.20) Sine wave generation independent of radio
Option 3 (Fig.15,16B) Sine wave using the existing radio audio amplifier

Additional Facilities
1. Automatic tape recording (Fig.21)
2. Appliance switching with delayed alarm (Fig.21)
3. Wake to normal radio with 5 minute alarm over-ride (Fig.21)
4. Wake to quiet radio with 5 minute alarm over-ride (Figs. 21 and/or 22)
5. Ratio muting during normal radio listening (Figs.21 and /or 22)

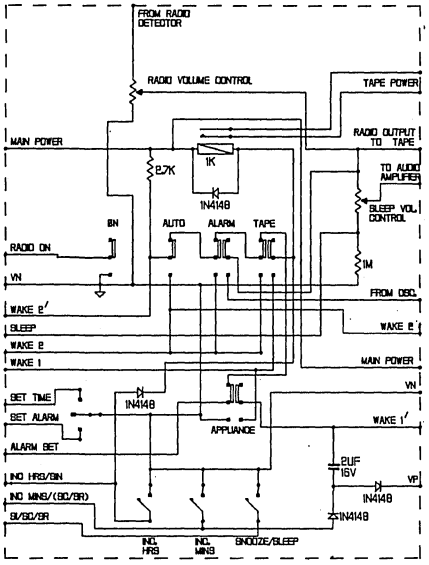


Fig.14 RADIO SWITCHING

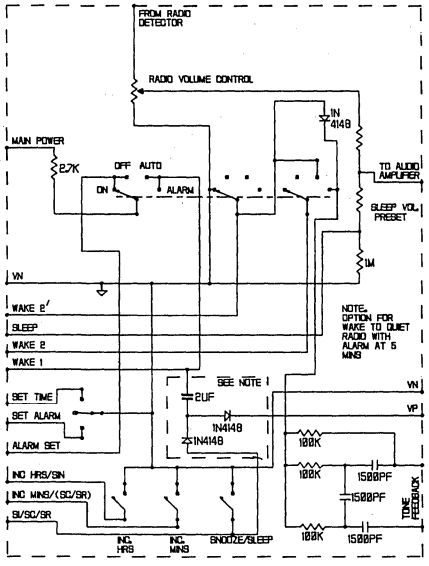


Fig. 15 RADIO SWITCHING

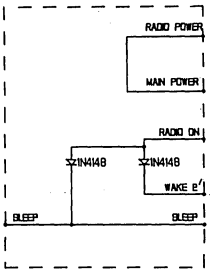


Fig. 16a RADIO SWITCHING BY BIAS CHANGE

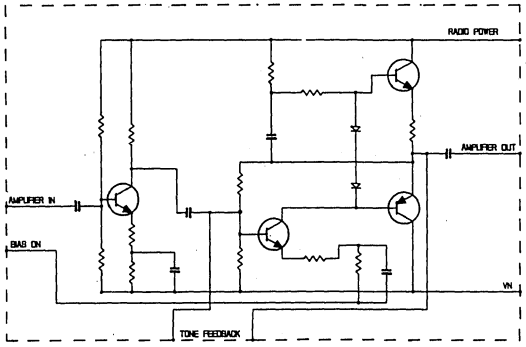


Fig. 16b TYPICAL TRANSFORMERLESS AUDIO AMPLIFIER

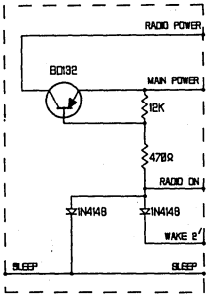


Fig.17 RADIO POWER SWITCHED BY TRANSISTOR

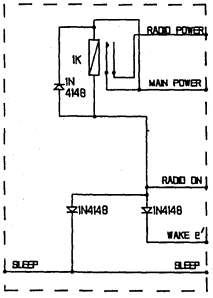


Fig.18 RADIO POWER SWITCHED BY RELAY

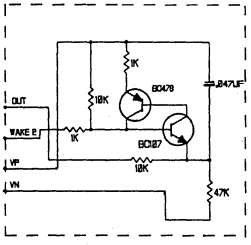


Fig.19 SAW TOOTH OSC

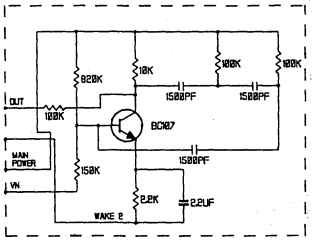


Fig. 20 SINE-WAVE OSC

CONSUMER

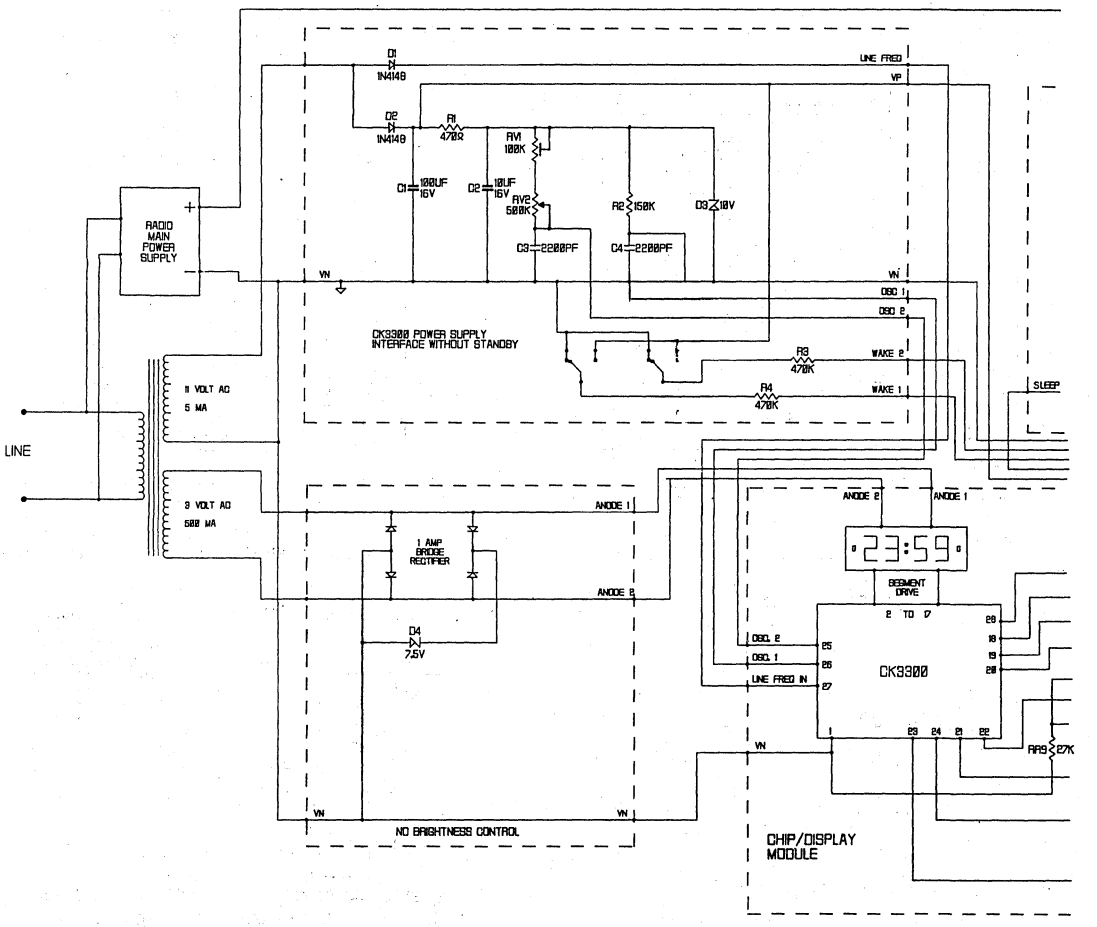


Fig.21(a) TYPICAL "BASIC" CLOCK RADIO CIRCUITRY

Appliances

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
CLOCK/TIMERS	24 hour programmable, repeatable on/off time switch with 4 digit clock.	AY-5-1230	8-78
		AY-5-1231	8-78
		AY-5-1232	8-78
DIGITAL THERMOMETER	Digital Thermometer and temperature controller.	AY-3-1270	8-82

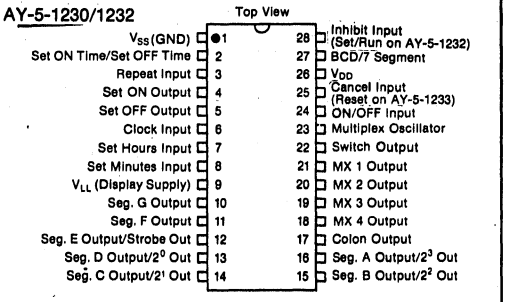
Clock / Timers

FEATURES

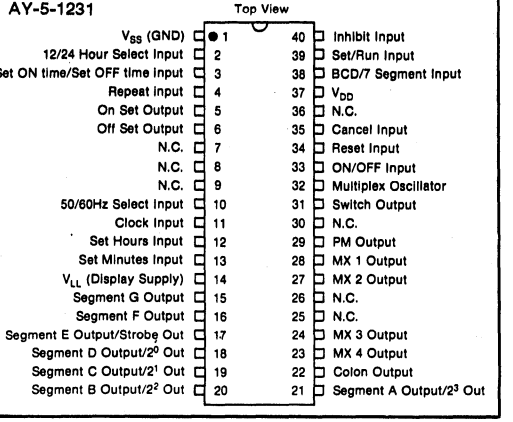
- 4 Digit Clock
- Drives 7 segment Fluorescent Displays
- Programmable switch on and switch off times
- Repeating or non-repeating operation
- Dimming control
- Power on reset, remains reset until time is set
- Foolproof switch on/off setting, if switch off time not programmed output stays on for 10 minutes only
- Non-multiplexed set inputs for low radiated noise
- Indication of set alarm state
- AY-5-1230/1232: 50Hz Input. 24 hour operation
- AY-5-1231: 50/60Hz Input, 12/24 hour operation

PIN CONFIGURATION

28 LEAD DUAL IN LINE
AY-5-1230/1232



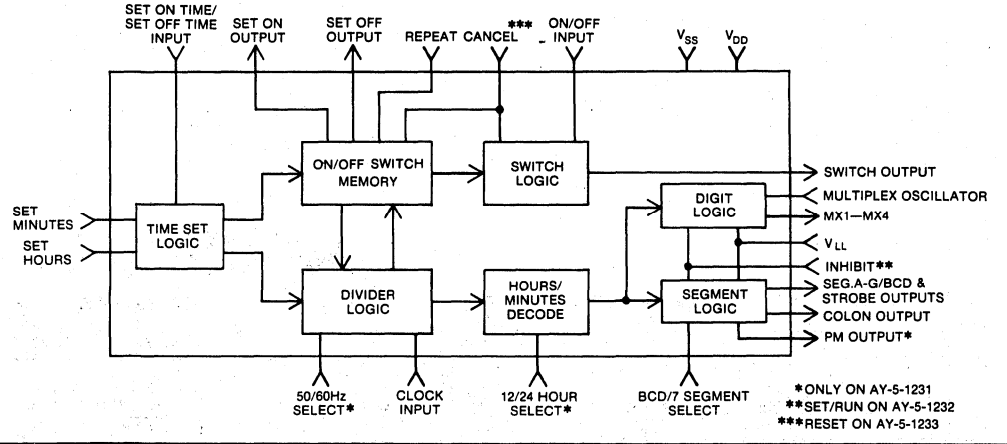
40 LEAD DUAL IN LINE
AY-5-1231



DESCRIPTION

The AY-5-1230 Series Clock/Timers are circuits designed to provide a four digit clock display and automatic on/off switching of a TV or other appliance at any desired time. A typical application would be the use of an AY-5-1230 Series circuit with GI's AY-5-8320 TV Time/Channel Display circuit to provide a clock display and automatic on and off switching of the TV at any desired time.

BLOCK DIAGRAM



CONSUMER

PIN FUNCTIONS

AY-5-1230 Pin. No.	AY-5-1231 Pin No.	AY-5-1232 Pin No.	Name	Function
1	1	1	V_{SS}	Positive Supply
2	3	2	Set ON time/ Set OFF time Input	When taken to logic '0' the ON time is displayed and the Set hours and Set minutes inputs operate the ON time counter. When taken to logic '1' the OFF time is displayed and the Set hours and Set minutes inputs operate the OFF time counter. When left open circuit the time is displayed. When either Set ON or Set OFF is activated the Switch logic is set and the switch output will operate at the set times.
3	4	3	Repeat Input	When connected to logic '0' the Switch output comes on every 24 hours. When left open circuit the Switch output comes on only once after which the Switch logic is reset. The switch logic can be set again by pressing Set ON and Set OFF.
4	5	4	Set ON Output	This output goes to logic '0' when an ON time has been set. It returns to '1' when the switch logic has timed out or has been cancelled.
5	6	5	Set OFF Output	This output goes to logic '0' when an OFF time has been set. It returns to '1' when the switch logic has timed out or has been cancelled.
6	11	6	Clock Input	The timing clock is input to this pin. Hysterisis is provided so that the input waveform is not critical.
7	12	7	Set Hours Input	When this input is taken to logic '0' the hours counter is advanced twice per second.
8	13	8	Set Minutes Input	When this input is taken to logic '0' the minutes counter is advanced twice per second. During setting the minutes counter does not overflow into the hours counter.
9	14	9	V_{LL} (Display Supply)	The on chip pull down resistors provided for each high voltage output are connected to this pin. When driving fluorescent display this pin is connected to -32 Volts.
10-16	15-21	10-16	7 Segment Outputs	High voltage outputs capable of driving fluorescent displays directly. At logic '0' to display. They have on-chip pull down resistors to V_{LL}.
13-16	18-21	13-16	BCD Outputs	In the BCD mode the time data is output on these pins.
17	22	17	Colon Output	This high voltage output is enabled on MX3 time and flashes once per second.
18-21	23,24 27,28	18-21	MX4-MX1 Outputs	These outputs are switched to logic '0' successively to select the digits, MX4 is 10s hours, MX1 is units mins. There are 5 time slots the fifth being blank. These outputs are high voltage and have on-chip pull down resistors to V_{LL}.
22	31	22	Switch Output	This output goes to logic '0' when the ON time is reached and returns to logic '1' when the OFF time is reached. If an OFF time has not been programmed the output will return to logic '1' ten minutes after the ON time has been reached. The output will sink 30mA.
23	32	23	Multiplex Oscillator	Not used normally. An external capacitor can be connected to reduce the mux frequency, or an external clock can be applied if required.
24	33	24	ON/OFF Input	When this input is taken to logic '0' the switch output is alternately turned ON and OFF. This input has antibounce logic to prevent maloperation.
25	35	25	Cancel Input	When this input is taken to logic '0' the Switch logic is reset and the Switch output turned off.
26	37	26	V_{DD}	Negative supply 15V nom. (11-19V)
27	38	27	BCD/7 Segment Select	When this input is wired to logic '0' BCD operation results.
28	40	—	Inhibit Input	When this input is taken to logic '0' display outputs are switched off. This input can be used for display dimming.
—	2	—	12/24 Hour Select	When connected to V_{SS} selects 12 hour operation.
—	10	—	50/60Hz Select	When connected to V_{SS} selects 60Hz operation.
—	29	—	PM Output	This output is on during the PM period. It is a high voltage output enabled at MX4 time slot.
—	39	28	Set/Run Input	When taken to logic '1', the clock is stopped and the seconds counter is reset to zero.
—	34	—	Reset Input	When taken to logic '0', this input resets either the clock, the "on" time, or the "off" time, depending on the state of the Set ON and Set OFF inputs.

NOTE:
1. All inputs have a pull down resistor to V_{DD}.
2. At power-on the chip is reset but the clock does not start to count until either the set hours or set minutes button has been pressed.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin (except display pins) with respect to V_{SS} pin . . . . . +0.3 to −20V
Voltage on display pins with respect to V_{SS} pin . . . . . +0.3 to −35V
Operating temperature range . . . . . 0°C to +70°C
Storage temperature range. . . . . −55°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = −11 to −19V
V_{LL} = −31 to −33V
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Min	Typ**	Max	Units	Conditions
Clock Input					
Frequency	—	50/60	—	Hz	50Hz only on AY-5-1230/1231/1232.
Logic '0'	+0.5	—	−2	Volts	Note 1
Logic '1'	-10	—	−19	Volts	
Multiplex Clock Frequency	—	100	—	kHz	Note 2
Control Inputs					
Logic '0'	+0.3	—	−1.5	Volts	
Logic '1'	−6	—	−19	Volts	
Pull Up Resistance	—	200	—	KΩ	to V_{DD}
Segment Output					
Logic '0'	—	—	−2	Volts	I_{OUT} = 2mA
Logic '1'	—	—	10	μA	V_{OUT} = −35V
Mx Outputs					
Logic '0'	—	—	−2	Volts	I_{OUT} = 5mA
Logic '1'	—	—	10	μA	V_{OUT} = −35V
Pull Up Resistance	—	200	—	KΩ	to V_{LL}
Switch Output					
Logic '0'	—	—	−2	Volts	I_{OUT} = 30mA
Logic '1'	—	—	10	μA	V_{OUT} = −19V
Set ON, OFF Outputs:					
Logic '0'	—	—	−2	Volts	I_{OUT} =2mA
Logic '1'	—	—	10	μA	V_{OUT} = −19V
Power Supply Current	—	6	13	mA	V_{DD} = −11V
	—	8	17	mA	V_{DD} = −19V

**Typical values are at +25°C and nominal voltages.

NOTE:
1. The clock input may be taken positive provided that the current is limited to 100μA
2. This results in a multiplex rate of 5kHz.

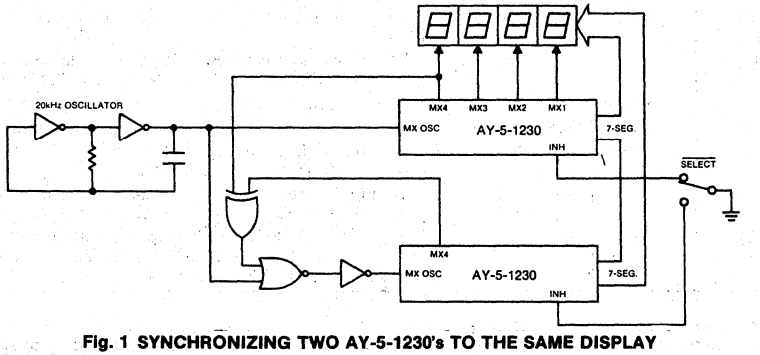


Fig. 1 SYNCHRONIZING TWO AY-5-1230's TO THE SAME DISPLAY

CONSUMER

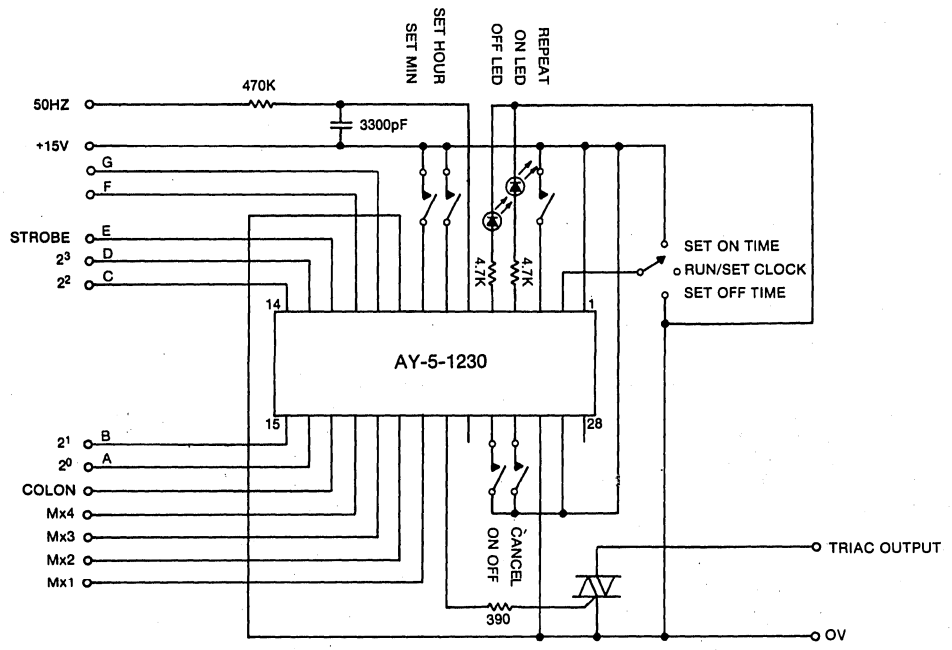


Fig. 2 AY-5-1230 CONNECTION DIAGRAM

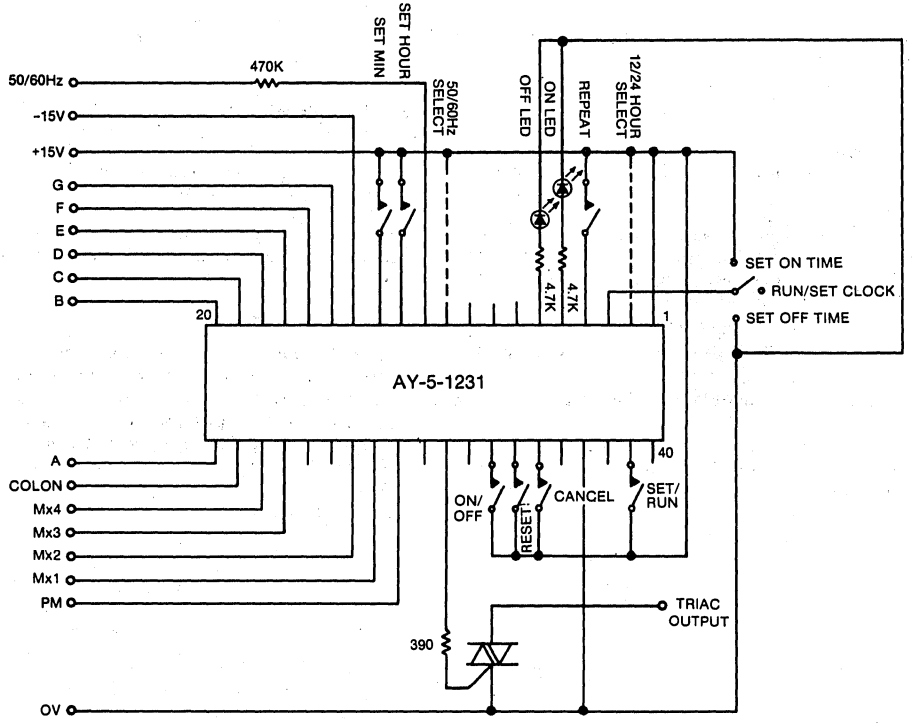


Fig. 3 AY-5-1231 CONNECTION DIAGRAM

CONSUMER

Digital Thermometer and Temperature Controller

FEATURES

- Measurement and control range −39.9°C to +39.9°C (option 20°C to 49.9°C)
- Accuracy ±1.0°C, 0°C to −30°C using Thermistor temperature sensor
- Direct drive of liquid crystal displays
- Direct drive of 0.6" common anode L.E.D. displays
- 40 pin dual in line package
- Can be used as a digital voltmeter with digital autozero ±399 range
- 9 volt supply
- Leading zero blanking
- Power failure and over-range indication by flashing display
- Adjustable Hysteresis 0, 0.2, 0.4, 0.8, 2, 4, 8 degrees
- Two control/alarm outputs, HIGH and LOW

DESCRIPTION

The Digital Thermometer/Controller chip is an N-Channel MOS integrated circuit which when used in conjunction with a Thermistor, an L.E.D. or L.C.D. display and a power supply forms a complete unit intended primarily for use in Deep Freezers, though it may also be used for the display and control of any parameter.

Two control outputs are provided, one which operates when the reading is higher than the set point and the other when the reading is lower. The switching hysteresis is presettable as required.

A power fail detector is incorporated on the chip. If power is removed for more than a specified time, the initial reading at restoration of power will be retained and the display will flash. The display will also flash if during normal operation an over-range condition occurs.

With minor changes to the peripheral circuitry, the chip can be used for other temperature ranges, or used as a 2¾ digit digital voltmeter.

OPERATION

The chip uses a single ramp conversion technique to measure the imbalance of a thermistor bridge temperature sensor. A digital autozero system which operates on every other measurement cycle, is employed to compensate for offsets in the comparators.

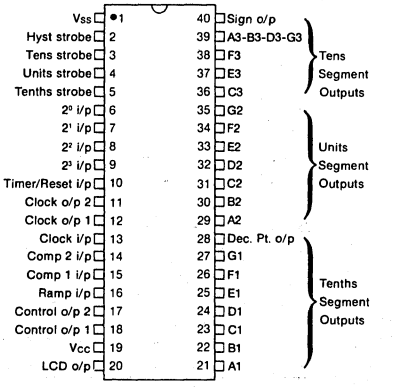
The chip may be used as a digital voltmeter by removing the thermistor network and connecting the signal to be measured between the two comparator inputs.

The set point circuitry compares the actual reading to the value presented to the set point inputs.

Two outputs are provided, one which operates at Set Point plus Hysteresis and the other which operates at Set Point minus Hysteresis. In addition, .05° display hysteresis has been introduced to prevent control output and L.S.D. jitter. An optional power failure detection circuit is provided. At power up the chip will read normally for about 10 sec—actual time determined by an external capacitor—then it will store the last reading and flash the display. In this condition the chip will continue to make measurements and operate the control outputs normally. Operating the reset button will restore the normal display. If there is a short duration power failure the circuit will ignore it, if it lasts longer than 10 sec the alarm condition will occur.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



HIGH READING OPTION

For normal operation Pin 39 drives segments A3, B3, D3 and G3 in parallel. Pin 38 drives segment F3, Pin 37 drives segments E3 and Pin 36 drives segment C3.

For 20.0 to 49.9 range Pin 39 drives segment C3. Pin 38 drives segment E3, Pin 37 drives segment A3 and D3 and Pin 36 drives segment F3. Segments B3, G3 are connected to Pin 28 (Decimal Point).

CONSUMER

PIN FUNCTIONS

Pin No.	Name	Description
1	V_{SS}	Negative Supply (0_V)
2	Hysteresis Strobe Output	Common output for Hysteresis and LED select switches
3	Tens Strobe Output	Common output for Tens and Sign select switches
4	Units Strobe Output	Common output for Units select switches
5	Tenths Strobe Output	Common output for Tenths select switches
6	Set Point 2^0 Input	Common input for 2^0 bit
7	Set Point 2^1 Input (Control & Hysteresis)	Common input for 2^1 bit
8	Set Point 2^2 Input (Control & Hysteresis)	Common input for 2^2 bit
9	Set Point 2^3 Input (Control & Hysteresis)	Common input for 2^3 bit
10	Timer Input/Reset Timer Input	Connected to a capacitor to V_{SS} and switch to V_{CC} for power failure detection and reset. The nominal delay time is 10 sec when a 10μF capacitor is used
11	Clock Output 2	Connected to frequency determining network
12	Clock Output 1	See Figure 1
13	Clock Input	
14	Comparator Input 2	Connected to nominal $V_{CC}/2$ reference
15	Comparator Input 1	Connect to thermistor network
16	Ramp Input	Connect to Resistor to V_{CC} and Capacitor to V_{SS}
17	Control Output 2 (HIGH)	Open drain output which turns ON when reading is greater than (Set Point + Hysteresis). Turns OFF again when reading equals Set Point
18	Control Output 1 (LOW)	Open drain output which turns OFF when reading equals (Set Point—Hysteresis)
19	V_{CC}	Positive supply (9V nom.)
20	LCD Backplate Output	Square wave output to drive backplate of LCD display
21	Segment A1 Output	
22	Segment B1 Output	
23	Segment C1 Output	
24	Segment D1 Output	
25	Segment E1 Output	
26	Segment F1 Output	
27	Segment G1 Output	
28	Decimal Point Output	
29	Segment A2 Output	Tens, Units and Tenths 7 segment outputs
30	Segment B2 Output	In LED mode these are open drain outputs
31	Segment C2 Output	designed to sink 12.5mA per segment
32	Segment D2 Output	In LCD mode these are push pull outputs
33	Segment E2 Output	
34	Segment F2 Output	
35	Segment G2 Output	
36	Segment C3 Output	
37	Segment E3 Output	
38	Segment F3 Output	
39	Segment A3, B3, D3, G,	
40	Sign Output	On for a negative reading

CLOCK OSCILLATOR

The Clock oscillator is designed to operate with an R-C network, an LC network or a Ceramic resonator. The choice will depend on the system Temperature and Voltage stability requirements.

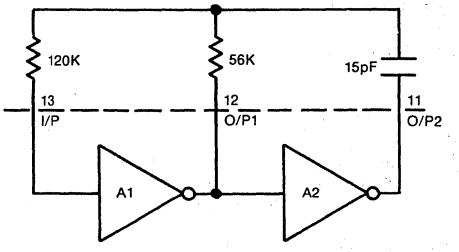
The thermometer reading is directly proportional to the clock frequency.

CONSUMER

CHIP INTERFACE CIRCUITS

The input configuration on the Set Point inputs is shown in Fig. 2.

The circuit for the display drive is shown in Fig. 3. and shows the internal switching required to drive LED or LCD displays.



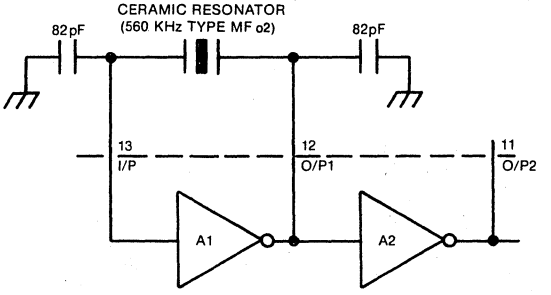


Fig. 1 TYPICAL OSCILLATOR CONFIGURATIONS

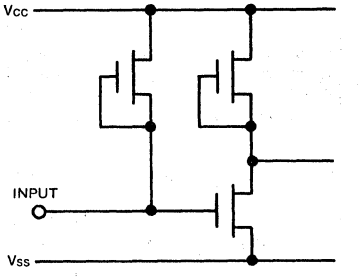


Fig. 2 SET POINTS INPUTS

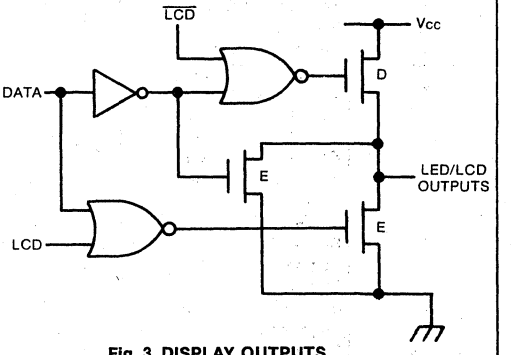


Fig. 3 DISPLAY OUTPUTS

CONSUMER

ANALOG CIRCUITRY

The Temperature measuring circuit consists of a bridge network connected across the power supplies.

One side of the bridge (which is connected to comparator 2 input) consists of two equal value fixed resistors. These set up a reference potential of approximately $V_{CC}/2$ (4.5V). The other side of the bridge (which is connected to Comparator 1 Input) consists of a Thermistor and a series resistor connected to V_{CC} and a resistor connected to V_{SS}. A suitable thermistor is Mullard Type 640-90003.

The bridge is arranged to balance at 0°. As the temperature varies, the voltage at Comparator 2 input goes from approximately 3V (at −39.9°) to 6V (at +39.9°) in a non linear fashion.

A non linear ramp is generated by R and C and the time taken for the ramp voltage to change from one comparator input voltage to the other gives the temperature. R is varied to adjust the FSD. The non linearity of the ramp to a large extent compensates for the non linearity of the thermistor network.

For use with linear sensors or as a digital voltmeter the Resistor would be replaced by a current source.

Reading will be negative if comparator input 1 voltage < comparator input 2.

Typical circuit diagrams showing the AY-3-1270 displaying temperature in a freezer are shown in Fig. 9 (with LED display) and Fig. 10 (with LCD display).

SET POINT PROGRAMMING

To set the control temperature, diodes are inserted in the program matrix with the cathodes connected to the strobe lines on pins 2, 3, 4. The code is B. C. D., and any temperature within the operating range can be selected by a suitable combination of diodes. For a negative temperature set point, a diode is inserted between pins 8 and 3.

When an L.E.D. display is being used the diode between pins 9 and 2 is inserted, which inhibits the L.C.D. backplate waveform. This waveform is shown in Fig. 4.

A timing waveform for the strobe lines is shown in Fig. 5.

2^0 (pin 6)	2^1 (pin 7)	2^2 (pin 8)	2^3 (pin 9)	
0.1	0.2	0.4	0.8	Tenths (pin 5)
1	2	4	8	Units (pin 4)
10	20	Minus	Do not Use	Tens (pin 3)
A	B	C	LED Display	Hysteresis (pin 2)

To set the hysteresis level, that is the temperature difference above and below the "set point" at which the control outputs operate, diodes are inserted in locations A, B, and C according to the following table. Fig. 6 shows the control output characteristics with temperature.

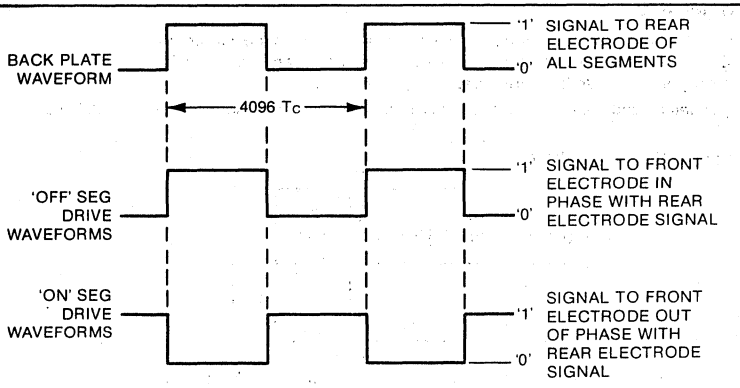
	Hysteresis	A	B	C
	0			
	±0.2	*		
	±0.4		*	
	±0.8	*	*	
Note 2	±2	*		*
Note 2	±4		*	*
Note 2	±8	*	*	*

*indicates presence of a programming diode

NOTES:

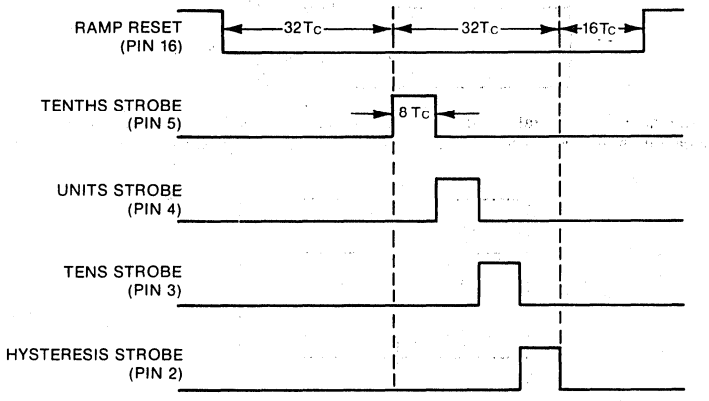
1. Set points must consist of valid BCD codes or incorrect readings will occur.
2. For hysteresis settings ±2, ±4 and ±8 the L.S.D. of the reading is ignored.
3. The ½° LSD Control and Display hysteresis should also be taken into account.
4. When in the "High Reading" mode it is necessary to program a set point 10°C lower than that required.
   E.g. To select 44°C diodes are inserted in the matrix between pins 6, 3/7, 3/8, 4.

CONSUMER



T_C = CLOCK PERIOD

Fig. 4 LCD DRIVE WAVEFORM



T_C IS CLOCK PERIOD

REPETITION RATE OF ABOVE CYCLES IS TWICE MEASUREMENT CYCLE

Fig. 5 STROBE OUTPUT TIMING

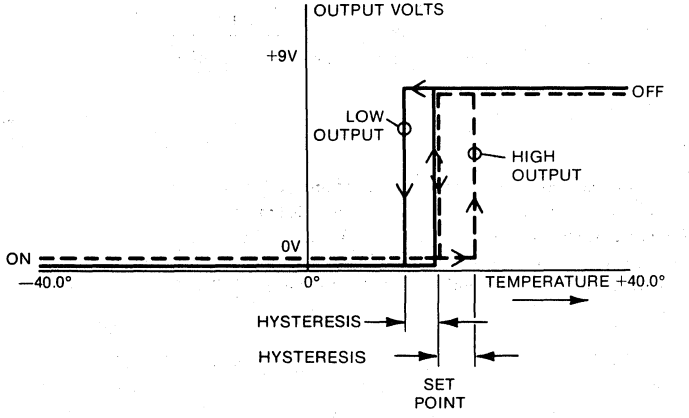


Fig. 6 SET POINT HYSTERESIS

CONSUMER

MEASUREMENT AND READ CYCLE

In order to compensate for offsets in the comparators, a digital autozero cycle operates on every other measurement cycle. Fig. 7 shows the internal ramp and comparator waveform.

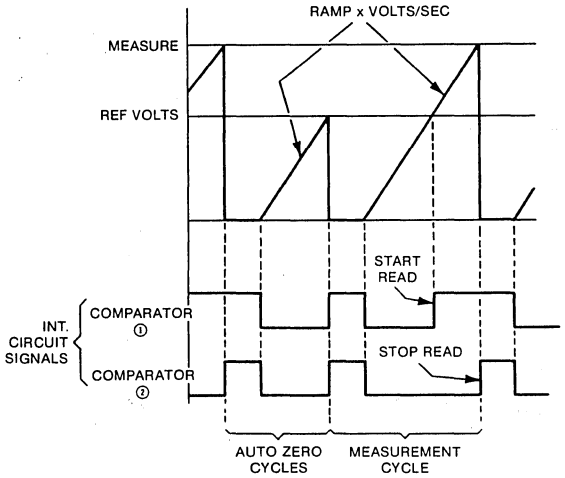


Fig. 7 TYPICAL MEASUREMENT/READ CYCLE

SYSTEM DIAGRAM

Fig. 8 shows a block schematic of the AY-3-1270 circuit.

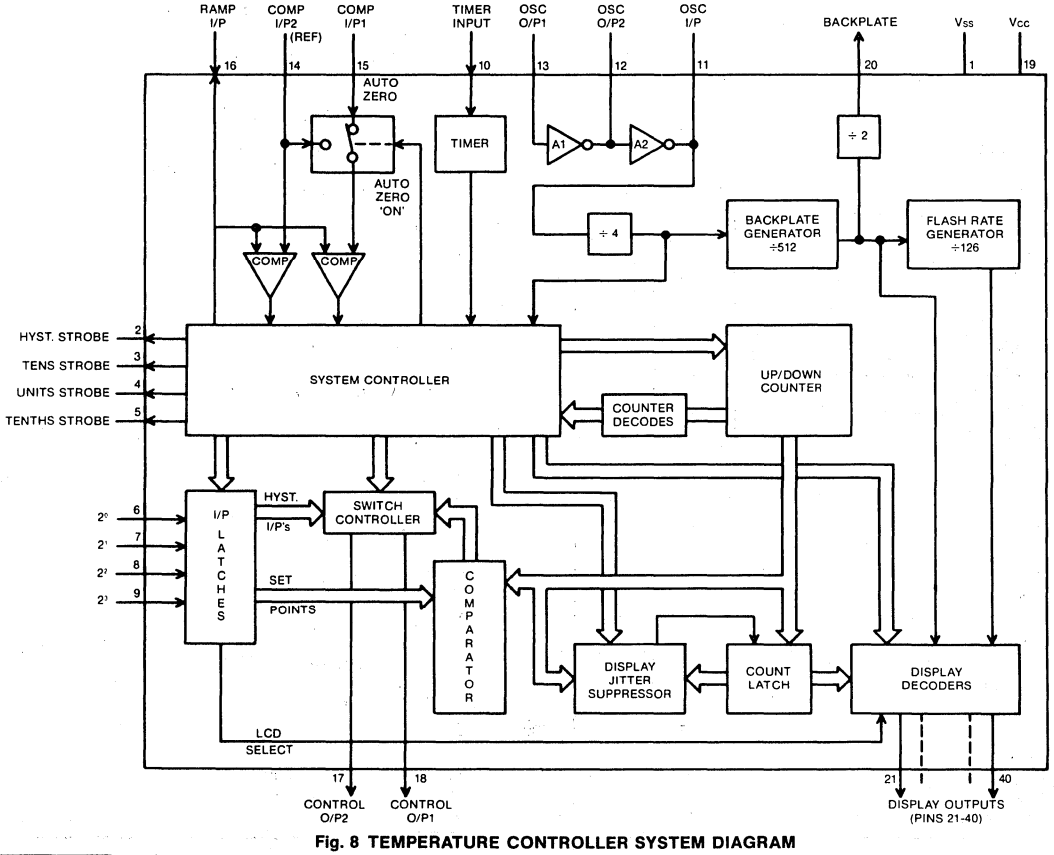


Fig. 8 TEMPERATURE CONTROLLER SYSTEM DIAGRAM

CONSUMER

ELECTRICAL CHARACTERISTICS

Maximum Ratings

Voltage on any pin with respect to V_{SS} ..... −0.3 to +18
Storage temperature range ..... −65°C to +150°C
Ambient operating temperature range ..... −25°C to +70°C
Maximum power dissipation at 70°C 800mW
Maximum segment output current (LED mode) 20mA
Maximum switch output current 30mA
Maximum total output current 250mA

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

V_{SS} = 0V
V_{CC} = (7.2V to 10.8V)
T_{amb} = −25°C to +70°C, positive logic convention

Characteristics	Min	Typ	Max	Units	Conditions
Segment, DP, Sign Outputs					
LED mode					
On resistance	—	—	160	Ω	V_{out} = +2V I_{sink} = 12.5mA
On resistance E3	—	—	80	Ω	V_{out} = +2V I_{sink} = 25mA
On resistance DP	—	—	53	Ω	V_{out} = +2V I_{sink} = 37.5mA
On resistance (A3, B3, D3, G3)	—	—	40	Ω	V_{out} = +2V I_{sink} = 50mA
Off leakage	—	—	10	μA	V_{out} = V_{CC}
Segment, DP, Sign Outputs					
LCD mode					
Logic '0' output	—	—	400	mV	Load = 50pF + 1 MOhm to
Logic '1' output	V_{CC}−50	—	—	mV	Backplate output (E3 load = 100pF + 500K DP load = 150pF + 330K A3, B3, D3, G3 load = 200pF + 250K)
Rise time	—	—	—	—	Under specified load conditions
Fall time	—	—	—	—	Under specified load conditions
Frequency	—	137	—	Hz	Clock (560kHz) ÷ 4096
LCD Backplate Output					
Logic '0' output	—	—	400	mV	Load = 1000pF and 50K
Logic '1' output	V_{CC}−50	—	—	mV	
Output frequency	—	137	—	Hz	Clock (560kHz) ÷ 4096
Rise time	—	—	—	—	Under specified load conditions
Fall time	—	—	—	—	Under specified load conditions
Backplate output to Segment output delay	—	—	—	—	
to Logic '1'	—	—	—	—	
to Logic '0'	—	—	—	—	
Control Outputs					
On resistance	—	—	110	Ω	V_{out} = +2V I_{sink} = 18mA
Off leakage	—	—	10	μA	V_{out} = +15 volts
Strobe Outputs					
On resistance	—	—	400	Ω	V_{out} = +1V I_{sink} = 2.5mA
Off leakage	—	—	10	μA	V_{out} = V_{CC}
Frequency	—	—	—	—	2 x reading rate
Set Point Inputs					
Logic '0' level	V_{SS}	—	2	V	
Logic '1' level	6	—	V_{CC}	V	
Pull up resistance	20	—	100	KΩ	to V_{CC} V_{in} = V_{SS}
Comparator Inputs					
Leakage current	—	—	1	μA	V_{in} = V_{CC}
Resolution	25	—	—	mV	
Common Mode Range	V_{SS}	—	V_{CC}−3V	V	
Ramp Input					
Discharge resistance	—	—	100	Ω	to V_{SS} see note 1
Leakage current	—	—	1	μA	V_{in} = V_{CC}
Timer Input					
Flash Threshold	1.25	—	2.00	V	
Reset Threshold	2	—	5	V	
Pull up resistance	650	—	—	KΩ	to V_{CC} (V_{in} = V_{SS})
Pull down resistance	60	—	—	KΩ	to V_{SS} (V_{in} = V_{CC})
Open circuit input voltage	2	—	3.5	V	

CONSUMER

Characteristics	Min.	Typ.	Max.	Units	Conditions
Clock					
Frequency	300	—	560	KHz	
Gain to output 1 (A1)	12	—	—	—	small signal open loop
Gain to output 2 (A2)	12	—	—	—	AC gain, F = 560kHz
Output impedance	—	—	10	KΩ	F = 560kHz
Input capacitance	—	—	12	pF	
Count frequency	—	12.5	—	kHz	Clock (560kHz) ÷ 32 see note 2
Flash rate, Overrange and Power Fail	—	2	—	Hz	Clock (560kHz) ÷ 158048
Supply current	—	40	60	mA	

NOTES:

1. Minimum resistance to V_{CC} = 1KΩ Maximum capacitance to V_{SS} = 10μf.
2. Reading is measurement time divided by Count Frequency period. Measurement time depends on both the voltage difference at the Comparator inputs and ramp speed at pin 16.

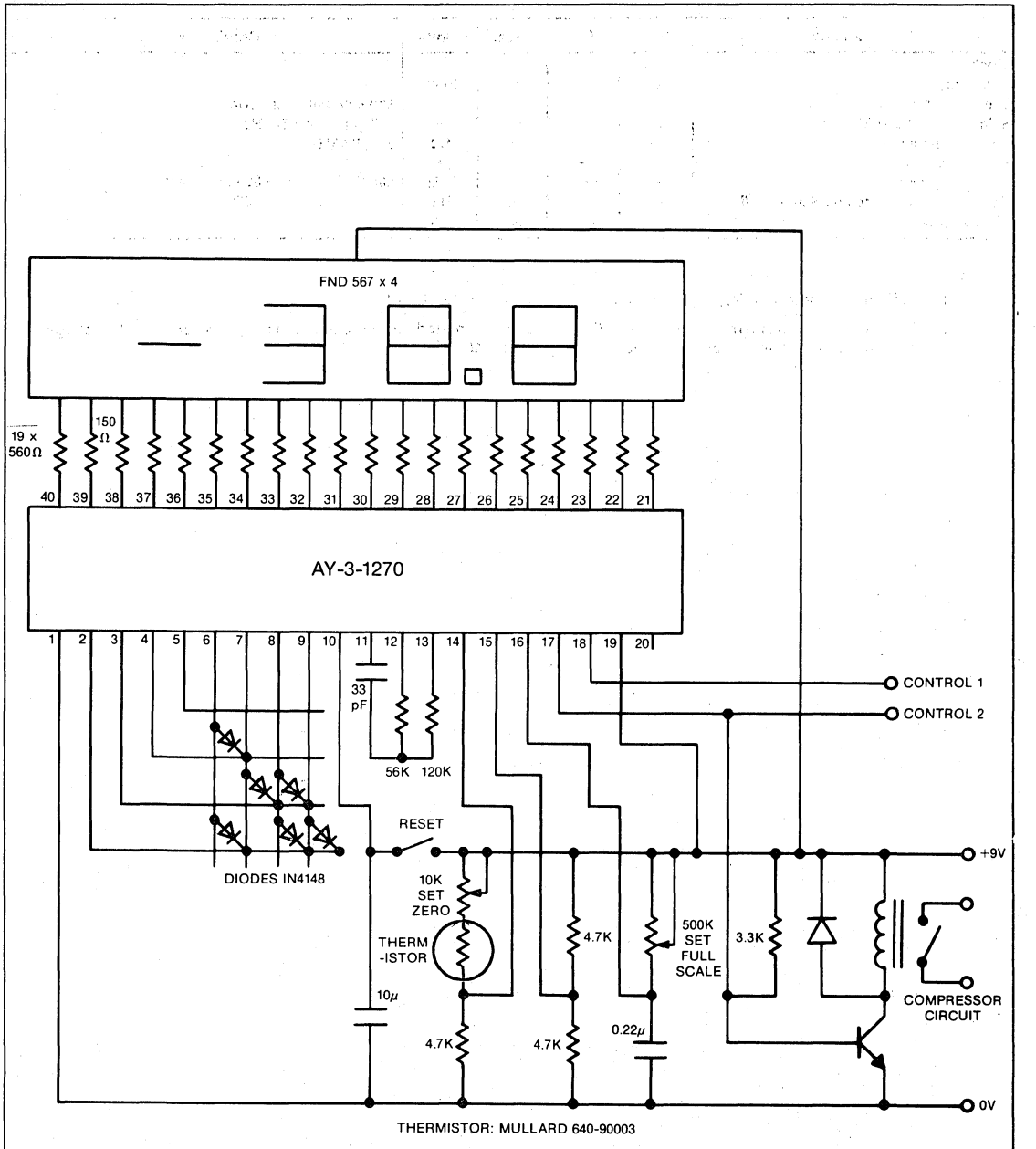


Fig. 9 THERMOMETER WITH LEAD DISPLAY

CONSUMER

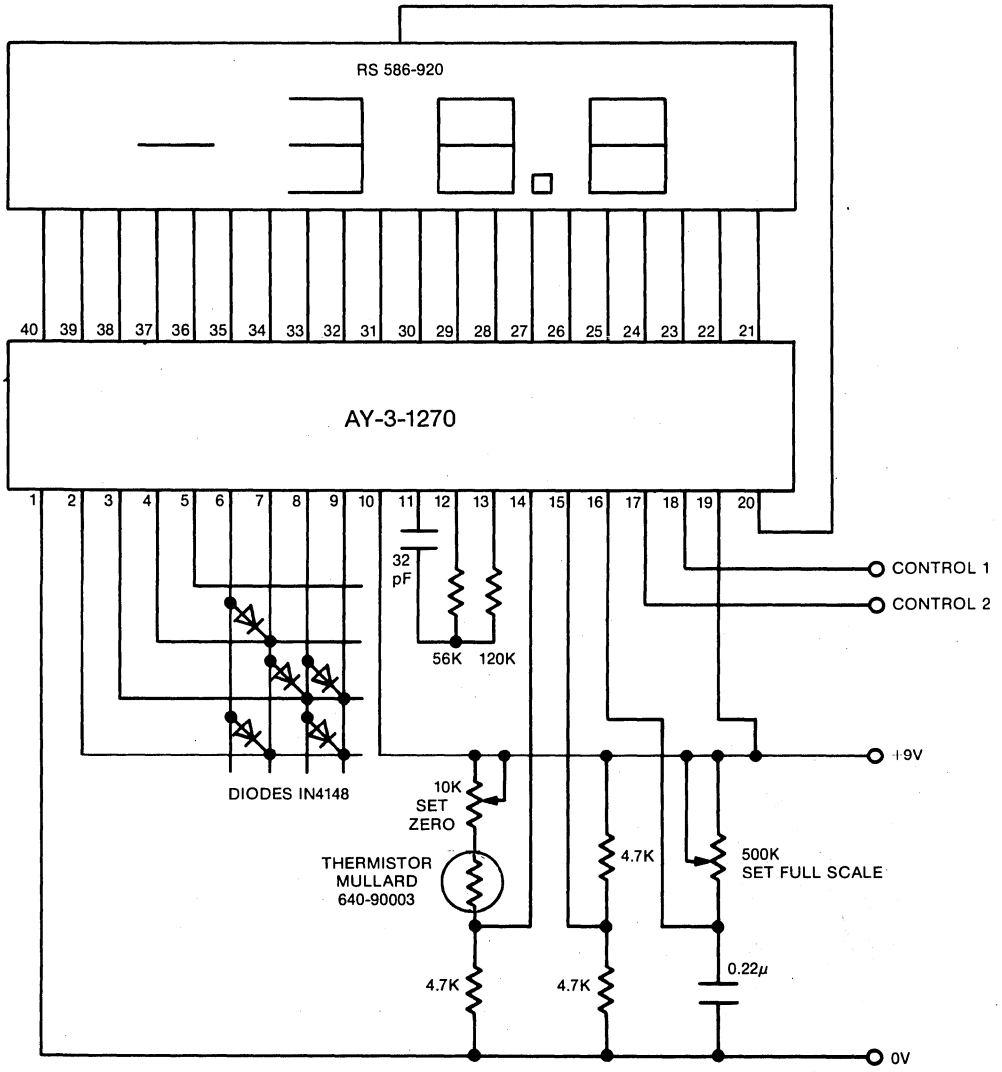


Fig. 10 THERMOMETER WITH LIQUID CRYSTAL DISPLAY

CONSUMER

GENERAL INSTRUMENT

CONSUMER

Counters/DVMs

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
3½ DIGIT DVM	DVM logic utilizing dual ramp integration.	AY-5-3507	8-94
3¾ DIGIT DVM	DVM logic utilizing single ramp integration.	AY-5-3500	8-99
4 DIGIT COUNTER/ DISPLAY	Counts, stores, and decodes 4 decades to 7-segment outputs.	AY-5-4007	8-103
		AY-5-4007A	8-103
		AY-5-4007D	8-103
FLUORESCENT DISPLAY DRIVER	Direct drive to fluorescent display stores and siplay with internal max clock.	AY-5-4121	8-109
		AY-5-4221	8-109

3½ Digit DVM

FEATURES

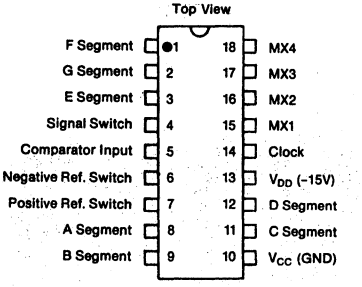
- 3½ Decade Display (±1999 max. reading)
- Automatic Polarity Detection
- Overrange Indication
- Direct LED 7-Segment Drive
- Up to 5 readings per second

DESCRIPTION

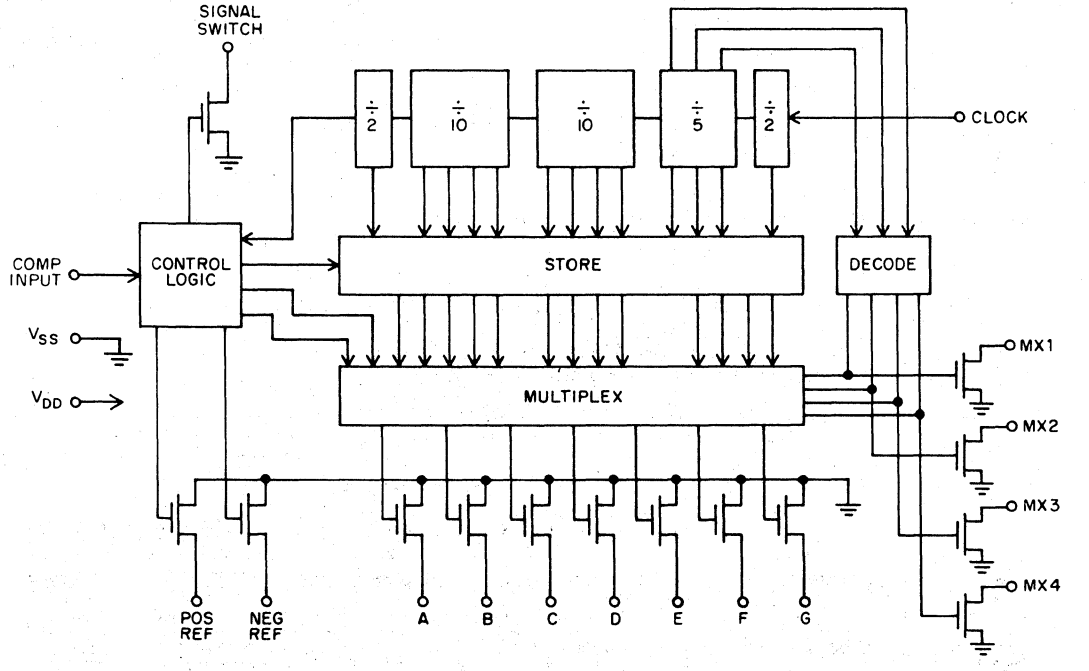
The AY-5-3507 is an MOS LSI circuit containing all the logic necessary for a 3½ Decade Digital Voltmeter utilizing Dual Ramp integration. Automatic polarity detection is incorporated as is automatic overrange indication. The outputs are mutiplexed onto a 7-segment bus allowing easy interface to LED and similar displays.

PIN CONFIGURATION

18 LEAD DUAL IN LINE



BLOCK DIAGRAM



CONSUMER

PIN FUNCTIONS

Name	Functions
COMPARATOR INPUT	A logic '0' level corresponds to a negative input signal. A logic '1' level corresponds to a positive input signal.
CLOCK INPUT	This signal should be supplied from an external oscillator giving a square wave signal.
REFERENCE SWITCH OUTPUTS	These outputs drive analog switches which connect the Reference Voltages to the Integrator. A logic '0' at the Comparator Input will be followed by a logic '1' at the Positive Reference Switch Output. A logic '1' at the Comparator Input will be followed by a logic '1' at the Negative Reference Switch Output.
SIGNAL SWITCH OUTPUT	This output will be at logic '1' during the time that the signal is connected to the integrator.
DISPLAY MULTIPLEX OUTPUTS	Each output will be at logic '1' for 2 clock periods to display (see Fig. 4). The outputs selected will be as follows:— MX1 0/1, ±, Over-range MX3 Decade 2 (10^1) MX2 Decade 3 (10^2) MX4 Decade 1 (10^0)
AY-5-3507 SEGMENT OUTPUTS	The outputs of the 3 decade counters are presented sequentially on the outputs A, B, C, D, E, F, G. In the first multiplex position 1 is indicated by segments B and C,—is indicated by segment G, overrange by the flashing of segments A and D. 0, + and underrange are not indicated.

OPERATION

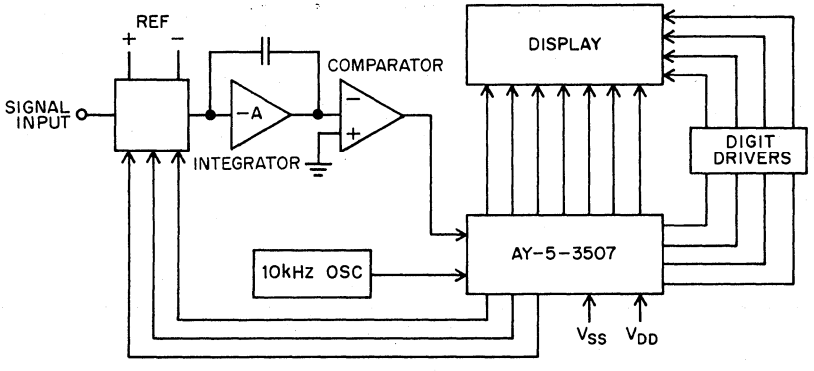
The operation of the circuit is as follows.

Initially the signal, and reference outputs are in the logic '0' state. The counter counts continuously and at the 1999 to 0000 transition a ÷2 is toggled driving the signal switch output to logic '1' turning on the signal switch. The integrator generates a ramp, the amplitude and polarity of which depend on the amplitude and polarity of the input signal. After a further 2000 clock pulses the ÷2 is toggled again. This stores the state of the comparator output in a D type flip flop (this signal represents the sign of the input signal). The appropriate reference switch is then energized to cause the integrator output to ramp back to zero. When the comparator output subsequently changes state the reference is switched off and the number in the counter is transferred to the store together with polarity information.

Should the input signal be so large that zero is not reached during one counter cycle, an overrange flip flop will be set and will remain set until the next 1999 to 0000 transition of the counter. During overrange the main display will be set to 0000 and the overrange indicator will flash.

To minimize pin requirements, a time shared output is used. The display store output (including ±, 0/1 and overrange) is gated sequentially, a decade at a time, onto a common 7 line output bus.

3½ DECADE DIGITAL VOLTMETER



CONSUMER

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Maximum voltage between any pin and V_{SS} pin . . . . +0.3 to −20 V
Operating temperature range . . . . . 0°C to +70°C
Storage temperature range. . . . . −65°C to +150°C
Maximum power dissipation . . . . 500mW (total), 50mW (per output)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = GND
V_{DD} = −12 to −18V
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Clock & Comparator Inputs					
Logic '0' Level	-6	—	-18	V.	
Logic '1' Level	+0.3	—	-1	V	
Input Leakage	—	—	10	μA	V_{IN} = -18V, T_A = +25°C
Display Multiplex Outputs (Note 1)					
Logic '1' sink current	1.2	2	3.2	mA	V_{OUT} = -2V, T_A = +25°C, V_{GG} = -12V
Logic '0' leakage current	—	—	10	μA	V_{OUT} = -18V, T_A = +25°C
Switch Outputs (Note 1)					
Logic '1' sink current	0.5	0.8	1.25	mA	V_{OUT} = -2V, T_A = +25°C, V_{GG} = -12V
Logic '0' leakage current	—	—	10	μA	V_{OUT} = -18V, T_A = +25°C
Segment Outputs (Note 1)					
Logic '1' sink current	4.25	7	11	mA	V_{OUT} = -2V, T_A = +25°C, V_{GG} = -12V
Logic '0' leakage current	—	—	10	μA	V_{OUT} = -18V, T_A = +25°C
Supply Current	—	1.5	2.2	mA	V_{DD} = -12V, T_A = +25°C
	—	3.6	5.25	mA	V_{DD} = -18V, T_A = +25°C
AC CHARACTERISTICS					
Clock & Comparator Inputs					
Input Capacitance	—	—	10	pF	V_{IN} = 0V, f = 1MHz
Clock Frequency	DC	—	20	kHz	V_{DD} = -18V
	DC	—	10	kHz	V_{DD} = -12V
Clock Pulse Width	10	—	—	μs	Note 2
Display Multiplex Outputs					
Propagation delay	—	—	4	μs	from Clock positive edge
Segment Outputs					
Propagation delay	—	—	10	μs	from Multiplex output positive edge

**Typical values are at +25°C and nominal voltages.

NOTE:
1. All outputs are single-ended ("open-drain"). External pull-down resistors are required.
2. A square waveform is preferred.

CONSUMER

TIMING DIAGRAMS

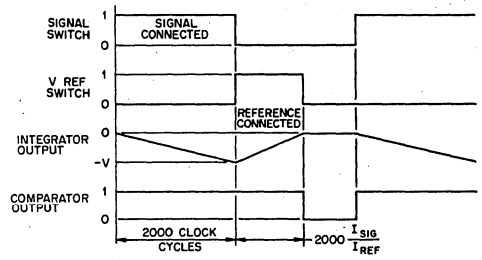


Fig.1

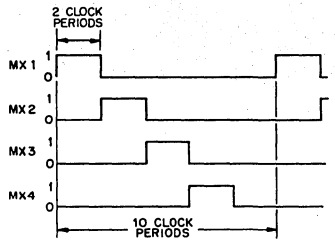
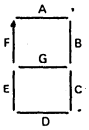


Fig.2 MULTIPLEX WAVEFORMS

TRUTH TABLES

7 SEGMENT OUTPUT TRUTH TABLE (MX2-MX4)

	Segment Output						
Digit	A	B	C	D	E	F	G
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1



MX1 OUTPUT TRUTH TABLE

	Segment Output							
Display	A	B	C	D	E	F	G	
0	0	0	0	0	0	0	0	
1	0	1	1	0	0	0	0	
+	0	0	0	0	0	0	0	
−	0	0	0	0	0	0	1	
UR	0	0	0	0	0	0	0	
OR	1	0	0	1	0	0	0	Flashed

ANALOG CIRCUIT DIAGRAMS

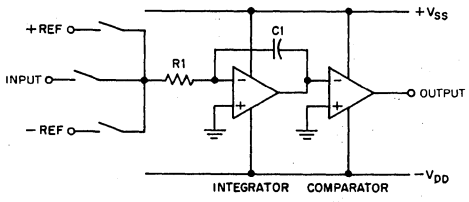


Fig.1 BASIC ANALOG CIRCUIT

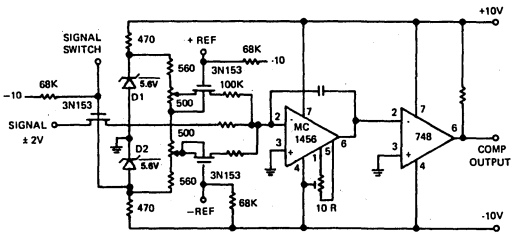


Fig.2 TYPICAL ANALOG CIRCUITRY

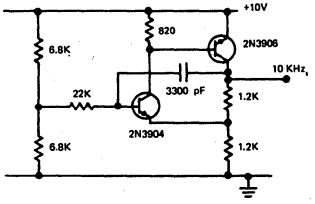
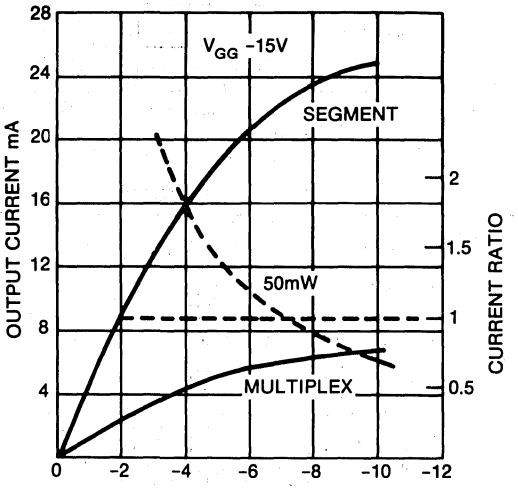


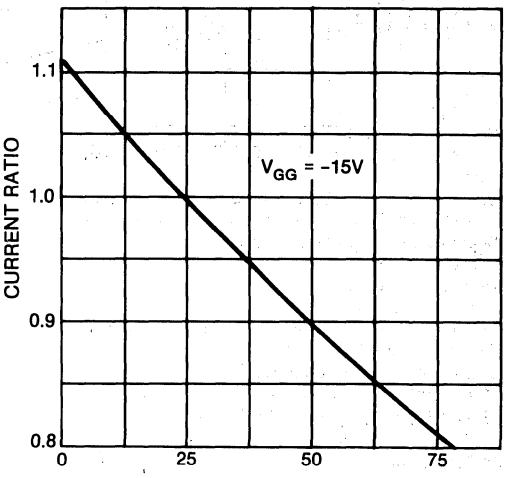
Fig.4 CLOCK OSCILLATOR

CONSUMER

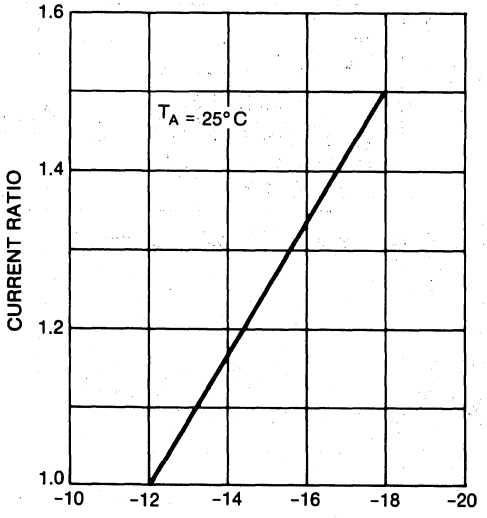
TYPICAL CHARACTERISTIC CURVES



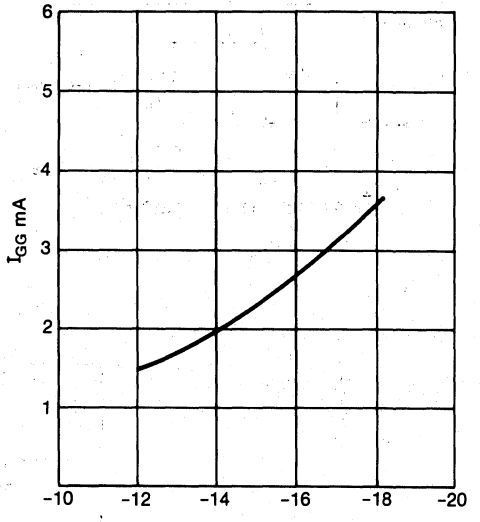
V_{OUT} Volts
OUTPUT CURRENT vs. OUTPUT VOLTAGE



TEMPERATURE °C
NORMALIZED OUTPUT CURRENT vs.
TEMPERATURE



V_{GG} Volts
NORMALIZED OUTPUT CURRENT
vs. SUPPLY VOLTAGE



V_{GG} Volts
SUPPLY CURRENT vs. SUPPLY VOLTAGE

CONSUMER

3¾ Digit DVM

FEATURES

- Single Ramp Integration
- Three measurement ranges 999, 1999, 2999
- Dual Polarity
- Reading Rate up to 70 measurements per second
- Overrange indication, 2 most significant digits flash
- Separate overrange output available on 1999 and 2999 ranges
- Underrange output
- Operating voltage 13V to 17V
- Power consumption 30mW typical
- 7 segment or BCD output
- Controllable display brightness
- Load enable freezes display
- Hold input halts measurement

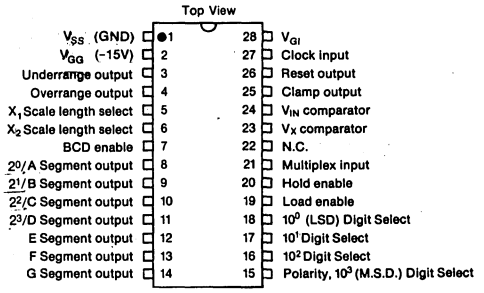
DESCRIPTION

The AY-5-3500 is a single ramp, dual polarity digital voltmeter chip having a selectable scale length of 999, 1999, 2999.

It is manufactured using the MTNS low voltage p-channel nitride technology. Low power dissipation achieved by the use of 4-phase logic with an "on chip" clock generator.

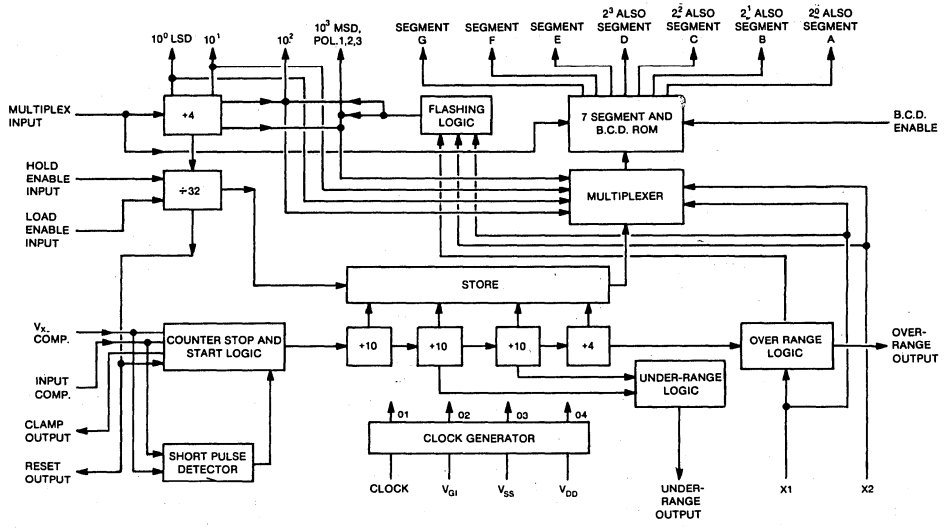
PIN CONFIGURATION

28 LEAD DUAL IN LINE



See next page for details of Pin Functions.

BLOCK DIAGRAM



CONSUMER

PIN FUNCTIONS

OVERRANGE OUTPUT
This output goes to logic '1' as soon as an overrange count has been detected. It returns as logic '0' at the end of the measurement cycle.

It operates at 2000 on the 1999 range
It operates at 3000 on the 2999 range

MEASUREMENT CYCLE
The measurement cycle lasts 128 Multiplex clock periods. Data is transferred to the display store from clocks 113 to 120. The counters are reset from 121 to 128.

UNDERRANGE OUTPUT
The underrange output is a pulse from clock 105 to 112 if the reading is less than 259.

SCALE LENGTH SELECT

X1	X2	Scale
0	1	999
1	0	1999
0	0	2999

OVERRANGING

Range	Count	Display	Overrange Output
999	0XXX	XXX	0
	1XXX	1XXX } First	0
	2XXX	XXX } Two Digits	0
	3XXX	3XXX } Flash	0
1999	0XXX	XXX	0
	1XXX	1XXX	0
	2XXX	1XXX } First Two	1
	3XXX	3XXX } Digits Flash	1
2999	0XXX	XXX	0
	1XXX	1XXX	0
	2XXX	2XXX	0
	3XXX	3XXX } First Two Digits Flash	1

CLAMP OUTPUT
The clamp output goes to a logic '1' after 3 Counter clock periods following the input from the V_{IN} comparator. This output is used to switch off the V_{IN} comparator thus reducing the average input current by a factor of approx. 70. Fig.2 shows input waveforms without use of clamp output and Fig.3 shows waveforms with use of clamp output and timing for Clamp output.

BCD ENABLE
Logic '0' = BCD
Logic '1' = 7 segment

BCD OUTPUTS
The BCD outputs appear on the 7 segment output lines (Logic (1) is the Active Level); E, F, G are blanked to logic '0'
$A = 2^0$
$B = 2^1$
$C = 2^2$
$D = 2^3$

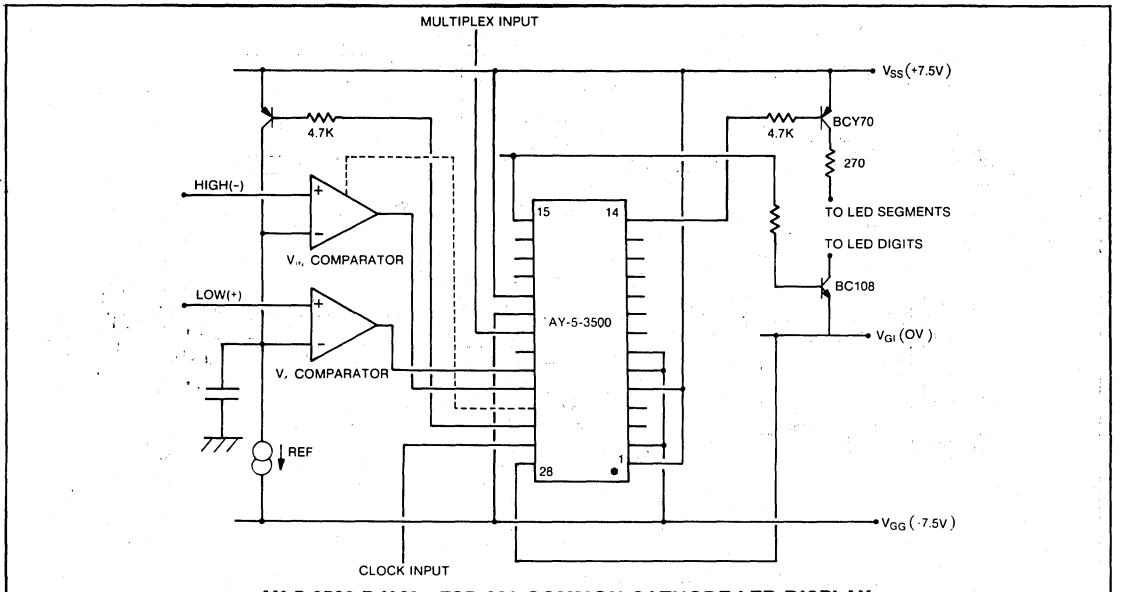
LOAD ENABLE
Logic '0' = Normal Operation
Logic '1' = Freeze Display

HOLD ENABLE
Logic '0' = Halts measurement cycle in reset state
Logic '1' = Normal Operation

RESET OUTPUT
Logic '1' resets ramp generator

NEGATIVE SIGN OUTPUT
Displayed on segment G output on 999 and 1999 ranges. Inhibited on 2999 range.

OPERATION
A linear stable ramp is generated and compared to zero volts and the input voltage in two comparators. The time between the changing of the comparator outputs is proportional to the magnitude of the input voltage, and the sequence of switching gives the polarity.



AY-5-3500 D.V.M. -FSD 999 COMMON CATHODE LED DISPLAY

CONSUMER

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin . . . . −20V to +0.3V
Storage temperature range. . . . . −65°C to +150°C
Ambient operating temperature range . . . . . 0°C to +70°C

*Exceeding these ratngs could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{GG} = −15 ±2V
V_{GI} = V_{GG}/2 (Note 8)
Temperature (T_A) = 0° C to +70° C

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input					
Frequency	—	200	—	kHz	
Pulse width	1.5	—	—	µs	At logic '0' and '1' levels
Rise and Fall time	—	—	1	µs	
Logic '0' level	+0.3	—	−1	V	
Logic '1' level	−9	—	−17	V	
Multiplex Input					
Frequency	0.5	1.5	10	kHz	(See Note 1)
Pulse width	15	—	—	µs	At logic '0' and '1' levels (Note 2)
Logic '0' level	+0.3	—	−1	V	
Logic '1' level	−4	—	−17	V	
Control Inputs					
Logic '0' level	+0.3	—	−1	V	
Logic '1' level	−4	—	−17	V	
Leakage (all inputs)	—	—	1	µA	V_{IN} = −10V at 25°C
Segment,Overrange, Underrange Outputs					
Logic '0'	—	—	30	kΩ	V_{OUT} = −0.3V (Note 3)
Logic '1'	—	—	2	kΩ	V_{OUT} = V_{GI} +1V (Note 4)
Digit Select Outputs					
Logic '0'	—	—	1	kΩ	V_{OUT} = −1V (Note 5)
Logic '1'	—	—	15	kΩ	V_{OUT} = V_{GI} +0.3V (Note 6)
Clamp and Reset Outputs					
Logic '0'	—	—	20	kΩ	V_{OUT} = −0.2V (Note 3)
Logic '1'	—	—	5	kΩ	V_{OUT} = V_{GI} + 1V (Note 7)
Supply Current	—	2	—	mA	V_{GG} = −15V excluding output current

**Typical values are at +25° C and nominal voltages.

NOTES
1. This gives a reading rate of typically 12 per second.
   On the 2999 range, the maximum Multiplex clock frequency must be less than the Counter clock frequency divided by 64.
   On the 1999 range, the maximum Multiplex clock frequency must be less than the Counter clock frequency divided by 42.
   On the 999 range the maximum Multiplex clock frequency must be less than the Counter clock frequency divided by 21.
2. In 7 segment mode, outputs are energized when Multiplex input is at Logic '1'.
   The display brilliance is therefore controlled by the input Mark-Space ratio.
3. Output device connected to V_{SS}.
4. Output device connected to V_{GI} segment energized.
5. Output device connected to V_{SS} digit selected.
6. Output device connected to V_{GI}.
7. Output device connected to V_{GI} Reset condition.
8. V_{GI} is only applied to the output drivers, thus its absolute value is not critical.

TIMING DIAGRAMS

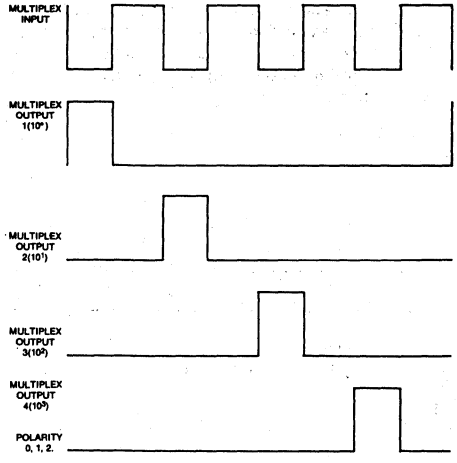


Fig.1 MULTIPLEX INPUT AND OUTPUT

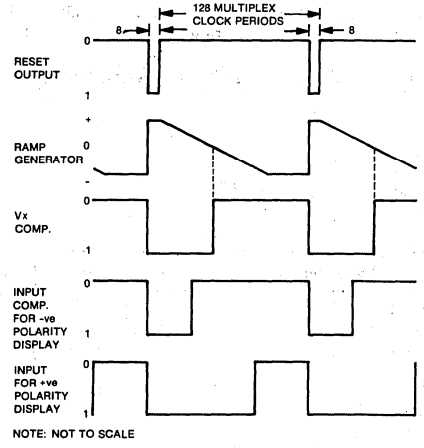


Fig.2 INPUT AND RESET OUTPUT

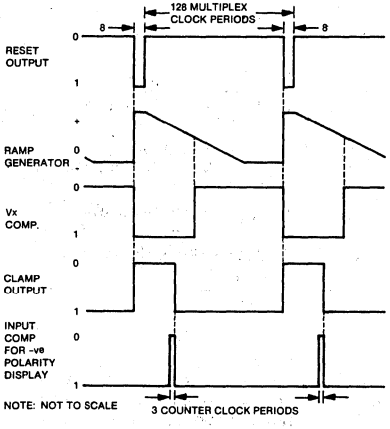
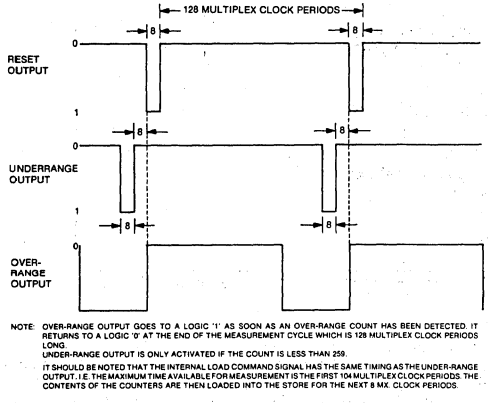


Fig.3 INPUT AND RESET OUTPUT TIMING DIAGRAM SHOWING CLAMP OUTPUT



NOTE: OVER-RANGE OUTPUT GOES TO A LOGIC '1' AS SOON AS AN OVER-RANGE COUNT HAS BEEN DETECTED. IT RETURNS TO A LOGIC '0' AT THE END OF THE MEASUREMENT CYCLE WHICH IS 128 MULTIPLEX CLOCK PERIODS LONG.
UNDER-RANGE OUTPUT IS ONLY ACTIVATED IF THE COUNT IS LESS THAN 259.
IT SHOULD BE NOTED THAT THE INTERNAL LOAD COMMAND SIGNAL HAS THE SAME TIMING AS THE UNDER-RANGE OUTPUT, I.E. THE MAXIMUM TIME AVAILABLE FOR MEASUREMENT IS THE FIRST 104 MULTIPLEX CLOCK PERIODS. THE CONTENTS OF THE COUNTERS ARE THEN LOADED INTO THE STORE FOR THE NEXT 8 MX. CLOCK PERIODS.

Fig.4 UNDER-RANGE AND OVER-RANGE OUTPUT

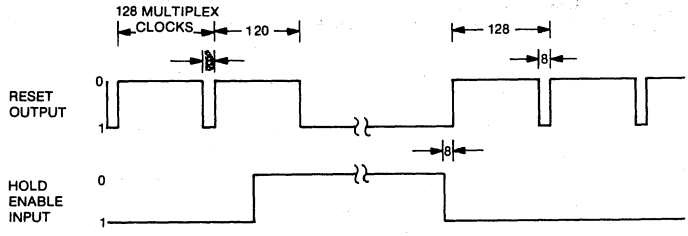


Fig.5 RESET OUTPUT WITH RESPECT TO HOLD ENABLE INPUT

CONSUMER

Four Digit Counter / Display Drivers

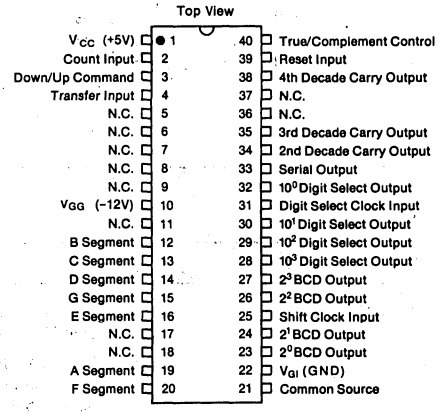
FEATURES

- Minimum interface required to drive most common types of LED, fluorescent, seven segment displays
- Large output current capability on seven segment outputs, typically 25mA with 1V drop
- Fully synchronous up/down counting operation
- Look ahead carry for error free outputs when reversing count direction
- Internal oscillator needing no external components for operating the digit select counter
- Four digit select outputs with inversion control for display driving flexibility
- Multiplexed BCD outputs and serial output from storage register is available
- TTL/DTL compatible on inputs and outputs
- Blanking action of Reset Input
- Counting rate up to 600 kHz

PIN CONFIGURATION

40 LEAD DUAL IN LINE
AY-5-4007A

Top View



DESCRIPTION

The Four Digit Counter Display Driver is an LSI subsystem designed for application in counting display systems such as frequency counters, digital voltmeters, digital timers, event counters using 7 segment numeric displays. It contains a 4 decade up/down synchronous BCD counter, a storage register, multiplexing circuits, internal oscillator for digit selection and 7 segment decoder to count and display up to 9999.

Built-in control circuits provide flexibility of use with a minimum of external components.

The device is constructed on a single monolithic chip using MTNS P-channel enhancement mode transistors.

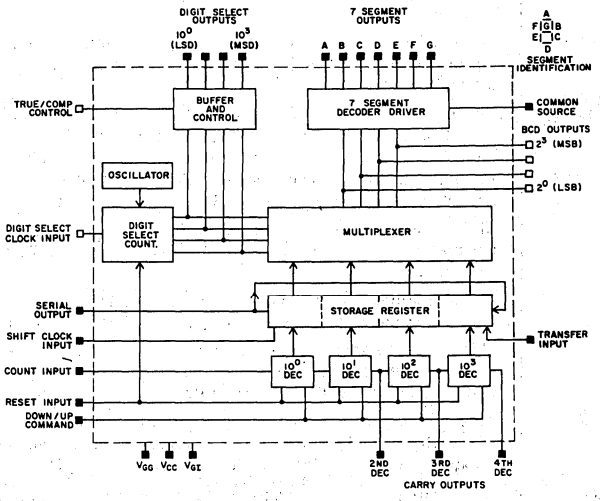
AY-5-4007A, available in 40 Lead Dual In Line package, allows for all available functions.

The AY-5-4007 and AY-5-4007D incorporate the most commonly used features in 24 Lead Dual In Line packages.

BLOCK DIAGRAM

AY-5-4007A shown:

■ indicates functions available with the AY-5-4007D.

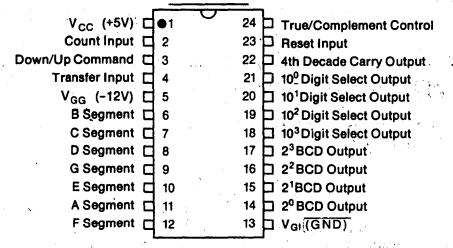


CONSUMER

PIN CONFIGURATIONS

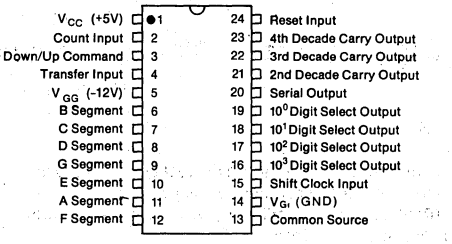
24 LEAD DUAL IN LINE
AY-5-4007

Top View



24 LEAD DUAL IN LINE
AY-5-4007D

Top View



NOTE: For AY-5-4007D, True/Complement control is internally connected to logic "0" level.

PIN FUNCTIONS

Name	Function
COUNT INPUT	Count Input operates the decade counters synchronously on the positive going edges (logic '0' to '1' transitions).
RESET INPUT	When this input goes to a logic '1' it resets the decade counters to 0000, forces the digit select counter to the MSD position and the Digit Select Outputs to 'not active' logic levels to blank the display. It must be present for a minimum of 10 μsec.
DOWN/UP COMMAND	The count direction depends upon the logic level on the DOWN/UP Command input. Logic '0' = Count UP. Logic '1' = Count DOWN.
2ND DECADE CARRY OUTPUT **3RD DECADE CARRY OUTPUT** **4TH DECADE CARRY OUTPUT**	Normally the Carry Outputs are at a logic '0' level; when activated a positive pulse is generated on the output line, which is identical with the Count Input causing the carry.
TRANSFER INPUT	Placing the Transfer Input at a logic '1' allows transfer of data from the decade counters to the storage register.
SHIFT CLOCK INPUT	This input is used to apply clock pulses to the storage register for serial shift operation. Normally Shift Clock is maintained at a Logic '1' and negative pulses are necessary to perform shift operation. Actual shifting of storage register data is done on the second edge (positive going) of each clock pulse. A Pull-up resistor is internally provided for the Shift Clock Input so that this line, if not used, may be left floating. Since the storage register is quasi-static in serial shift operation the width of negative pulses (at logic '0') has to be limited to 20 μsec. During serial shift operation the Transfer input must be at a logic '0'.
SERIAL OUTPUT	This is the serial output of the storage register. When serial shift operation is not performed the Serial Output is the least significant bit of the least significant digit of the storage register.
10^0 DIGIT SELECT OUTPUT (LSD) **10^1 DIGIT SELECT OUTPUT** **10^2 DIGIT SELECT OUTPUT** **10^3 DIGIT SELECT OUTPUT (MSD)**	These outputs provide sequentially an active logic level (logic '1' if the True/Complement Control is at a logic '1'; logic '0' if the True/Comlement Control is at a logic '0'), to specify which of the corresponding digits is selected and displayed, the remaining 3 Outputs being 'not active'. All the Digit Select Outputs are forced to a 'not active' logic level as long as the Reset Input is active.
2^0 BCD OUTPUT(LSB) **2^1 BCD OUTPUT** **2^2 BCD OUTPUT** **2^3 BCD OUTPUT(MSB)**	These outputs provide the Binary Coded Decimal representation of the digit being selected and displayed by the multiplexer. The truth table shows BCD Codification of these outputs.
"A" TO "G" SEGMENT	These outputs are programmed according to the truth table. Each output terminal is actually connected to the drain of the corresponding output transistor.
COMMON SOURCE	This is the common of the seven segment output transistors. When not externally available the corresponding terminal is internally tied to VGI (0V) line. It may be connected to any voltage between VSS and VDD according to requirements.
TRUE/COMPLEMENT CONTROL	This input controls the polarity of the Digit Select Outputs active logic level. When the TRUE/COMPLEMENT Control is at a logic '1', active level for the Digit Select Outputs is a logic '1', when at a logic '0' active level is a logic '0'.
DIGIT SELECT CLOCK INPUT	An external signal applied to this terminal overrides the internal oscillator. When the internal oscillator is used, this terminal must be left floating.

CONSUMER

ELECTRICAL CHARACTERISTICS

Maximum Ratings *

Voltage on any pin with respect to V_{CC}. . . . . −20 to +0.3V
Storage temperature range. . . . . −65°C to +150°C
Ambient operating temperature range . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

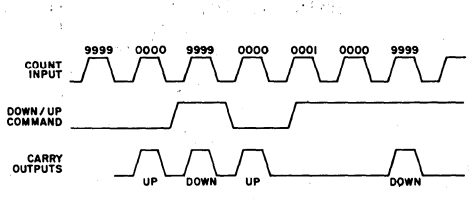
V_{CC} = +5.0 ±0.5V V_{GG} = −12V ±1V OR −7.0V ±0.5V
V_{GI} = 0V Operating Temperature (T_A) 0°C to +70°C

Characteristic	V_{GG} = −12V ±1V			V_{GG} = −7V ±0.5V			Units	Conditions
	Min	Typ	Max	Min	Typ**	Max		
Inputs								
Logic '0'	V_{GG}	-	+0.8	V_{GG}	-	+0.8	Volts	See Fig. 4
Logic '1'	V_{CC}−1.5	-	V_{CC}+0.3	V_{CC}−1.5	-	V_{CC}+0.3	Volts	
Capacitance	-	-	10.0	-	-	10.0	pF	V_{IN} = V_{CC} f = 1MHz
Leakage	-	-	5.0	-	-	5.0	µA	V_{IN} − V_{CC} = −10V at 25°C
Repetition Rate	D.C.	-	600	D.C.	-	350	kHz	Square Wave
Pulse Width	0.7	-	-	1.0	-	-	µsec	Pulse either high or low
Tr & Tf	-	-	100			100	µsec	
True/Complement/ Control Input								
Input Current	10	40	100	10	-	50	µA	V_{IN} = V_{CC}
	10	25	50	10	-	25	µA	V_{IN} = V_{GI} See Fig. 5
Digit Select Clock								
Input Current	10	60	150	5	25	75	µA	V_{IN} = V_{CC} (Sink)
	50	250	1600	50	150	1000	µA	V_{IN} = V_{GI} (Source) See Fig. 3
Internal Freq.	1.0	2.0	4.0	1.0	2.0	4.0	kHz	
External Freq.—Data only	D.C.	-	100	D.C.	-	50	kHz	
Display	D.C.	-	15	D.C.	-	7	kHz	Display Duty Cycle 25%
Shift Clock								
Frequency	D.C.	-	1	D.C.	-	0.8	MHz	
Pulse Width	0.4	-	1000	0.5	-	1000	µsec	See functional description
Input Current	20	100	400	10	30	200	µA	V_{IN} = V_{GI} (See Fig. 6)
Outputs—7 Segment (See Note 2)								
Leakage Current	-	-	10	-	-	10	µA	V_{OUT}—V_{CC} = −10V at 25°C
Device on Current	15	25	45	12	20	35	mA	V_{CS}—V_{OUT} = +1.0V at 25°C, V_{CS} = V_{CC}
Device on Current	12	18	27	7	11	17	mA	V_{CS}—V_{OUT} = −1.0V at 25°C, V_{CS} = V_{GI}
Power Dissipation (per segment at 25°C)	-	-	200	-	-	200	mW	See Note 1 & Fig. 1
Other Outputs								
Logic '0'	-	0.2	0.4	-	0.3	0.4	Volts	I_{OL} = 1.6mA with 10pF load
Logic '1'	V_{CC} −1.0	V_{CC} −0.65	-	V_{CC} −1.0	V_{CC} −0.65	-	Volts	I_{OL} = 50µA
Propagation Delay	-	-	1.0	-	-	1.5	µsec	Carry Output } See Fig. 2
			1.5	-	-	2.0	µsec	Serial Output }
Tr, Tf Rise, Fall Times	-	0.15	0.3	-	0.3	0.6	µsec	
Power								
I_{GG}	-	25	40	-	13	20	mA	(V_{CC} to V_{GG})

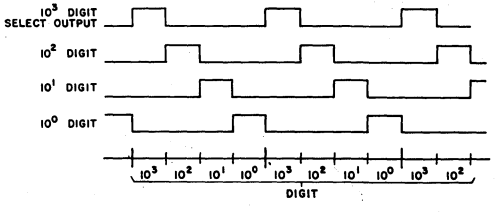
**Typical values are at +25°C and nominal voltages.

NOTES:
1. Derate Power Linearly to 100mW at 70°C.
2. See also Typical 7-Segment Output Curves, Figs. 9, 11, & 13 (−12V ±1V)
   See also Typical 7-Segment Output Curves, Figs. 10, 12, & 14 (−7V ±0.5V)

TIMING DIAGRAMS



CARRY OPERATION



DIGIT SELECT OPERATION
(True/Complement Control is at logic '1' level)

CONSUMER

OPERATION

Decade Counters

The four decade counters are synchronously operated on the positive going edges of the Count Input; a single DOWN/UP Command controls the direction of counting. The edge-triggered structure of the master-slave flip-flops allows the count direction to be changed between count pulses at either Count Input level. A Reset Input resets decade counters to 0000.

Carry outputs are provided at the 2nd, 3rd and 4th decade; these outputs are activated when an overflow (in counting up) or an underflow (in counting down) condition exists in the corresponding decade counter. The carry output pulse is the same as the Count Input pulse causing the carry.

The look ahead design of the carry stages gives error free outputs when reversing the count direction.

Storage Register

Data in the decade counters is transferred to the storage register under control of the Transfer Input signal. The Transfer Input may be connected to a logic '1' for a continuous transfer and display operation.

The Storage register may also be operated as a parallel-in serial-out shift register. In this case clock pulses are to be provided to Shift Clock Input, the serial content of storage register is available on the Serial Output line, and recirculated back to the first stage input. A train of 16 clock pulses is needed to extract the full content of the register, least significant bit of least significant digit first. When operating the storage register serially, Transfer input is to be kept at a logic '0'.

Digit Select Counter and Multiplexer

The digit select counter is driven by a built in oscillator which requires no external components. The internal oscillator can be overridden by applying an external signal to the Digit Select Clock Input.

The digit select counter controls the multiplexer to route information from storage register to the 7 segment decoder drivers and to the BCD Outputs.

The counter scans from MSD (10^3 digit) to LSD (10^0 digit). Each of the four Digit Select Outputs is sequentially activated when the corresponding digit is selected and displayed.

The Digit Select counter is forced to MSD position and Digit Select Outputs are forced to 'not active' logic levels as long as Reset Input is active. This feature blanks the display when the device is being reset. The True/Complement Control inverts the Digit Select Outputs active logic level for flexibility of output interface circuitry.

Internal delay logic ensures that both 7 segment outputs and BCD outputs are valid before activation of the corresponding Digit Select Output to avoid "ghost images".

7 Segment Decoder Driver

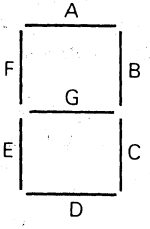
The 7 segment decoder drivers consist of very low impedance output transistors (typically 40 ohms) to minimize external interface components when driving 7 segment displays such as LEDs, fluorescents, incandescents, etc.

The 7 Segment Outputs are the drains of the corresponding output transistors, these outputs are programmed according to the truth table below. A Common Source terminal is also available to increase flexibility of use.

DIGIT	7 SEGMENT OUTPUT TRANSISTOR							BCD OUTPUT			
	A	B	C	D	E	F	G	MSB 2^3	2^2	2^1	LSB 2^0
0	*	*	*	*	*	*	–	0	0	0	0
1	–	*	*	–	–	–	–	0	0	0	1
2	*	*	–	*	*	–	*	0	0	1	0
3	*	*	*	*	–	–	*	0	0	1	1
4	–	*	*	–	–	*	*	0	1	0	0
5	*	–	*	*	–	*	*	0	1	0	1
6	*	–	*	*	*	*	*	0	1	1	0
7	*	*	*	–	–	–	–	0	1	1	1
8	*	*	*	*	*	*	*	1	0	0	0
9	*	*	*	*	–	*	*	1	0	0	1

LEGEND:
* output transistor ON
– output transistor OFF
0 logic '0'
1 logic '1'

SEGMENT IDENTIFICATION



7 SEGMENT AND BCD OUTPUTS TRUTH TABLE

CONSUMER

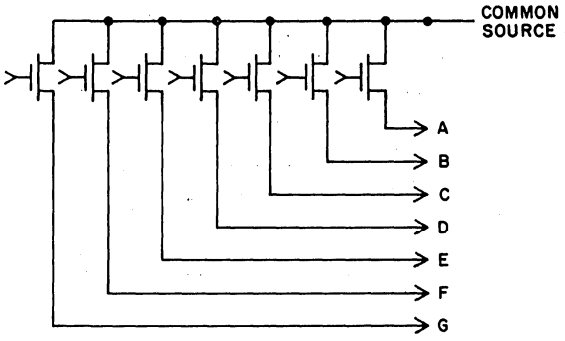


Fig.1 7-SEGMENT OUTPUTS

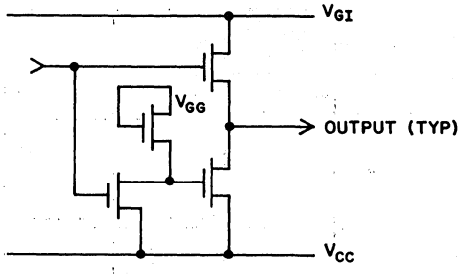


Fig.2 ALL OTHER OUTPUTS

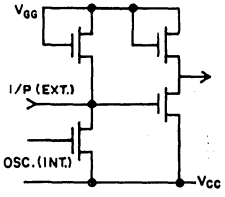


Fig.3 DIGIT SELECT CLOCK INPUT

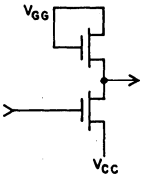


Fig.4 TYPICAL INPUT

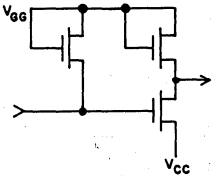


Fig.5 TRUE/COMPLEMENT INPUT

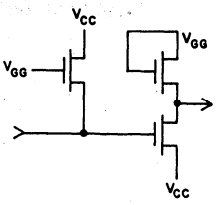


Fig.6 SHIFT CLOCK INPUT

CIRCUIT DIAGRAMS

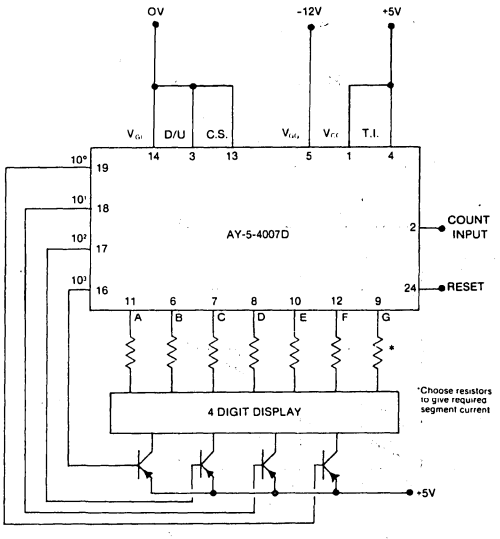


Fig.7 COMMON CATHODE LED DISPLAY

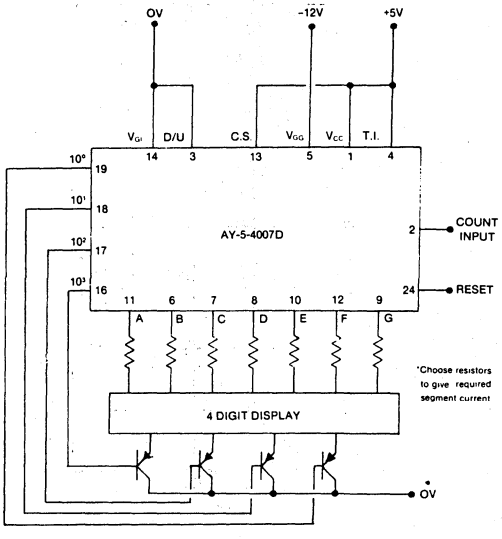


Fig.8 COMMON ANODE LED DISPLAY

CONSUMER

TYPICAL CHARACTERISTIC CURVES

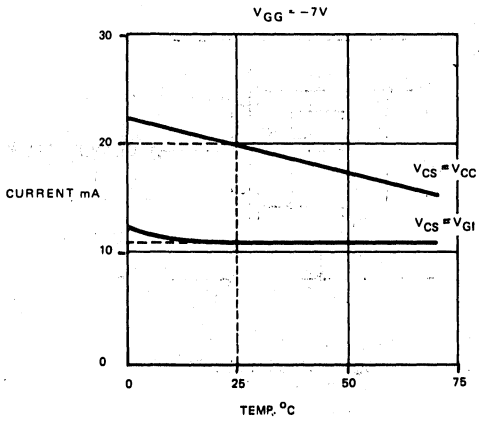


Fig.9

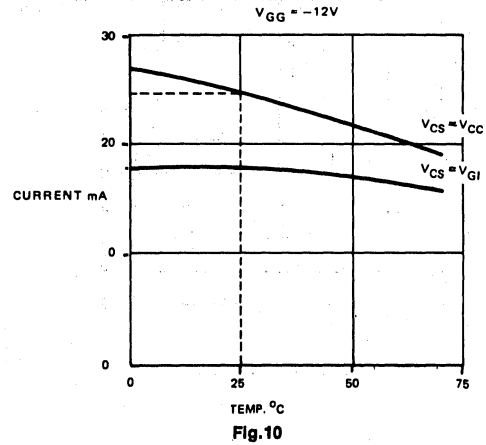


Fig.10

TYPICAL CURVES OF SEGMENT CURRENT VS. TEMPERATURE AT 1V ACROSS OUTPUT DEVICE

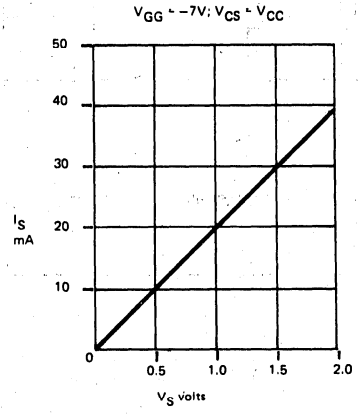


Fig.11

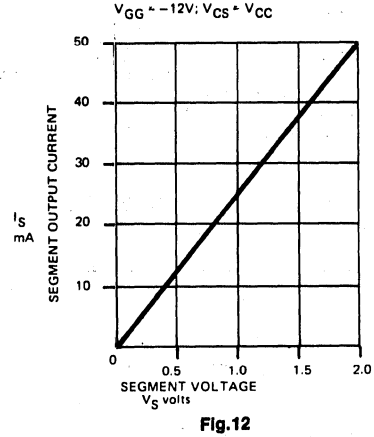


Fig.12

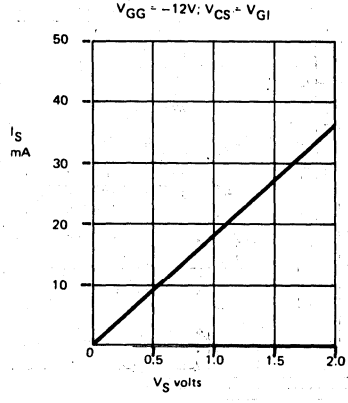


Fig.13

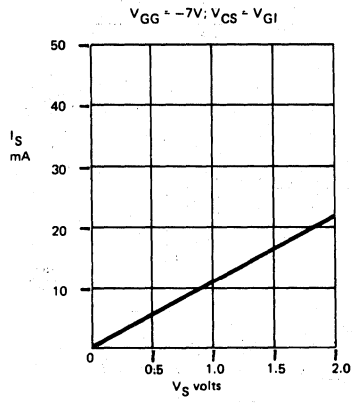


Fig.14

TYPICAL SEGMENT OUTPUT CURRENT VS. OUTPUT VOLTAGE AT +25°C

CONSUMER

Fluorescent Display Driver

FEATURES

- Multiplex drive for 7 or 21 digits without loss of brightness
- Accepts data in BCD or 7 segment format

DESCRIPTION

This family of devices can accept serial data from any system in BCD or 7 segmant format. Once accepted, the data is staticised and multiplexed out at a frequency of 8KHz to directly drive a segment fluorescent display.

Devices in the family are available according to the characteristics shown in the following table:

Device Type	Number of Digits	Data Input Format	Package
AY-5-4121	21	BCD	40 Pin
AY-5-4221	21	7 Segment	40 Pin

OPERATION

There are 2 modes of operation. In the first mode the CK input is forced and data input is synchronized with the clock line.

In the second mode a capacitor is connected between CK and V_{SS}. This allows the oscillator to free run. Data is then input asynchronously with the clock line.

Synchronous Operation (e.g. Data Input from PIC 1650A)

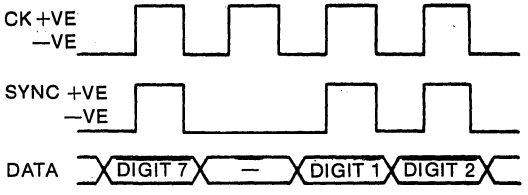


Fig. 1

The timing diagram for the control signals is shown in Fig. 1.

The CK line forces the oscillator and the SYNC line is used to strobe in data.

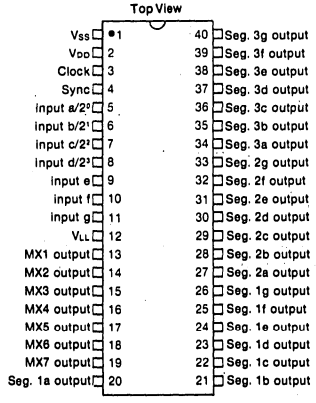
The input counter which is used to address the latches is reset by holding the SYNC line negative for one or more clock pulses. When the SYNC line is taken positive the data input to the first latch is enabled.

When this line falls, the input counter is clocked on and the second latch is addressed. Data input to the latch is then enabled by taking the SYNC line positive.

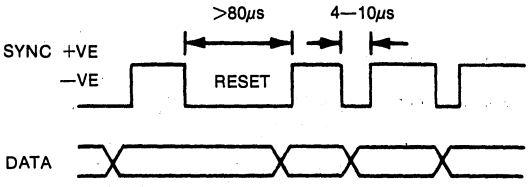
As can be seen from the timing diagram, data changes must take place when the SYNC is negative to ensure that date is valid during the period when the data input is enabled.

PIN CONFIGURATION

AY-5-4121/4221



Asynchronous Operation (e.g. Data Input from PIC 1650A)



In this case the SYNC line is used as before. In order to reset the counter, the line is held negative for a period >80μs. In order to clock onto the next latch, the line is taken negative for a period of between 4μs and 10μs.

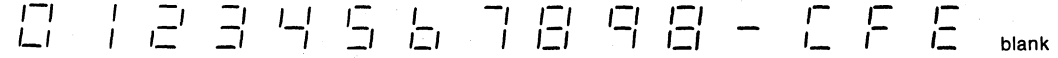
Again data change must take place when the SYNC line is negative to ensure that data is valid during the period when the data input is enabled.

DATA INPUT

In the seven segment option a negative level (V_{DD}) at the segment input causes that segment to be turned on at the appropriate MX period.

In the BCD option the logic 1 is taken as the positive level V_{SS}. Data is decoded as follows:

AY-5-4221



It is possible to change these characters by mask option.

CONSUMER

PIN FUNCTIONS

Pin No.	Name	Function
1	V_{SS}	Positive Supply
2	V_{DD}	Negative Supply
3	CK	This is the oscillator input. A capacitor is connected between this pin and V_{SS} to allow the oscillator to free run
4	SYNC	This input controls the Serial data input to the latches
5—11	Data Input	In the seven segment option a negative level turns the appropriate segment on. The BCD option, logic 1 is taken as the positive level (V_{SS})
—	DP Input	Logic levels as for Data Input
12	V_{LL}	Display supply voltage. All high voltage outputs have internal pull-down resistors connected to this pin
—	MX Outputs	Multiplex outputs are switched to V_{SS} to select a digit
13—19	MX Outputs	Multiplex outputs are switched to V_{SS} to select up to 3 digits
—	Segment Outputs	These outputs are switched to V_{SS} to turn on a segment
20—40	Segment Outputs	These outputs are switched to V_{SS} to turn on a segment. The outputs are arranged in 3 groups allowing up to 3 separate digits to be displayed on each multiplex slot

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... +3.0V to −35V
Operating temperatures range ..... 0°C to 85°C
Storage temperature range ..... −55°C to 150°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

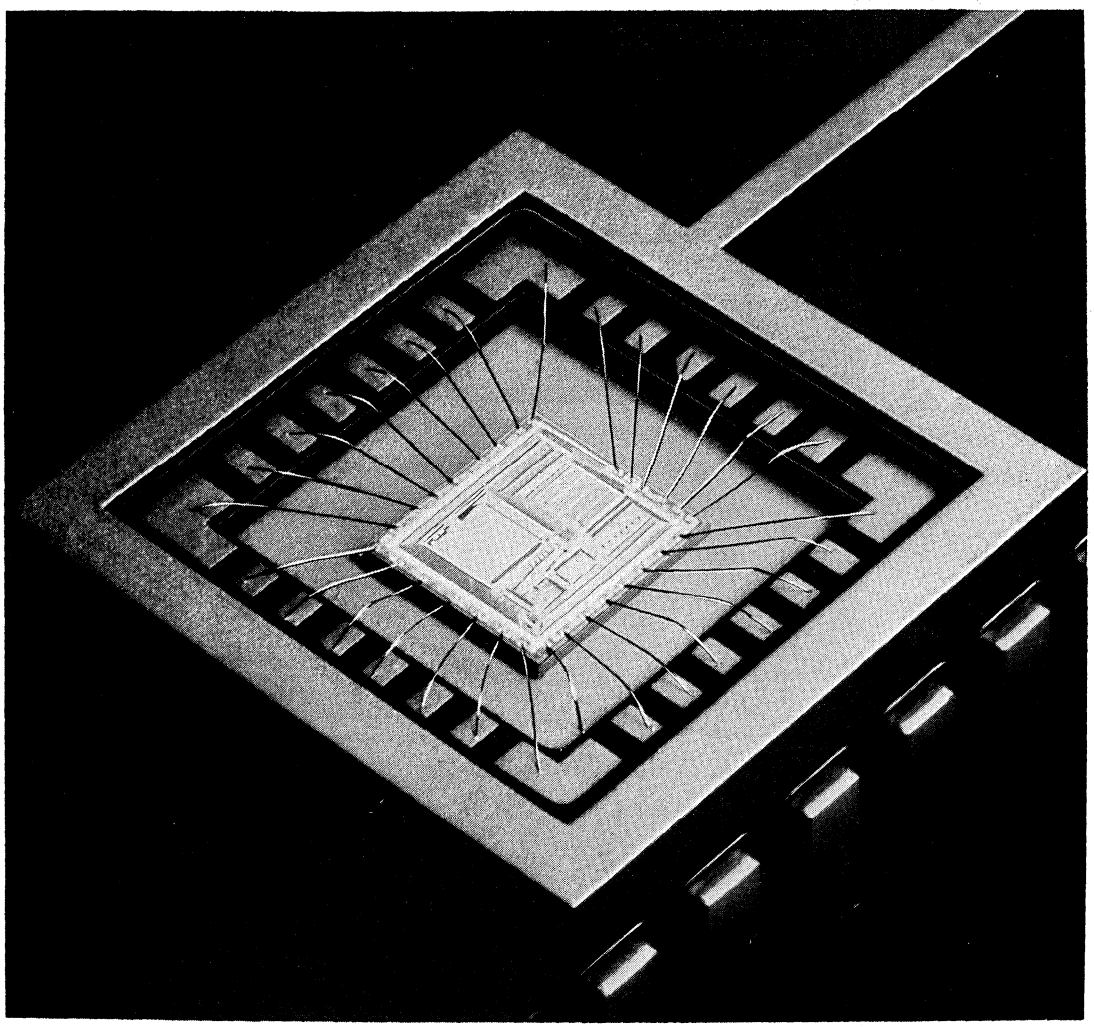
Standard Conditions (unless otherwise specified)

V_{SS} = 0V
V_{DD} = −12V ± 10%
V_{LL} = V_{DD} to −33V

Characteristics	Min	Typ	Max	Units	Conditions
Multiplex Clock Frequency	—	25	—	kHz	1000pF between CK and V_{SS}
Control Inputs					
Logic '0'	+0.3	—	−1.5	Volts	
Logic '1'	−5	—	V_{DD}	Volts	
Multiplex Outputs					
Logic '0'	—	—	−2	Volts	I_{out} = 5mA (note that on 21 digit versions total I_{out} is 3 x 5mA = 15mA)
Segment Outputs					
Logic '0'	—	—	−2	Volts	I_{out} = 2mA
Pull down current on high	300	—	550	μA	V_{LL} = −33 Volts V_{out} = −2 Volts
Voltage Outputs	40	—	75	μA	V_{LL} = −33 Volts V_{out} = −2 Volts

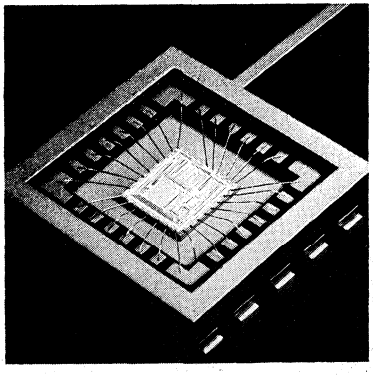
CONSUMER

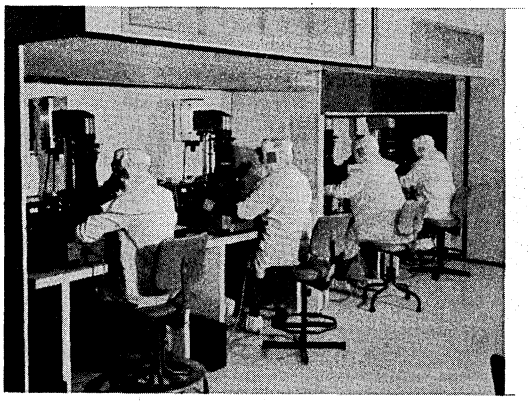
General Information 9



GENERAL INSTRUMENT

A Total Technological Service





GENERAL INSTRUMENT

The Microelectronics Division of General Instrument Corporation is one of the world's leading manufacturers of LSI (Large Scale Integrated) microcircuits. A pioneer in MOS in 1966, General Instrument is a worldwide source of microcircuits utilizing Hybrid, Bipolar and MOS technologies in service to the consumer, industrial and public service marketplaces.

The Microelectronics Division has facilities in every major market providing customers with a full spectrum of services including immediate delivery...new product development...applications engineering...and high volume circuit manufacturing.

Strategically Located Plants

The Microelectronics Group operates five main production facilities in the United States, Europe and Far East. Plants at Glenrothes, Scotland; Chandler, Arizona; and Hicksville, New York, have complete capability for product design, mask making, diffusion, assembly, test and quality assurance. Factories in Kaohsiung, Taiwan, and Manila, Philippines are dedicated to high volume assembly, test, quality assurance and applications of Microelectronics products.

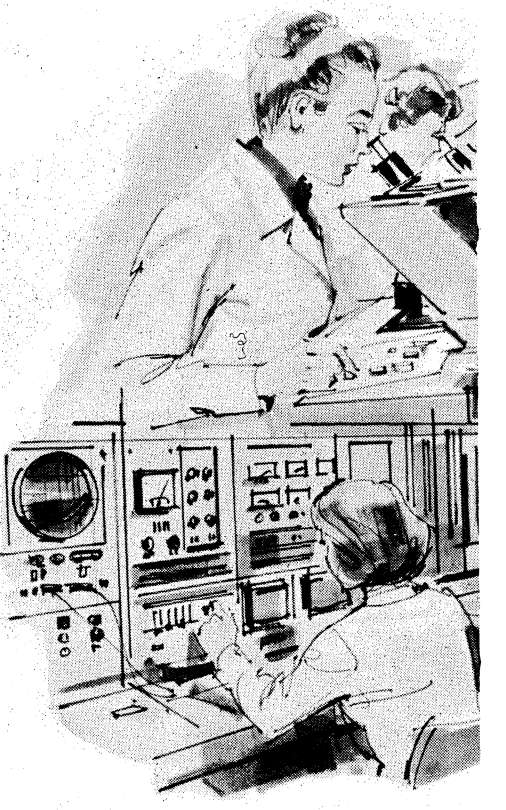
In addition to providing reliable sources of supply on three continents, General Instrument operates each plant as a backup facility to the others, to insure uninterrupted delivery. Common processes and equipment are employed and major product styles are always produced in at least two separate locations. To maintain uniform standards from plant to plant, the quality assurance and process control groups at each facility are directed by quality control policy established at Group and Corporate levels.

Processes

Microelectronics products produced by the Microelectronics Division are in accordance with technologies that are standard to the Microelectronics industry. Production capability exists for P-Channel Metal Gate, N-Channel Metal Gate, N-Channel Silicon Gate, CMOS and I^2L. In addition, General Instrument is the world's leading manufacturer of products in the non-volatile memory nitride technology. This broad repertoire provides you, the customer, with the best process for the job every time.

Product Quality

With a major investment in product test and in-line quality control equipment, the Microelectronics Division of General Instrument is dedicated to delivery of complex integrated circuits to the incoming quality level and with the reliability its customers require. Most products routinely receive final test at elevated temperature



temperature and extensive burn-in facilities exist for 100% preshipment stress as well as confirmation of outgoing product quality.

Customer Service

General Instrument Microelectronics believes in CUSTOMER SERVICE. Customer Service departments are maintained at each major location to provide immediate response to questions concerning order service and delivery. Our customer service personnel are trained to consider our customers' needs as their most urgent requirement. Call on them and let us prove that we are dedicated to responsive service.

Advanced Design Centers

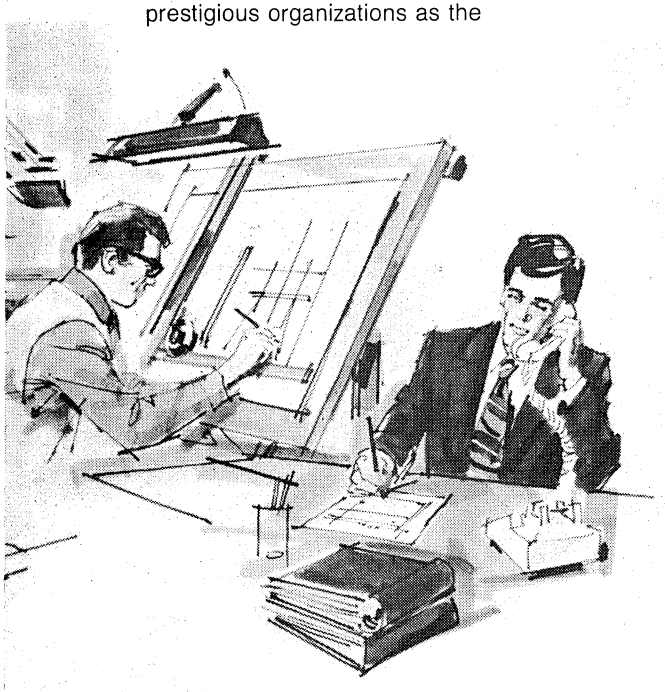
To provide our customers with the latest in LSI technology, General Instrument Microelectronics maintains R&D centers at Glenrothes, Scotland; Hicksville, New York; and Chandler, Arizona. In addition, the Microelectronics activity is supported by general research in various fields carried out with such prestigious organizations as the Massachusetts Institute of Technology, State University of New York at Stony Brook and the University of Utah.

In addition to its extensive catalog of standard products, General Instrument Microelectronics is happy to provide custom design service to satisfy special requirements. In some cases, the application is best served by a software or firmware modification of one of our standard microprocessors. In other cases, a dedicated microprocessor is more cost effective. These services may be arranged through any of the Microelectronics sales offices.

Applications Assistance Around the Globe

To provide the special applications assistance that customers may require, General Instrument Microelectronics maintains fully staffed Applications Centers at strategic locations around the world...
U.S.A. — Hicksville, New York; Chandler, Arizona; and Los Angeles, California.
EUROPE — Glenrothes, Scotland; London, England; Paris, France; Munich, Germany.
ASIA — Kaohsiung, Taiwan; Tokyo, Japan; and Hong Kong.

Arrangements can be made for immediate assistance from these centers by contacting any of the sales offices listed in this booklet.

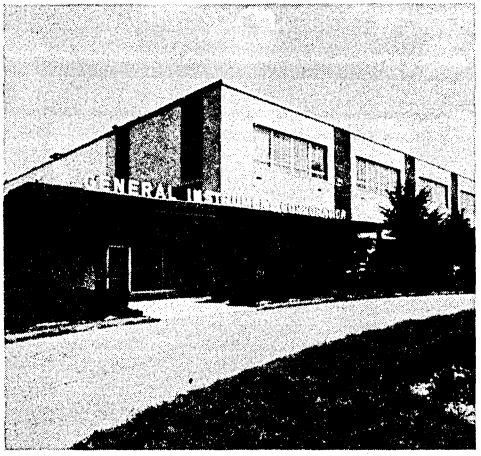


Corporate Support

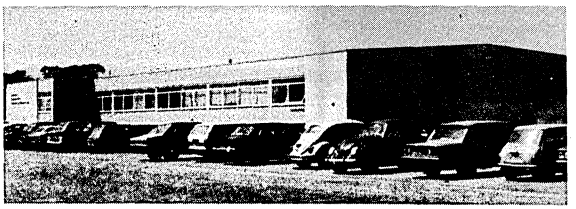
General Instrument Microelectronics is backed by the full resources of the General Instrument Corporation, which has for over 50 years been among the leaders in the application of modern technology to entertainment, industrial, military, data and communications electronics. The skills, production know-how, and technological capability of the entire General Instrument organization are utilized by the Microelectronics Group to further improve its products and customer services.

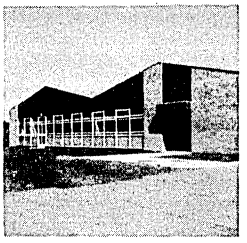
Among the many other electronic components manufactured by General Instrument are discrete semiconductors, relays, miniature lamps, and TV components. General Instrument is a leading manufacturer of cable TV products, off-track and on-track wagering systems, point-of-sale equipment and apparatus for defense applications.

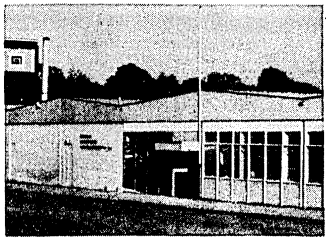
MANUFACTURING FACILITIES



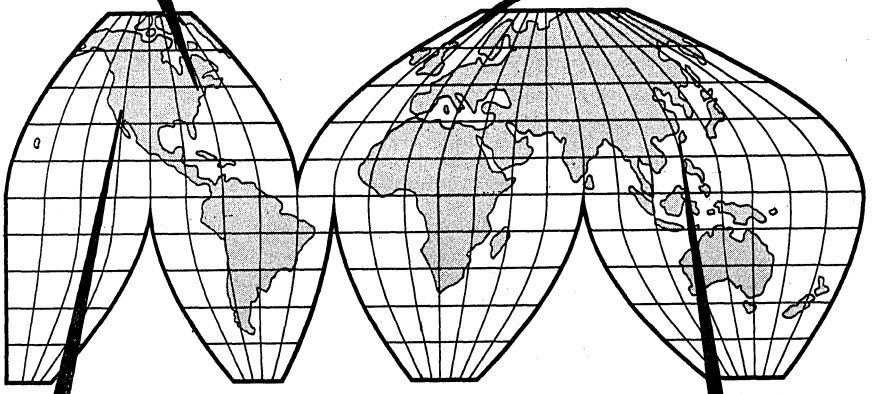
HICKSVILLE, NEW YORK



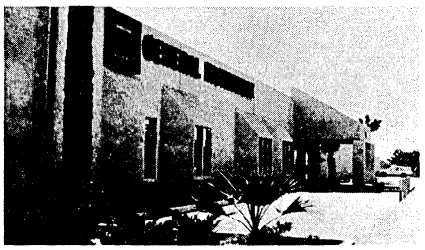


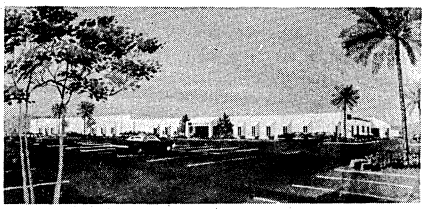


GLENROTHES, SCOTLAND

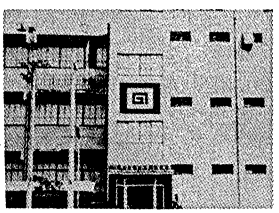


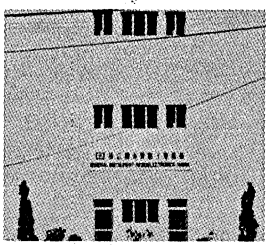
CHANDLER, ARIZONA





KAOHSIUNG, TAIWAN

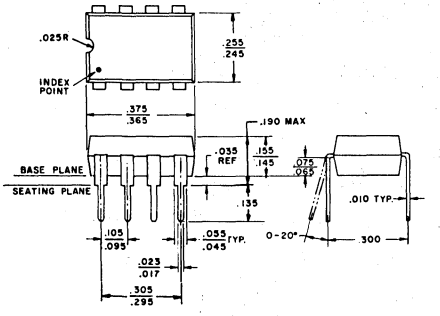




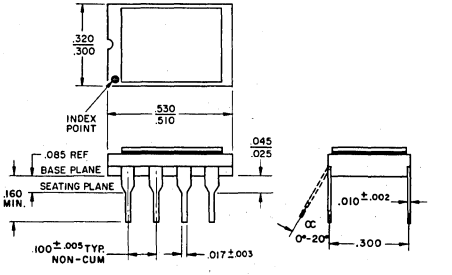
PACKAGE OUTLINES

PACKAGE OUTLINES (All dimensions in inches)

8 LEAD DUAL IN LINE

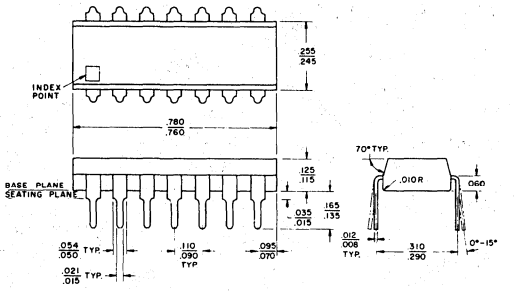


PLASTIC



CERAMIC

14 LEAD DUAL IN LINE



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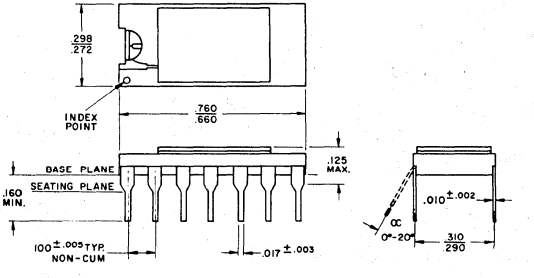
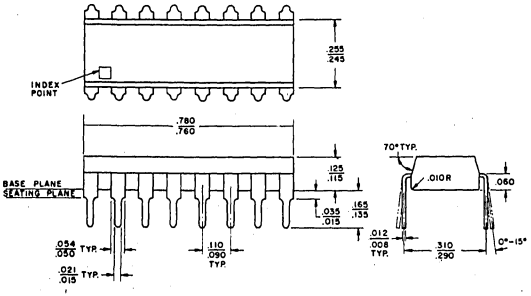


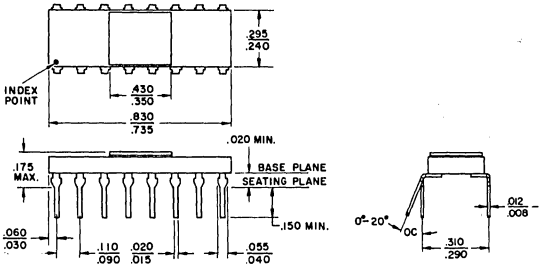
CERAMIC

GENERAL INFORMATION

PACKAGE OUTLINES (All dimensions in inches)

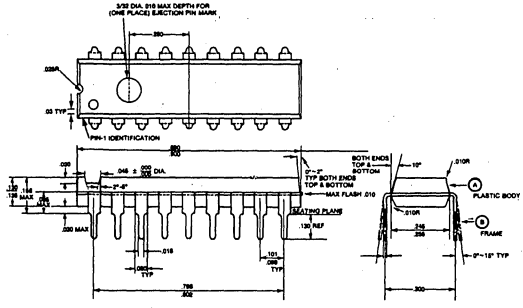
16 LEAD DUAL IN LINE

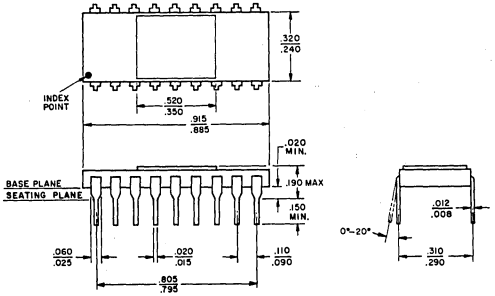




PLASTIC **CERAMIC**

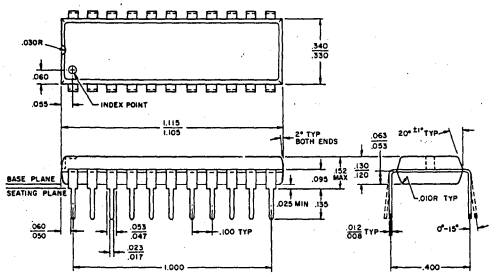
18 LEAD DUAL IN LINE

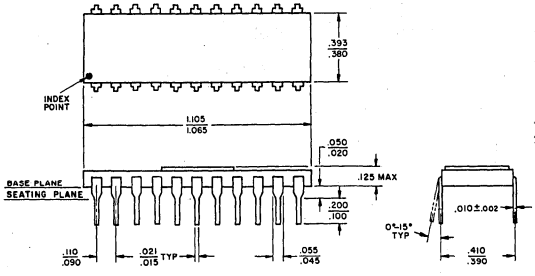




PLASTIC **CERAMIC**

22 LEAD DUAL IN LINE





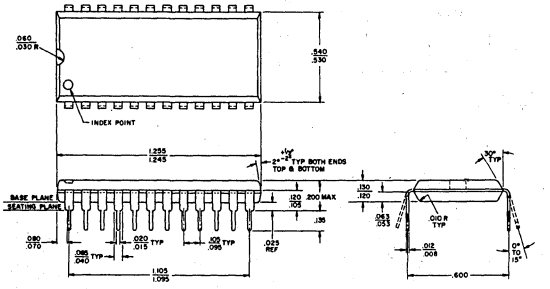
PLASTIC **CERAMIC**

GENERAL INFORMATION

PACKAGE OUTLINES

PACKAGE OUTLINES (All dimensions in inches)

24 LEAD DUAL IN LINE



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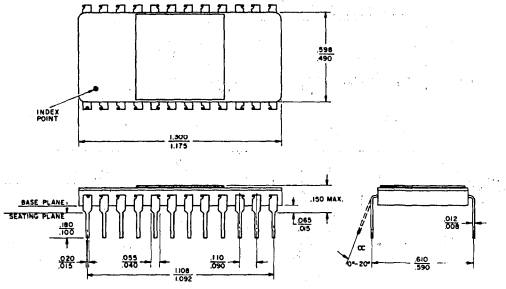
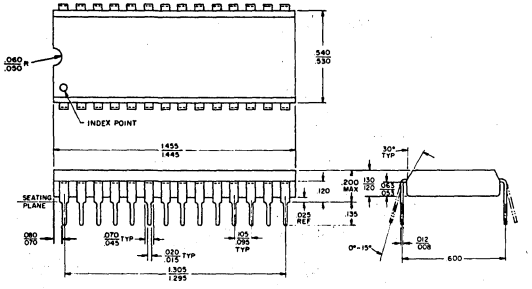


CERAMIC

28 LEAD DUAL IN LINE



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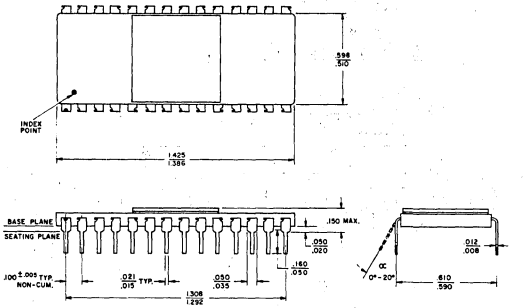
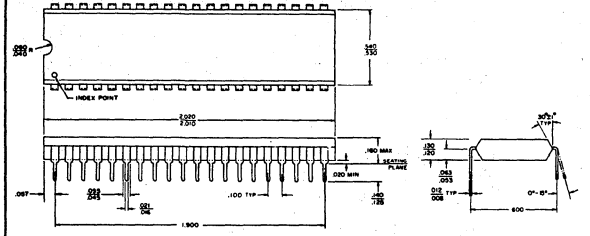
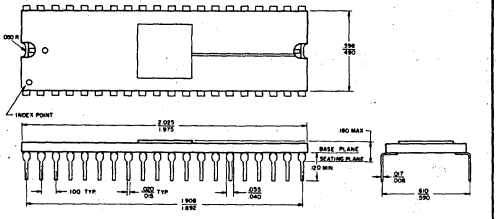


CERAMIC

40 LEAD DUAL IN LINE



PLASTIC

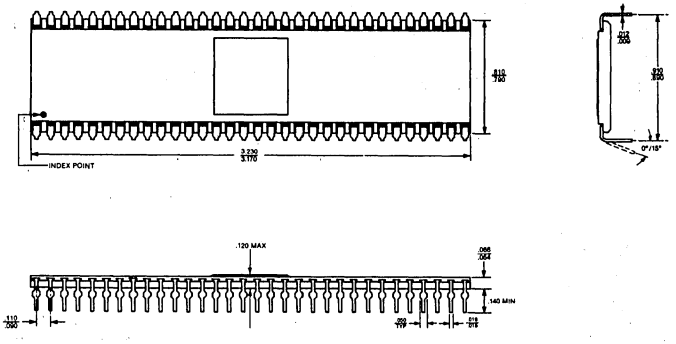


CERAMIC

GENERAL INFORMATION

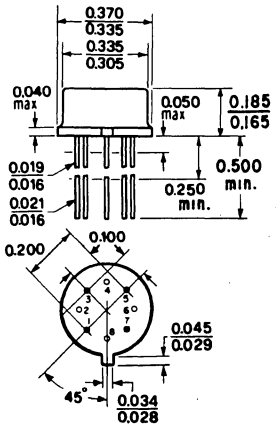
PACKAGE OUTLINES (All dimensions in inches)

64 LEAD DUAL IN LINE

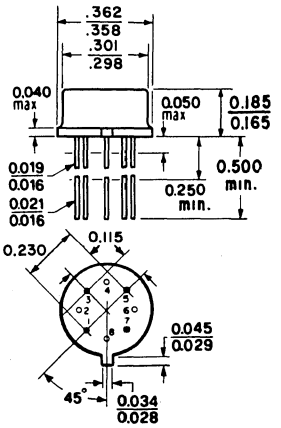


CERAMIC

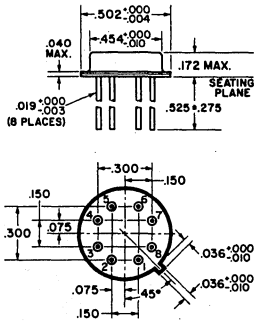
8 LEAD TO-78



8 LEAD TO-99



8 LEAD TO-8

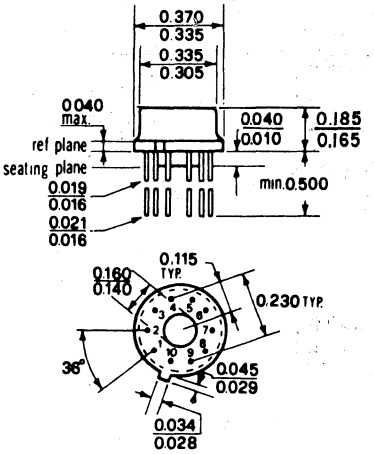


GENERAL INFORMATION

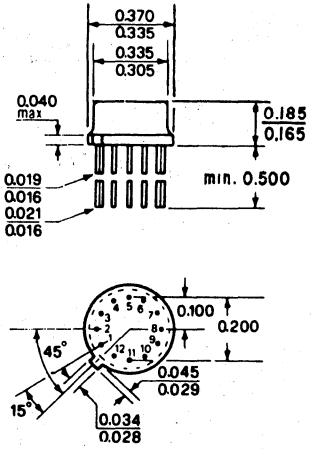
PACKAGE OUTLINES

PACKAGE OUTLINES (All dimensions in inches)

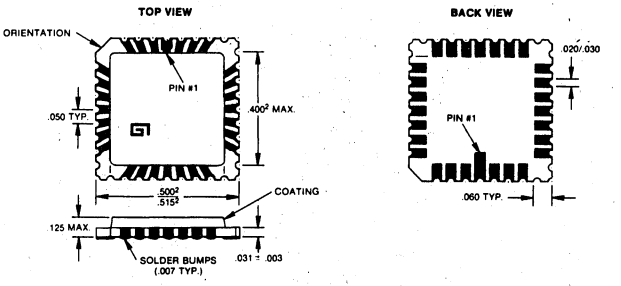
10 LEAD TO-100



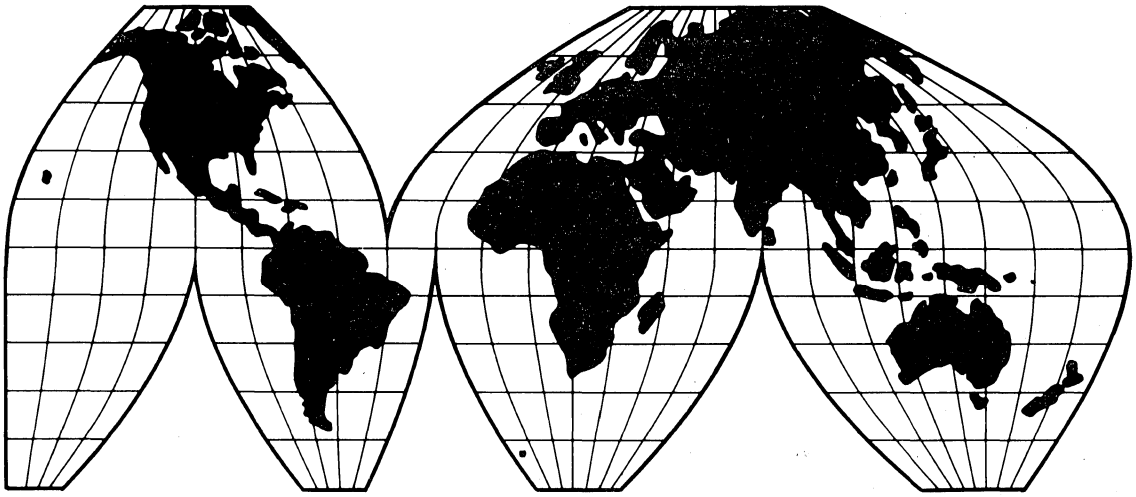
12 LEAD TO-73



28 LEAD MINI-PAK



GENERAL INFORMATION



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A. Consumer and Entertainment—1%.

B. Industrial and Military products—.65%.

Repairs that are the Seller's responsibility may, at Seller's election, be made at Buyer's premises.

6. QUANTITIES. Any variation in quantities shipped over or under the quantities ordered (not to exceed 5% for standard products and not to exceed 10% for custom and custom-patterned products) shall constitute compliance with Buyer's order and the unit price shall continue to apply. All claims for shortages in excess of such variations shall be made within ten (10) days after date of receipt of shipment.

7. CONTINGENCIES. Seller shall not be liable for any delay in performance or for non-performance, in whole or in part, caused by the occurrence of any contingency beyond the control either of Seller or Seller's suppliers, including, but not limited to, war (whether an actual declaration thereof is made or not), sabotage, insurrection, riot or other act of civil disobedience, act of a public enemy, failure or delay in transportation, act of any government or any agency or subdivision thereof affecting the terms of this contract or otherwise, judicial action, labor dispute, accident, fire, explosion, flood, storm or other Act of God; shortage of labor, fuel, raw materials, tools, dies, or equipment; or technical or yield failure. Any such delays shall excuse Seller from performance, and Seller's time for performance shall be extended, for the period of the delays and for a reasonable period thereafter. If any contingency occurs, Seller may allocate production and deliveries among any or all of Seller's customers as Seller may determine, including, without limitation, regular customers not then under contract and Seller's (including Seller's subsidiaries' and affiliates') own requirements for further manufacture or other use.

8. SUBSTITUTION AND MODIFICATION OF GOODS. Seller has the right to modify the specifications of goods designed by Seller and substitute substantially equivalent goods manufactured to such modified specifications.

9. WARRANTIES. Seller, except as otherwise herein provided, warrants that the goods shall be free from defects in materials and workmanship (under normal use and services) for the following periods:

A. Consumer and Entertainment products—90 days.

B. Industrial and Military products—1 year.

C. Processed semiconductor chips—30 days.

Seller's warranties shall not extend to any items subjected to accident, misuse, neglect, alteration, improper installation, improper testing or unauthorized repair.

Seller makes NO WARRANTY as to experimental or developmental goods or goods not manufactured by Seller. As to goods not manufactured by Seller, at Buyer's request, Seller, to the extent permitted by Seller's contract with its supplier, shall assign to Buyer any rights Seller may have under any warranty of the supplier thereof.

Seller's warranties extend to the Buyer and to no other person or entity.

Seller's warranties as hereinabove set forth shall not be enlarged, diminished or affected by, and no obligation or liability shall arise or grow out of, Seller's rendering of technical advice or service in connection with Buyer's order of the goods furnished hereunder.

The foregoing are in lieu of all warranties, express, implied or statutory, including, but not limited to, any implied warranty of merchantability or fitness for a particular purpose and any other warranty obligation on the part of the Seller.

10. PROPRIETARY RIGHTS AND CONFIDENTIALITY.

(a) All information, know-how, programming, software, trademarks, trade secrets, plans, drawings, specifications, designs and patterns furnished or created by Seller or by Seller's agents or contractors (other than Buyer) and any and all property rights embodied therein are and shall remain the sole property of Seller and neither Buyer nor any other party shall have or acquire any interest therein.

(b) Buyer recognizes and acknowledges that certain confidential, secret or proprietary information possessed by Seller ("Information") is a valuable business asset of Seller and that disclosure of the Information would cause grave and irreparable injury to Seller. Buyer shall at all times, whether during the term of this contract or subsequent thereto, honor, maintain and protect the confidentiality and secrecy of such of the Information as Seller may disclose to Buyer or its agents. Buyer shall not make any copies of any of the Information without prior written consent of Seller and will take appropriate action to restrict access to the Information to those of its employees and agents who have an actual need for such access in the course of their duties. This provision shall survive the performance, termination or cancellation of this contract.

11. TOOLING. Unless otherwise expressly provided, Seller will retain title to, possession of, and the right to exclusive use of, all jigs, dies, fixtures, molds, patterns, gauges, taps, equipment, manufacturing aids and similar devices, made or obtained for the performance of this contract, without regard to whether a separate charge is made for the same.

12. PATENT INDEMNITY. Seller will defend any suit or proceeding brought against Buyer to the extent that such suit or proceeding is based on a claim that goods manufactured and sold by Seller to Buyer constitute direct infringement of any valid United States patent and Seller shall pay all damages and costs awarded by final judgment (from which no appeal may be taken) against Buyer, on condition that Seller (i) is promptly informed and furnished a copy of each communication, notice or other action relating to the alleged infringement, (ii) is given authority, information and assistance necessary to defend or settle such suit or proceeding in such manner as Seller shall determine, and (iii) is given sole control of the defense (including the right to select counsel), and the sole right to compromise and settle such suit or proceeding. Seller shall not be obligated to defend or be liable for costs and damages if the infringement arises out of compliance with Buyer's specifications or from a combination with, an addition to, or modification of the goods after delivery by Seller, or from use of the goods, or any part thereof, in the practice of a process.

If any goods manufactured and supplied by Seller to Buyer are held to directly infringe any valid United States patent and Buyer is enjoined from using the same, or if Seller believes such infringement is likely, Seller will exert reasonable efforts, at its option and at its expense, (i) to procure for Buyer the right to use such goods free of any liability for patent infringement, or (ii) to replace (or modify) such goods with a non-infringing substitute otherwise complying substantially with all the requirements of the contract, or (iii) upon return of the goods, refund the purchase price and the transportation costs of such goods. If the infringement is alleged prior to completion of delivery of the goods, Seller has the right to decline to make further shipments without being in breach of contract. If Seller has not been enjoined from selling such goods to Buyer, Seller may (at Seller's sole election), at Buyer's request, supply such goods to Buyer, in which event Buyer shall be deemed to extend to Seller the same patent indemnity hereinabove stated.

The same patent indemnity shall be deemed to be extended to Seller by Buyer if any suit or proceeding is brought against Seller based on a claim that the goods manufactured by Seller in compliance with Buyer's specifications infringe any valid United States patent.

The foregoing states the sole and exclusive liability of the parties hereto for infringement or the like of patents, trademarks and copyrights, whether direct or contributory, and is in lieu of all warranties, express, implied or statutory in regard thereto, including, without limitation, the warranty against infringement specified in the Uniform Commercial Code.

13. SOFTWARE INDEMNIFICATION AND DISCLAIMER.

(a) In the event any software used by Seller in the products shown on the front hereof is furnished or created by someone other than Seller, Buyer shall indemnify and hold Seller harmless from and against any and all loss, claim, damages, liability, cost, expense (including reasonable attorneys' fees) and any causes of action whatsoever, arising out of or in connection with claims by third parties of any description or nature concerning any such software, including, but not limited to, a claim that such software is owned by a third party.

(b) Seller hereby disclaims any and all liability for any claims or damages of any description or nature arising from: (1) the unknowing duplication or use of Buyer's software, in whole or in part, in products manufactured by Seller for others; or (2) alleged error in any software furnished or created by (i) any person other than Seller or (ii) Seller if Buyer has approved such software.

14. TERMINATION. Except as provided in paragraph 15(a) this contract shall not be terminated by Buyer without Seller's prior written consent. If Seller so consents to such termination, Buyer shall be liable for termination charges including, without limitation, a price adjustment based on the quantity of goods actually delivered as provided in paragraph 2, and all costs, direct and indirect, incurred and committed for this contract together with reasonable allowance for prorated expenses and anticipated profits.

15. REMEDIES AND DAMAGES.

(a) Where Buyer rightfully and timely rejects or justifiably revokes acceptance of items, or where Buyer has accepted nonconforming items and has timely notified Seller of a breach of warranty, Seller's sole and exclusive liability will be (at Seller's option) to repair, replace or credit Buyer's account with respect to any nonconforming goods returned to Seller during the applicable warranty period set forth above, and with respect to any nonconforming services, on condition that (i) Seller is, promptly upon Buyer's discovery of the nonconformity, notified in writing with a detailed explanation, (ii) the nonconforming goods are returned to Seller, F.O.B. Seller's plant from which the goods were shipped, and (iii) Seller's examination discloses that such items are nonconforming.

Where Seller fails to make shipment or repudiates or breaches any other material provisions of this contract (other than the warranty against patent infringements), including, without limitation, Seller's obligations with respect to nonconforming items, Buyer shall promptly give written notice to Seller. In the event that Seller does not cure any such failure to ship, repudiation or breach within 60 days after receipt of such notice, then Buyer shall have the right, at its option, to cancel the specific quantity of products not shipped, or terminate this contract as to the products as to which such repudiation or breach related, and that shall be Buyer's sole and exclusive remedy. If Buyer desires to exercise such right of termination it shall give written notice to Seller.

Except as set forth above, in no event will Seller be liable to anyone for direct, indirect, special, incidental or consequential damages for breach of any of the provisions of this contract, including, but not limited to, breach of provisions regarding warranties, indemnities and patent infringement. Such excluded damages include, without limitation, costs of removal and reinstallation of items, loss of goodwill, loss of profits and loss of use.

(b) Seller has the right to cancel this contract if: (i) unless otherwise specified on the front hereof, Buyer does not release all quantities within twelve (12) months, and unless caused by Seller's fault, shipment does not occur within eighteen (18) months after the date Seller received Buyer's order; or (ii) in Seller's sole judgment, Buyer's financial condition does not justify the terms of payment applicable from time to time, and upon demand therefor, Buyer shall not immediately comply with any modification of payment terms required by Seller in accordance with paragraph 3.

If Seller exercises such right to cancel, Buyer shall be liable for the charges referred to in paragraphs 2 and 14 in addition to any other remedies Seller may have hereunder or at law.

16. WAIVER. In the event of any default or breach by Buyer, Seller has the right to refuse to make further shipments. Seller's failure to enforce at any time or for any period of time any of the provisions of this contract shall not constitute a waiver of such provisions or of the right of Seller to enforce each and every provision.

17. GOVERNING LAW. The validity, construction and performance of this contract and the transactions to which it relates shall be governed by the laws of the State in which the chief executive offices of the Seller are located, without regard to conflict of laws principles. All actions, claims or legal proceedings in any way pertaining to this contract or such transactions shall be commenced and maintained in the courts of such State or in a federal court of the United States physically situated in such State and in no other court or tribunal whatsoever, and the parties lereto each agree to submit themselves to the jurisdiction of such court.

18. GOVERNMENT CONTRACTS. If the items to be furnished hereunder are to be used in the performance of a United States Government contract or subcontract and a United States Government contract number appears on Buyer's order or other written communication to Seller, those clauses of the applicable United States Government procurement regulation which are mandatorily required by Federal Statute to be included in United States Government subcontracts will be deemed incorporated herein by reference and will control if inconsistent with any provisions of this contract.

19. ASSIGNMENT. This contract is binding upon and inures to the benefit of the parties hereto and the successors and assigns of the entire business and goodwill of either Seller or Buyer or that part of the business of either used in the performance of this contract, but will not be otherwise assignable except that Seller has the right to assign accounts receivable, or the proceeds of this contract. Nothing in this contract shall inure to the benefit of or be deemed to give rise to any rights in any third party, whether by operation of law or otherwise.

20. SEVERABILITY. If any of these Terms of Sale is declared invalid by a court, agency, commission or other tribunal or entity having jurisdiction thereof, the application of such provisions to parties or circumstances other than those as to which it is held invalid or unenforceable shall not be affected thereby, and each term not so declared invalid or unenforceable shall be valid and be enforced to the fullest extent permitted by law and the rights and obligations of the parties shall be construed and enforced as though a valid commercially reasonable term consistent with the undertakings of the parties under the order had been substituted in place of the invalid provision.

21. SET-OFF. Buyer may not set-off any amount owing from Seller to Buyer against any amount payable by Buyer to Seller, whether or not related to this contract.

22. MERGER. This contract constitutes the final written expression of all terms of the agreement relating to the transactions described on the front hereof and a complete and exclusive statement of those terms. This contract supersedes all previous communications, representations, agreements, promises or statements, either oral or written, with respect to such transactions (including, without limitation, any terms proposed by Buyer) and no communications, representations, agreements, promises or statements of any kind made by any representative of Seller, which are not stated herein; shall be binding on Seller. No addition to or modification of any printed provision of this contract will be binding upon Seller unless made in writing (referring specifically to Buyer's order) and signed by an officer of Seller. No course of dealing or usage of trade or course of performance will be deemed relevant to explain or supplement any term expressed in this contract.

GENERAL INSTRUMENT